The ESA Microelectronics Programme

Past, present and future

Sandi Habinc
European Space Agency

Presentation Outline

Trends in microelectronics developments:

- **From ASIC to VHDL core, via ASSP**
- **From qualified foundries to commercial processes**

Microelectronics in on-board avionics:

- **Microprocessors, microcontroller and DSP**
- **Telemetry and telecommand**
- **Spacecraft controller-on-a-chip**

VHDL cores:

- **In-house developments**
- **Commercial developments**

Payload application examples:

- **Single-chip imagers**
- **Particle detector front-ends**

Conclusions

Trends in Microelectronics Developments

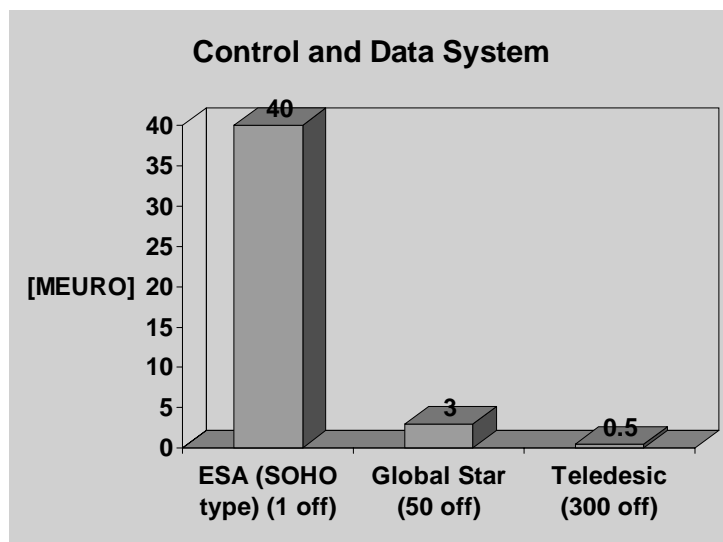# Cost Reduction Trend for Avionics

Requirements for commercial missions - reduction of:

- **cost**
- **power**
- **mass**
- **size**

This requires highly integrated equipment for platform and payload.

New time to market requirements.

Control and Data System

[MEURO]	

40
35
30
25
20
15
10
5
0

40

3

0.5

ESA (SOHO type) (1 off)   Global Star (50 off)   Teledesic (300 off)

From ASIC to VHDL Core, Via ASSP

- **VHDL adopted by ESA as preferred HDL in early nineties:**
  - **The only standard hardware description language**
  - **Multi-vendor support**
- **VHDL model delivery required for each ASIC developed, allowing ESA to independently verify the design**
- **ESA funded ASIC developments resulted in the delivery of prototypes or components integrated in equipment:**
  - **Difficult for competing companies to obtain the devices**
  - **Intellectual property (IP) rights owned by design house**
- **Application specific standard product (ASSP):**
  - **Components distributed and supported by european manufacturing foundry, under fair and equal conditions to all european buyers**
  - **VHDL model for board-level simulation required**
  - **IP rights still belonged to the design house**

Board-level Simulation

- **Much effort was spent on perfecting VHDL models for board-level simulation, addressing aspects such as functional accuracy, simulation performance and ease-of-use**
- **Difficult to establish an efficient distribution mechanism:**
  - **Allowing companies to get access to models without giving away design information**
  - **Pre-analysed VHDL models were often distributed**
- **An approach to commercialising the models was attempted but failed due to poor interest from companies, not being willing to pay for maintenance etc.**
- **Models have consequently been distributed free of charge by ESA to several companies who have been using them in both scientific and commercial spacecraft developments.**
- **Good results were achieved with models that were made available freely on the net, provided with no or limited support from ESA.**

VHDL Cores and Intellectual Property

- ASSP concept includes protection of European foundries:
  - ASSP designs are not open to other companies
  - Avoiding multiple competing implementations of the same function since it would decrease the interest for foundries to support the devices
- With only a few European foundries offering space qualified process, the above approach has been given less attention:
  - Board-level models are not an important output from ASIC/ASSP developments
  - Synthesisable VHDL cores are requested as a deliverable
- Other reasons for moving from ASSPs to VHDL cores:
  - Increased capacity of new qualified technologies allows System-On-a-Chip implementations of space applications
  - System houses are not integrating components anymore, they are integrating VHDL cores

---

From Qualified Foundries to Commercial Processes

Many radiation hard foundries have left the arena:
- reduced demand by former military customers
- no commercially interesting volume from space customers

Expensive to support European foundries which are only providing radiation hard technology:
- dual use approach
- commercial host process necessary

Current situation:
- single foundry in Europe, TEMIC, owned by ATMEL (US)
- increasing US dependence for radiation hard technologies
- tightening of US export licensing (Oct 17th, 1998)

The conclusion is that ESA must provide an alternative for microelectronic technologies that is independent of US and which is possible to fund within limited general budget.

Proposed Programme of Work

Usage of latest, advanced, deep sub-micron, non US dependent <u>commercial</u> technologies:

- **higher density, higher performance, lower power, lower cost, faster evolution**
- **avoid cost for new space specific process generation**
- **avoid dependence on government for survival**
- **no additional operational cost due to low space demand**
- **problem: radiation tolerance**

Possible solutions:

- **improve radiation performance through design**
- **fly more redundant systems**
- **shielding**
- **perform in-flight radiation monitoring**
- **activate/deactivate systems based on measurement**
- **deactivated systems in annealing mode**

Foreseen Activities

Initial verification activity:

- **Verification of necessity and applicability of specific radiation tolerant design techniques to large designs for commercial deep sub-micron technologies**
- **Consequence of having libraries with few elements**

Follow-on activity:

- **Develop library independently from foundries and industry**
- **Select complex applications and implement with the library**
- **Perform backend activities in an independent design house**
- **Manufacturing using Multi Project Wafer run**
- **Radiation performance evaluation of circuits**
- **Investigate appropriate quality assurance approach and establish requirements to ensure adequate reliability levels**
- **Adaptations of the library to new technology generations**

**Regular evaluation activities to validate performance**

Long Term Commitment

Discuss and agree the approach with the relevant European industrials concerned:

- **Select a deep sub-micron technology (0.18 μm), preferably from or at least accessible through a European foundry without US dependence**
- **Long term agreement with foundry, to ensure availability of the technology for low volume production**
- **Long term agreement with a design centre, independent from foundry and space industry, to ensure maintenance of library to cope with tool and technology evolution**
- **Allocate adequate financial resources in the ESA general budget to cover continuous technology development**
- **Set up a support centre in ESA**
- **ESA to take a more direct role in this activity, a shift from being the customer to being a provider**

Microelectronics in On-board Avionics

Microprocessors
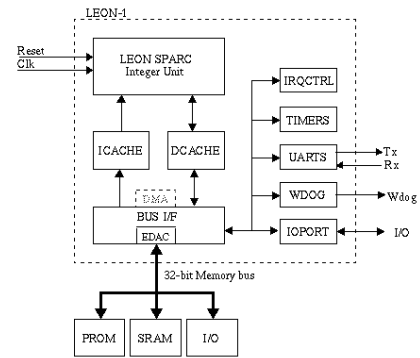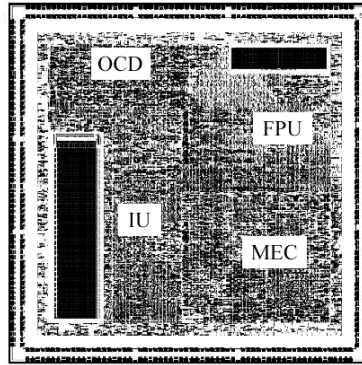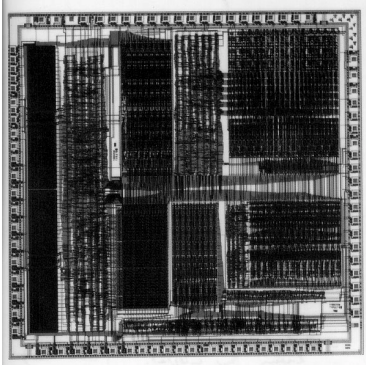
| MA31750	Single Chip SPARC TSC695E	LEON (SPARC V8)
MIL-STD-1750	**Operating Range**	**synthesizable, 27kgates + RAM**
3 MIPS	2.7V up to 5.5V from -55°C to +125°C	**fault-tolerant, 100 MIPS**
16 bit/32 bit ALU	2.5V capability from -55°C to +125°C	**instruction & data caches**
Hardware Multiplier (24bx24b) and Barrel Shifter (32b)	**Performance**	**32-bit memory bus with EDAC**
	25 MIPS , 5 MFIOpS @ 35 MHz, 5V, 1.5W	**interrupt controller, timers**
	14 MIPS , 3 MFIOpS @ 20 MHz, 3V, 0.4W	**UART, 16-bit I/O port**
		write protection, watchdog
MITEL 1.5 μm, SOS Proprietary design	**TEMIC 0.5 μm MG2RT IU block from Cypress FPU block from MEIKO**	**TEMIC 0.35 μm MH1RT IP developed & owned by ESA**

Microcontroller

Microcontroller based on 8032 VHDL Core:

- **Memory management, extension and protection**
- **De-multiplexed Address/Data bus**
- **One RS232 UART**
- **Three USARTs (RS232, PacketWire or TTC-B-01)**
- **Communication FIFOs**
- **Three 16-bit counters with extended time count duration**
- **CRC acceleration**
- **Program downloading and program execution from SRAM**
- **TEMIC MG2 0.5 μm Sea-of-Gates**
- **Radiation-tolerant, latchup-free, low SEU sensitivity**
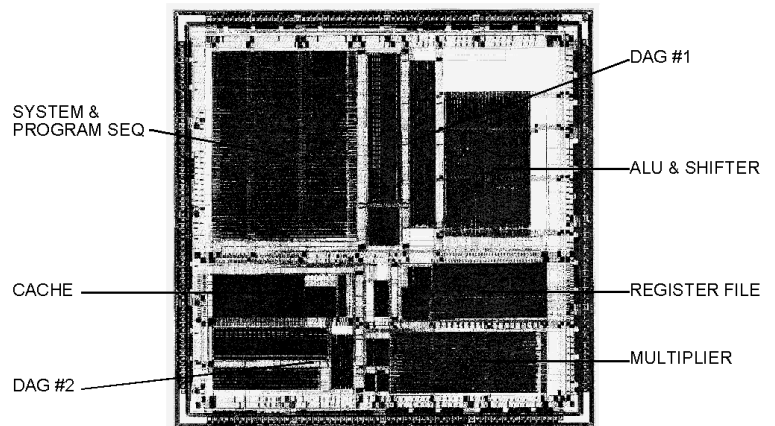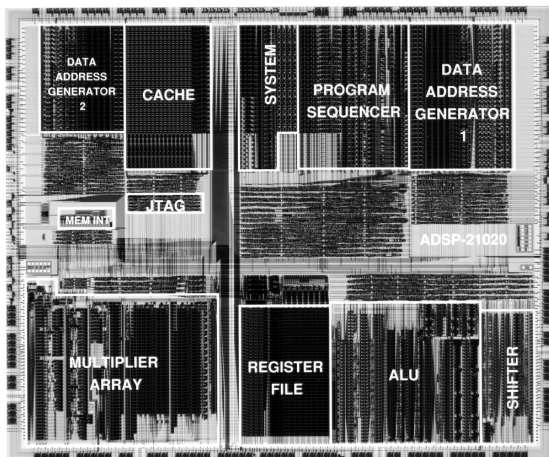- **Small 100 pin CQFP**

Microcontroller Architecture
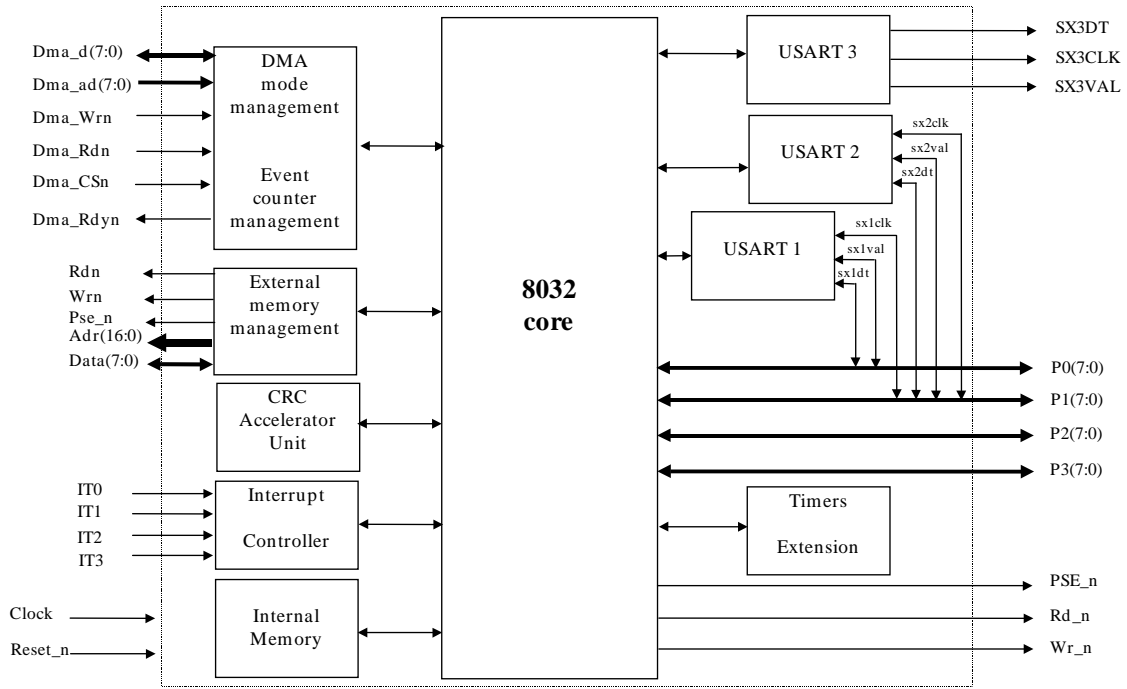
Digital Signal Processor (TSC21020)

- **Transfer from ADSP21020 to TEMIC/MHS TSC21020**
- **Radiation hard**
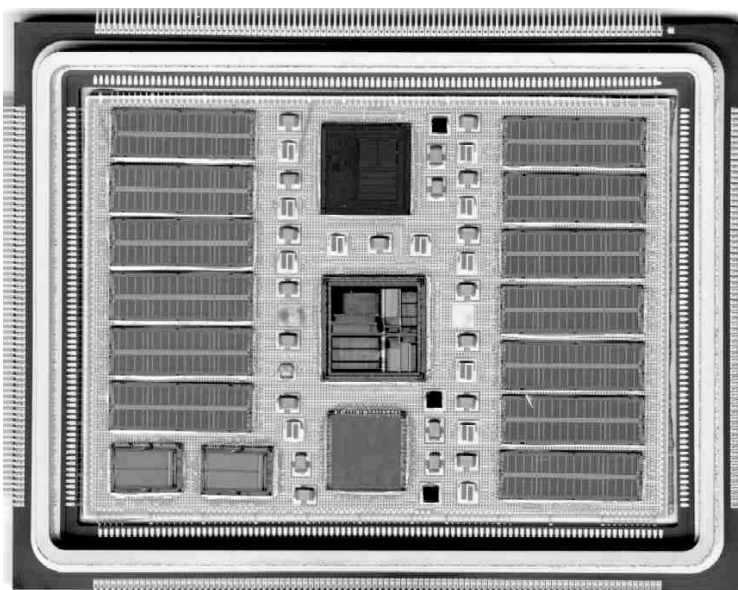- **Low sensitivity to SEU**
- **Latchup free**

DSP Peripheral Controller

The DSP Peripheral Controller (DPC) is a generic support device suitable for on-board applications using the TSC21020 processor. The device implements those support functions which are required for the integration of the processor with other devices in a board design:

- Initialisation of the Program Memory by DMA via the User Extension Interface or via the Synchronous Serial Link
- SRAM and DRAM support with write access protection
- 40-bit User Extension interface (automatic conversion to and from a 32-bit data)
- Powerful 16-bit programmable versatile IO port:
  - serial ports, 4 pulse generators, full duplex UART
- External interrupts, 32-bit timers, watchdog, CRC
- Radiation Tolerant better than 50 krad,
- Latch Up immunity better than 100 MeV.

TSC2102 & DPC MCM

- **TSC21020E Digital Signal Processor**
- **DPC ASIC**
- **Program and Data SRAM (4 * 128k32) with EDAC and write access protection**
- **DPRAM (2 * 8k16)**
- **IEEE-1355 Protocol Controller (SMCS)**
- **User Extension Bus Transceivers**
- **All silicon components from TEMIC (F)**

TSC2102 & DPC MCM Architecture

JTAG Interface

20 bits address bus
Control bus
48 bits data bus

Program Memory
(SRAM implementation)
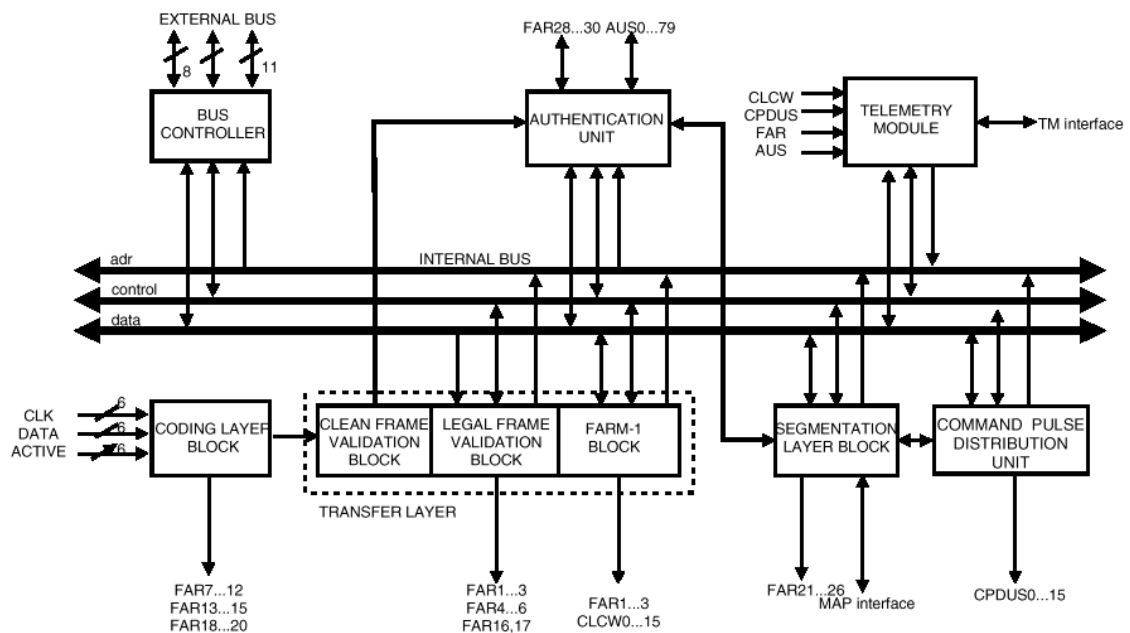
Check bits

JTAG Interface

Program Memory Interface

21020 DSP

Data Memory Interface

Interrupt Request

DPC

16 bits

Flexible IO Port

External Interrupts

Chip Select + Ctrl

User Extension Interface

Parity bit
32 bits data bus
20 bits address bus

Buffer

Parity bit
Data
Address

1355 Interface Controller

3 x 1355 serial links

Check bits
40 bits data bus
Control bus
20 bits address bus

Data Memory
(SRAM implementation)

CCSDS Telecommand Decoder Architecture

EXTERNAL BUS

8   11

BUS CONTROLLER

FAR28...30 AUS0...79

AUTHENTICATION UNIT

CLCW
CPDUS
FAR
AUS

TELEMETRY MODULE

TM interface

adr   INTERNAL BUS
control
data

CLK
DATA
ACTIVE

6
6
6

CODING LAYER BLOCK

CLEAN FRAME VALIDATION BLOCK

LEGAL FRAME VALIDATION BLOCK

FARM-1 BLOCK

SEGMENTATION LAYER BLOCK

COMMAND PULSE DISTRIBUTION UNIT

TRANSFER LAYER

FAR7...12
FAR13...15
FAR18...20

FAR1...3
FAR4...6
FAR16,17

FAR1...3
CLCW0...15

FAR21...26
MAP interface

CPDUS0...15

CCSDS Telecommand Decoder Subsystem
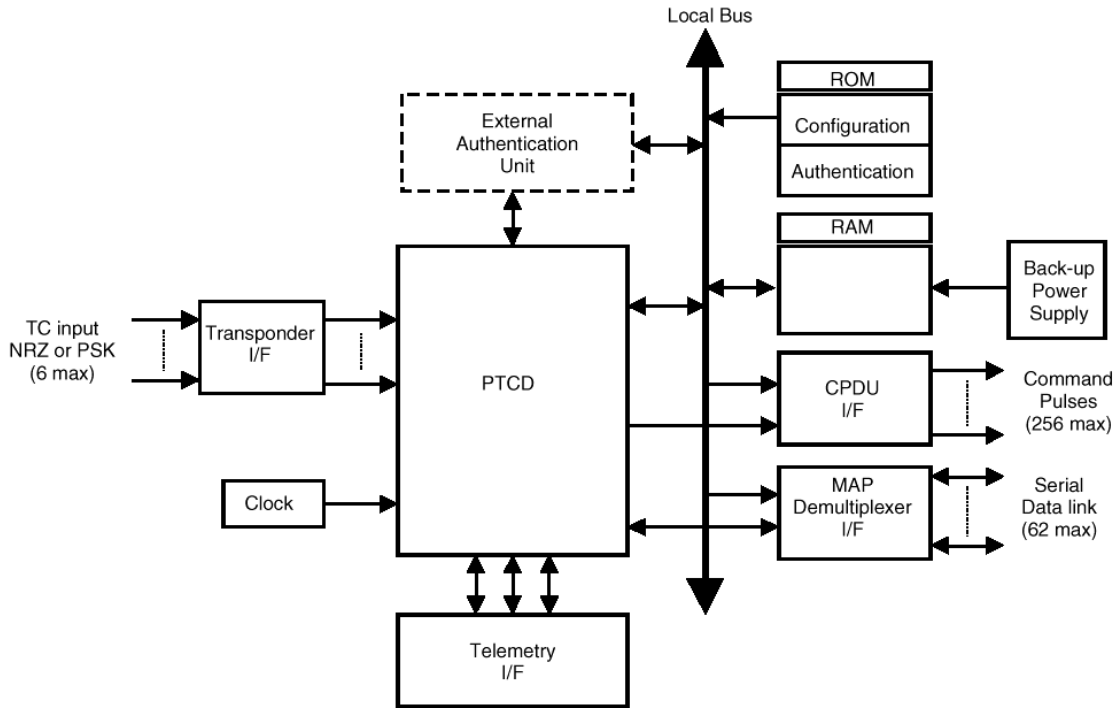
CCSDS Packet Telemetry Encoder

CCSDS Reed-Solomon Encoder

Frame		FrameOut
RSIn		RSOut
IL0	Control	Symbol
IL1	+	Symbol_N
IL2	NRZ-M	Ready
	+	
Advanced	Pseudo	
Mark	Randomiser	
Pseudo		

Check Symbol Memory

Serial Shift Register

Adder

Parallel Hold

Parallel Multiplier

RSIn → Reed-Solomon encoder → Pseudo-Randomiser (optional) → NRZ-M encoder (optional) → RSOut ⋯ CEIn → Convolutional encoder → CEOut

---

CCSDS Turbo Encoder

- ● Always connected
- ○ Never connected
- ◐ Connected every other symbol
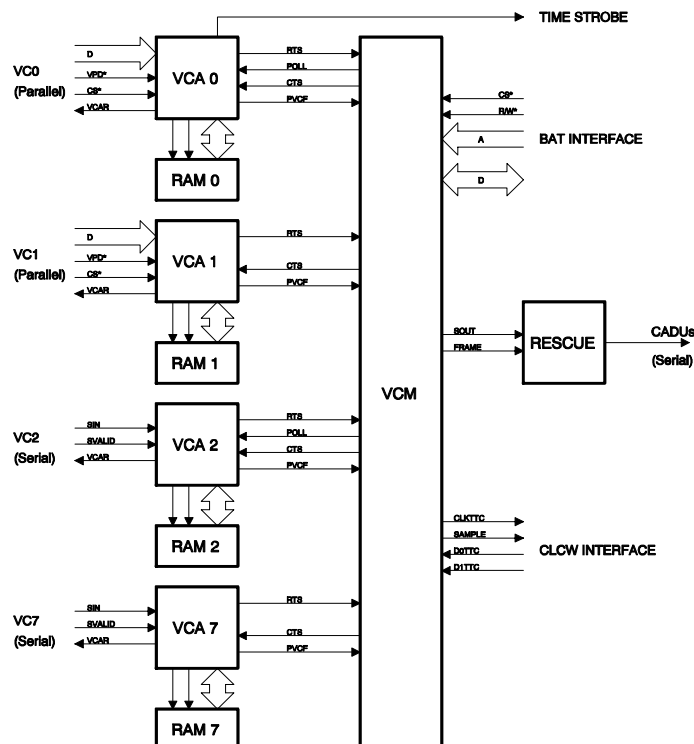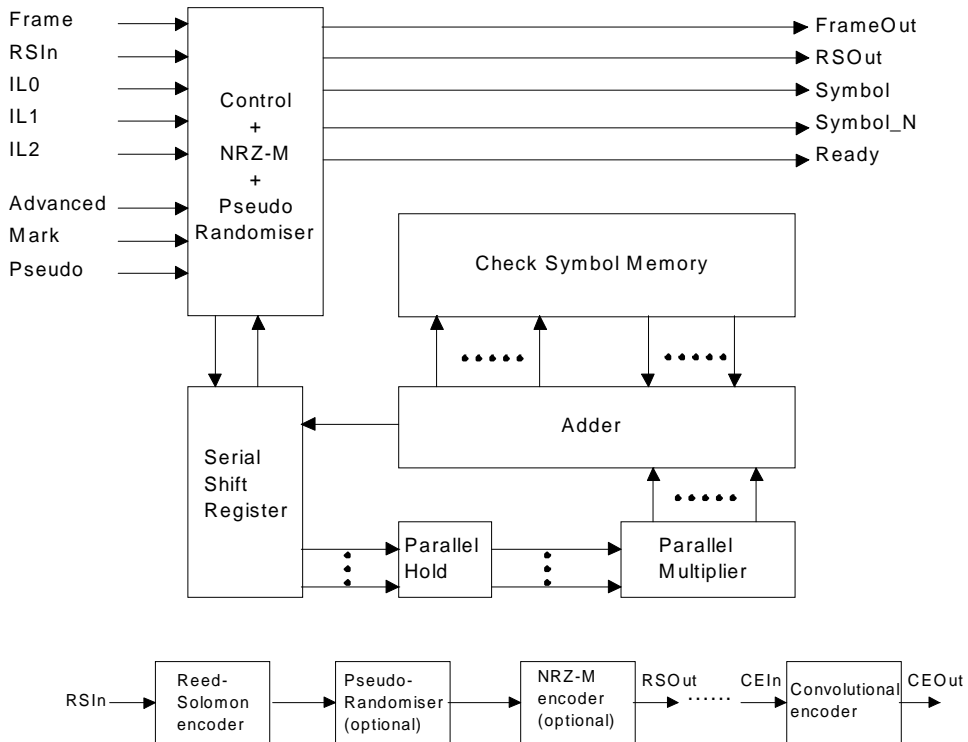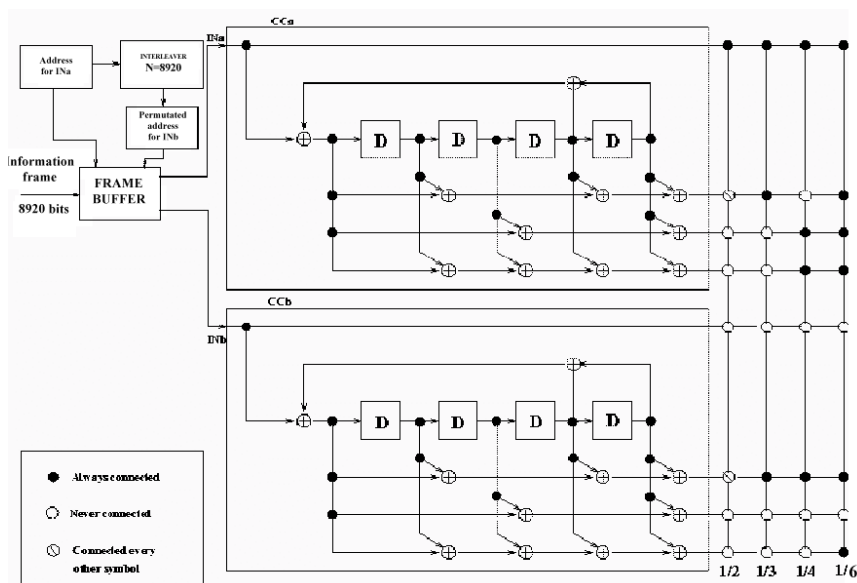
| Code Rate	Improvement [dB] @ FER = 10^{-4}	Improvement [dB] @ FER = 10^{-6}
1/2	1.7	≈ 1.2
2/5	2.0	≈ 1.6
1/3	2.3	≈ 2.0
1/4	2.5	≈ 2.0
1/6	2.7	≈ 2.0

Packetised Essential Telemetry Retrieval ASIC

- **Compliant to CCSDS/ESA Packet Telemetry Standard**
- **Synchronous PacketWire or RS232 (9600/115200 bps)**
- **40 discrete inputs, 32 can be used for analogue inputs**
- **8-bit ADC with selectable input ranges from 0-1 V or 0-4 V**
- **CRC and CCSDS/ESA Time Reference Field in packet**
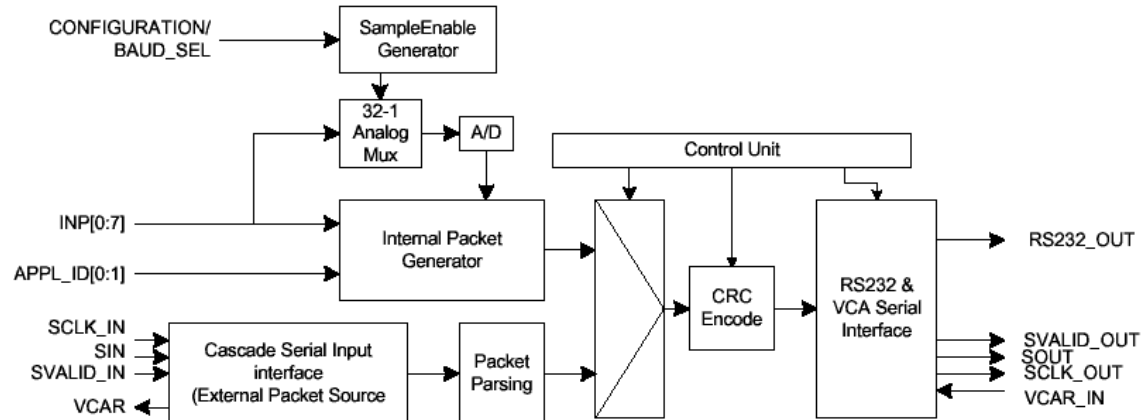

PETRA in a Spacecraft System

- PETRA devices can be cascaded to provide housekeeping and monitoring service through out the spacecraft.
- The information can be routed to the Central Processor using an asynchronous interface (also suitable for testing).
- The information can also be routed directly to the Packet Telemetry Encoder using a PacketWire interface.
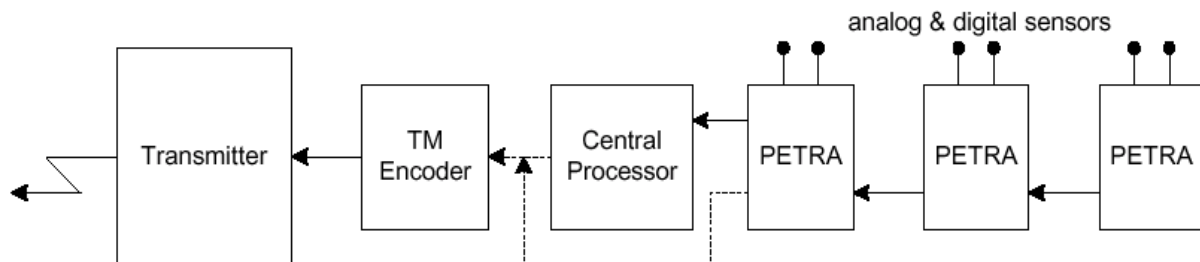
Local Time Management System (LTMS)

- **CCSDS CUC Elapsed Time**
- **Time resolution from 2^{-19} to 2^{-22} of a second**
- **μP interface**
- **Time stamp & alarm clock**
- **Stopwatch**
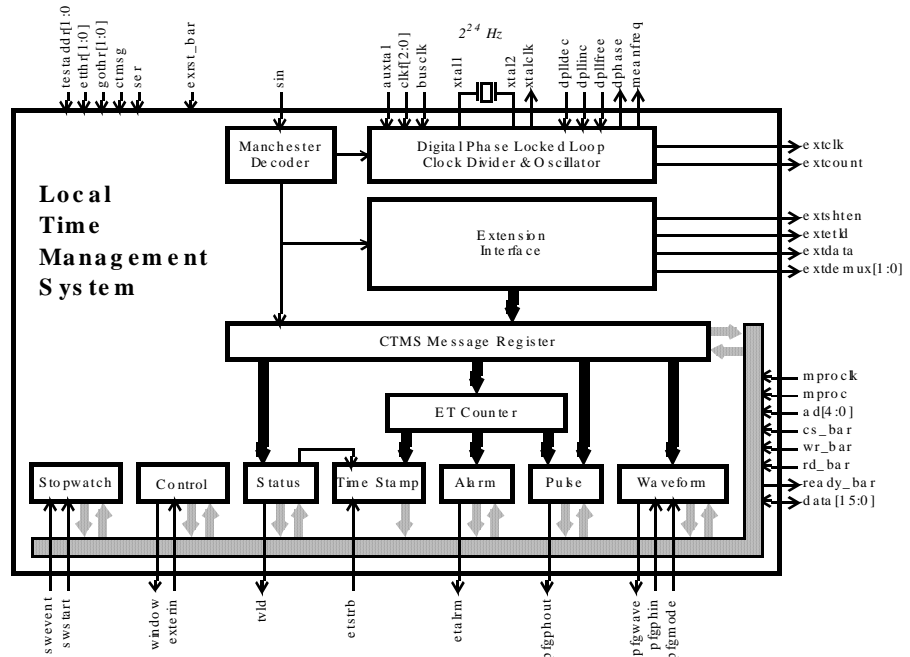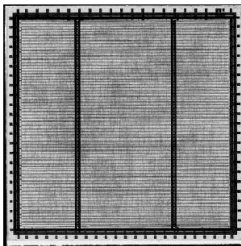
Advanced GPS/GLONASS ASIC (AGGA)
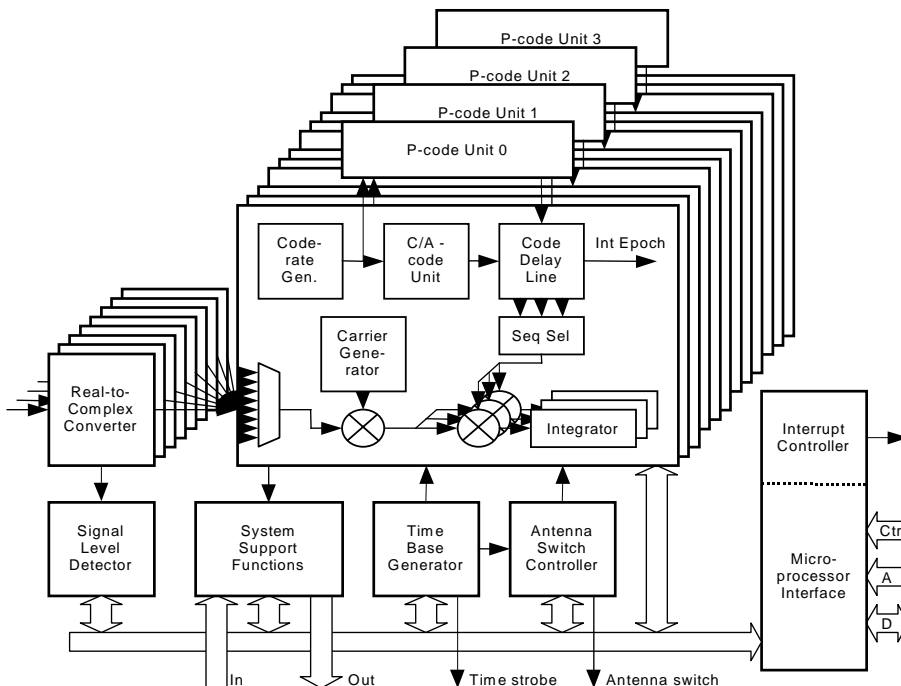
Specifications

- **0.7 μm Std-cell Alcatel Microelectronics 826 ktransistors**
- **0.5 μm Sea-of-Gate TEMIC (F) 200 kgates**
- **IF sampling, R-to-C conversion, final down-conversion, 12 channel, highly programmable**
- **Features for multipath mitigation and adaptive semi-codeless tracking of Y-code**

Applications
- **Spacecraft control**
- **Orbit determination**
- **Atmospheric sounding**
- **Reference stations**

Spacecraft Controller-on-a-Chip (SCOC)

- **VHDL cores are being used in a pilot SOC demonstrator development under ESA contract**
- **A complete data handling system is being designed as a single digital device**
- **The design is entirely based on cores or reuse of existing building blocks.**
- **Both ESA in-house, commercial and company specific cores are used**
- **The device is expected to comprise some 300 kgates and**
- **300 kbits on-chip memory**
- **Commercial Alcatel Microelectronics 0.35 μm standard-cell CMOS process is the current baseline**

SCOC Architecture
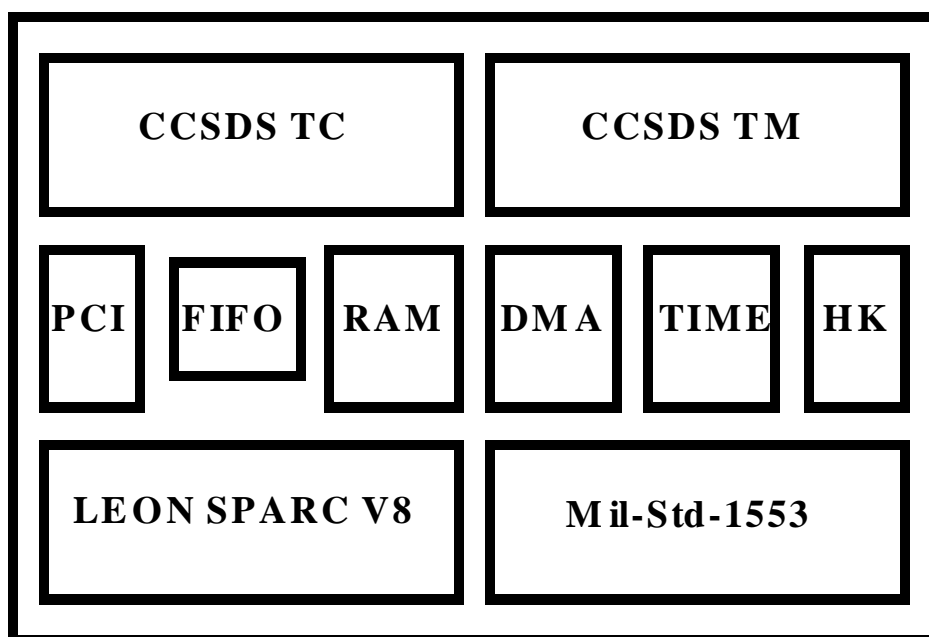
CCSDS TC			CCSDS TM		
PCI	FIFO	RAM	DMA	TIME	HK
LEON SPARC V8			Mil-Std-1553		

SCOC Block Diagram
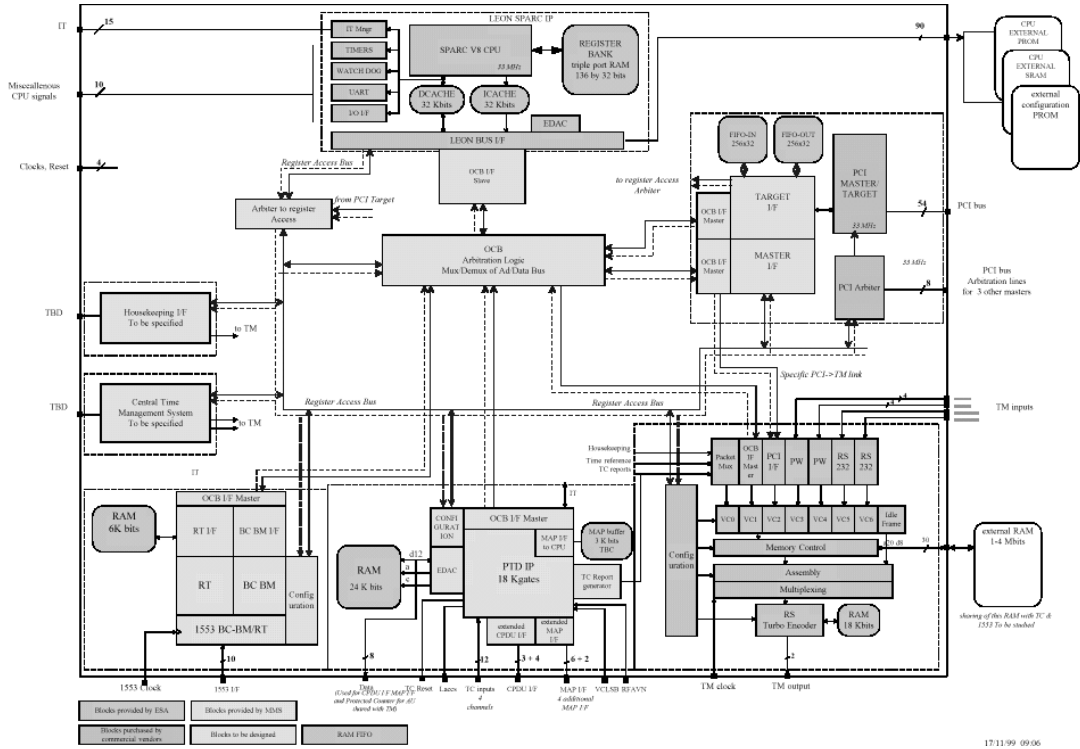
VHDL Cores

Managing VHDL Cores

In a pilot ASIC development using and producing VHDL cores the following principles were laid down to manage the cores:

- Cores that are provided by ESA to the contractor should remain the property of ESA, including any modifications.

- Licensing rights for commercial cores that are purchased as part of the development should belong to ESA, with the right to sub-licence/distribute the cores to European space companies.

- For VHDL cores developed in the contract, ESA should be granted the ownership, with unlimited rights to distribute the core to European space companies.

- For existing VHDL cores belonging to the contractor, considered as background information, ESA should be granted the right to use them for in-house developments.

Developing VHDL Cores

- For each VHDL core that is required in ASIC developments a trade-off is being made between an in-house development, contracted development or purchase of a commercial core.

- In many cases it has been considered important to have full and unlimited property rights to VHDL cores for certain key functions. These developments require in-house expertise.

- The advantage of in-house developments is that the cores can be freely distributed on the net. There are no restrictions related to non-European users. The benefit is that a larger user base can be addressed, which can potentially provide vital feedback, allowing continuous improvement of the cores. The disadvantages are issues such as support, quality level etc.

- The output from ESA funded developments are by default restricted to the member states, making distribution difficult.

Purchasing VHDL Cores

- **Quality level of VHDL code and documentation of commercial cores is not always complying to standards.**

- **Independent verification efforts have been made for a commercial core and three serious bugs were found. The core had been validated and used in commercial products.**

- **Modifications for SEU protection etc. can be costly, often requiring a new verification or even new validation.**

- **Licensing issues are difficult to handle from ESA's point of view. ESA would like to buy the VHDL core once, but use it in multiple developments involving different companies. Two approaches are considered:**
    - **ESA allowed to sub-licence the core (ESA taking responsibility for contracting companies)**
    - **ESA purchases the core and subsequent buys are discounted (provider is handling contracting companies)**

In-house Developed VHDL Cores

CCSDS Telemetry Channel Encoders:
- **Reed-Solomon Encoder**
- **Convolutional Encoder**
- **Turbo Encoder**
- **Bundled with old packet TM encoders (VCA, VCM, TeamSat, TTC-B-01, PacketWire, etc.) 20kEURO**

CCSDS Packet Telemetry Encoder:
- **Replaces VCA and VCM**
- **New VHDL core optimised for multiple virtual channels using one external memory**
- **Reed-Solomon / Turbo / Convolutional encoders included**
- **Beta testing for those purchasing the above bundle**

CCSDS Time Code Format:
- **CUC compliant time management core**

Free In-house Developed VHDL Cores

VME Bus Controller (EVI32):

- **Targeted to the ERC32 SPARC V7 chip set**
- **Freely available:**

  www.estec.esa.nl/wsmwww/erc32/evi32.html

SPARC V8 (LEON):

- **SPARC V8 based CPU with SEU protection and error handling**
- **Freely available:**

  www.estec.esa.nl/wsmwww/leon

CAN Local Bus

- **In-house reference development**
- **Freely available:**

  ftp.estec.esa.nl/pub/ws/wsd/CAN

SPARC V8 - LEON

FREE LEON IS EUROPEAN AGENCY'S SPARC-LIKE CORE
Includes separate instruction, data caches, 32-bit memory bus

*Universal asynchronous receiver/transmitter

SOURCE: EUROPEAN SPACE AGENCY
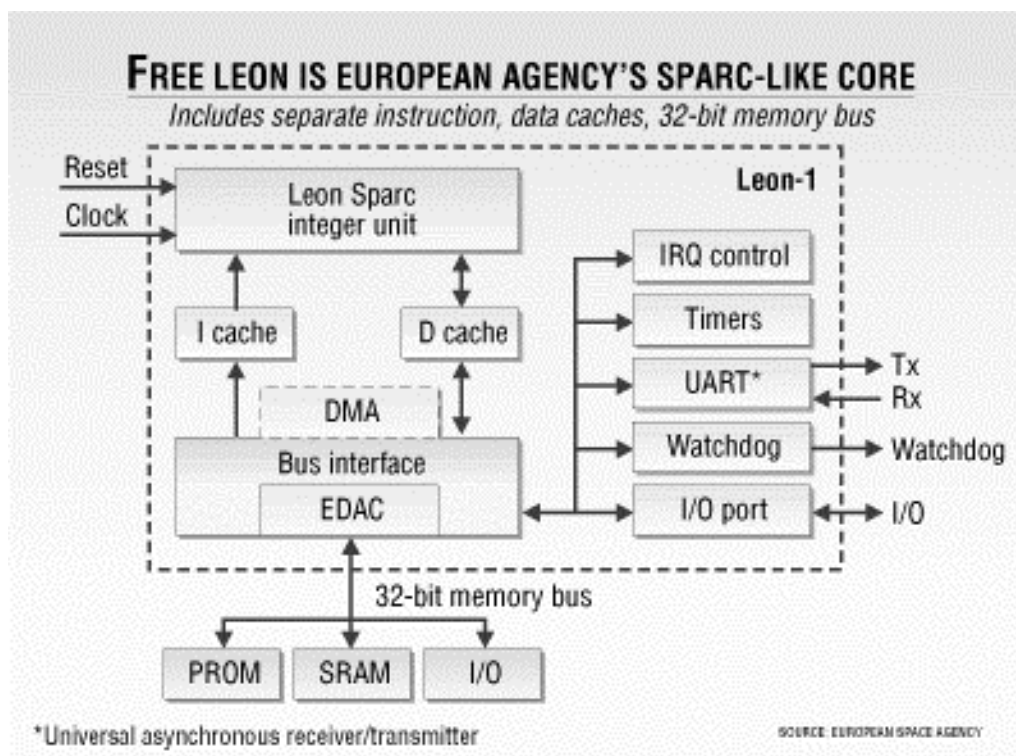
Industrial VHDL Cores

CCSDS Packet Telecommand Decoder:

- **Baseline is that the VHDL code from the development of the existing PTD will be provided to ESA. The code has been validated in-flight.**
- **VHDL code to be limited to European developments under ESA contract.**
- **In addition: partial in-house development completed, follow-on planned this year.**

Wavelet Image Compression:

- **Research development targeting a commercial process**
- **Design written in C++, from which VHDL can be generated.**
- **Core limited to space applications under ESA funding.**

Ongoing VHDL Core Developments

PCI Local Bus (32 bit / 33 MHz)

- **In-house development**
- **Low cost alternative to commercial cores**
- **Requires continuation covering verification and validation**
- **In-house follow-on considered**

PSS-04-0255 Bus Terminal

- **Industrial development**
- **Initially available to European space companies**

IEEE 1355 (SpaceWire)

- **In-house development initiated**
- **Low cost alternative**

Purchased/Planned VHDL Cores

Intel 8032 compatible VHDL core

- **ESA has the right to sub-licence to European companies developing ASICs under ESA contract**
- **20kEURO per development**
- **Richard Watts and Associates (RAW) (UK)**

PCI Local Bus (32 bit / 33 MHz)

- **ESA has the right to appoint European companies under ESA contract for a discount fee**
- **15kEURO per development**
- **InSilicon (formerly Phoenix/Sand Microelectronics) (USA)**

Mil-Std-1553

- **Available from European source**
- **ADV Technologies (F)**

Payload Application Examples

Single-chip Imagers

Integrated Radiation-tolerant Imaging System Series

Integrated Radiation-tolerant Imaging System (IRIS) is a series of running ESA developments aiming at a single chip monitoring imaging system:

- **IRIS-1**
    - **Sensor and ADC only**
    - **Control logic and spacecraft interfaces in an FPGA**
    - **Silicon available and chosen for space flight**
- **IRIS-2**
    - **Integration of sensor and logic**
- **IRIS-3**
    - **High resolution and local image memory, with companion compression chip (wavelet algorithm)**
    - **Radiation-tolerant chip set**

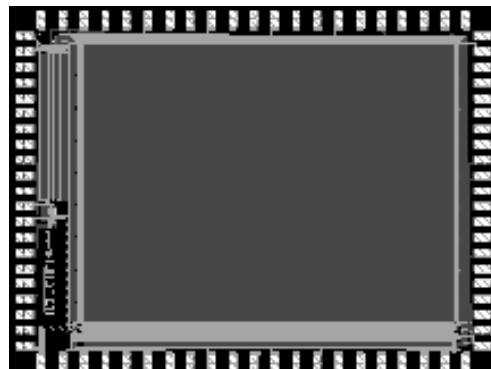**Developed by IMEC and FillFactory (B).**

Integrated Radiation-tolerant Imaging System - 1

- **CMOS APS**
- **640 x 480 pixels**
- **8 bits digitisation on-chip**
- **10 images per second**
- **optional colour filters**
- **support for windowing**
- **on-chip double sampling for image non-uniformity correction**
- **0.7 μm process**
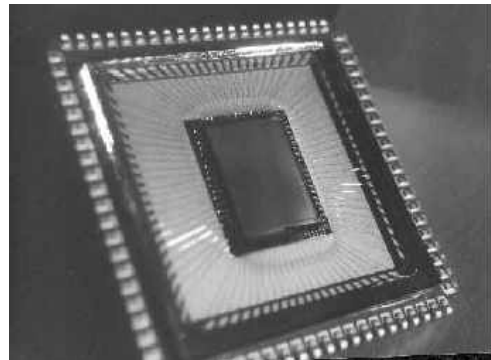
Integrated Radiation-tolerant Imaging System - 2

Operational miniature radiation-tolerant camera with few components:

- **IRIS chip, power supply and line drivers**
- **Easy to use as stand-alone camera on spacecraft**
- **Standard ESA interfaces and packetising protocol**

Application areas:

- **Monitoring and visual telemetry**
- **Low-grade earth and planetary imaging**
- **Low-end image gathering on small platforms such as planetary probes, lander and rover near imaging**
- **Robotics (high frame rates and windows)**
- **Spacecraft optical guidance and navigation**

Integrated Radiation-tolerant Imaging System - 2

Format:	**640 x 480, pitch 14 μm**
Architecture:	**integrating 3-transistor photo diode pixel, double sampling column amplifiers**
Speed:	**3 million pixels per second, up to 10 full frames per second, more when windowed or sub-sampled image frame**

Windowing, sub-sampling, interleaving, digital pixel binning

Standard spacecraft interfaces

Serial digital command interfaces

Serial and parallel digital pixel data interfaces

Analogue or digital (8 bit) pixel data output

Raw data or CCSDS/ESA standard packetisation (TM/TC)

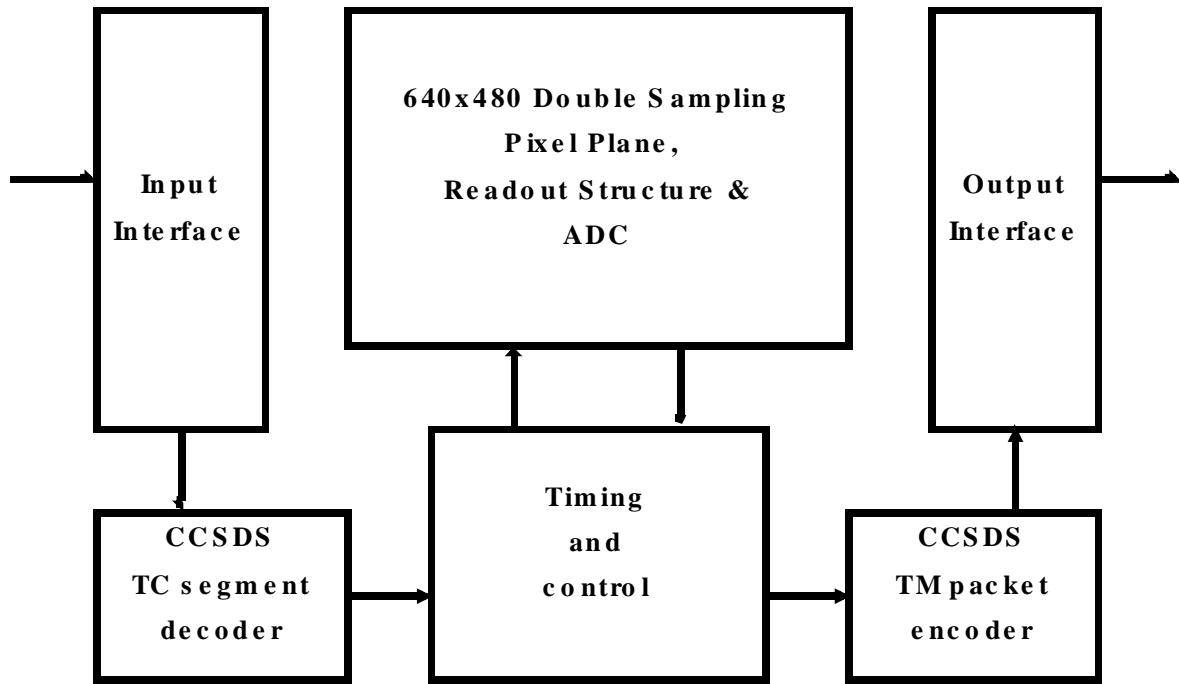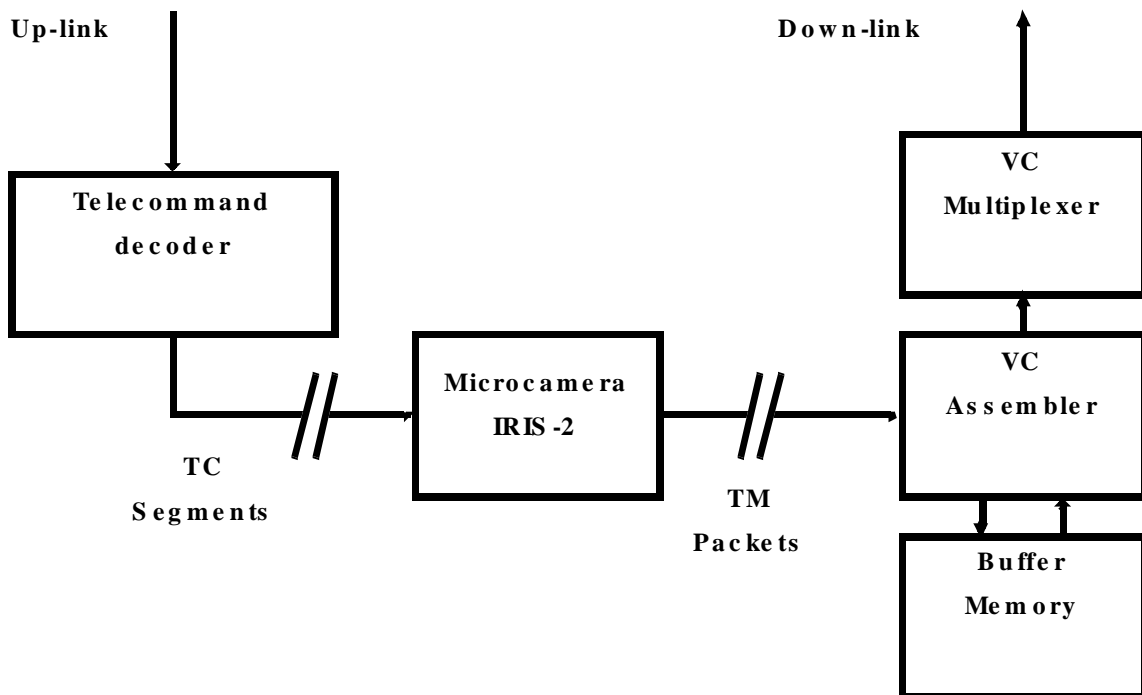# IRIS-2 Sensor Architecture

```
┌──────────────┐      ┌─────────────────────────────┐      ┌──────────────┐
│              │      │  640x480 Double Sampling    │      │              │
─→│   Input      │      │      Pixel Plane,           │      │   Output     │──→
│  Interface   │      │   Readout Structure &       │      │  Interface   │
│              │      │         ADC                 │      │              │
│              │      └─────────────────────────────┘      │              │
│              │             ↑        │                    │              │
└──────────────┘             │        ↓                    └──────────────┘
        │             ┌──────────────┐                          ↑
        ↓             │   Timing     │                          │
┌──────────────┐      │    and       │      ┌──────────────┐
│   CCSDS      │  →   │   control    │  →   │   CCSDS      │
│ TC segment   │      │              │      │ TM packet    │
│  decoder     │      │              │      │  encoder     │
└──────────────┘      └──────────────┘      └──────────────┘
```


Envisaged Spacecraft Integration of IRIS-2

Up-link   Down-link

```
   │                                              ↑
   ↓                                              │
┌──────────────┐                         ┌──────────────┐
│ Telecommand  │                         │     VC       │
│  decoder     │                         │ Multiplexer  │
│              │                         │              │
└──────────────┘                         └──────────────┘
   │                                              ↑
   ↓          ┌──────────────┐                    │
              │  Microcamera │          ┌──────────────┐
     //   →   │   IRIS -2    │   //  →  │     VC       │
              │              │          │  Assembler   │
  TC          └──────────────┘          │              │
Segments         TM                     └──────────────┘
               Packets                     ↑      ↑
                                        ┌──────────────┐
                                        │   Buffer     │
                                        │   Memory     │
                                        └──────────────┘
```

# Integrated Radiation-tolerant Imaging System - 3

- **Sensor size: 1024 x 768 pixels, 10 bits resolution**

- **Colour imaging capability, by overlaying a colour filter matrix**

- **Performance: visual and near infrared spectral response; 3 lx sensitivity low noise, high anti blooming, low pixel non-uniformity, high fill factor and quantum efficiency**

- **Frame rate: at least 10 Hz for the full frame at 10 bit pixel depth, higher full frame rates using lower pixel resolutions**

- **Readout options: sub-windowing, interlacing, local memory**

- **Radiation tolerance: target total dose 50 krad, latch-up free and low sensitive to single event upsets**

- **Operating temperature: -40 °C to +65 °C as a minimum range**

- **Power consumption: 400 mW at maximum frame rate, featuring a low power mode, single 5 V supply**

IRIS-3 Sensor Architecture
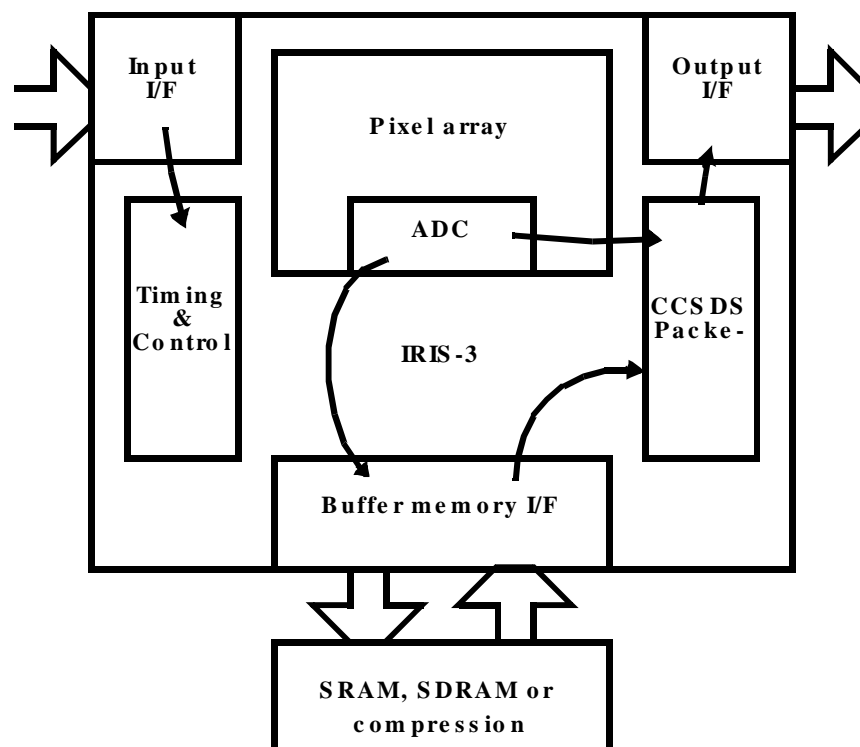
IRIS-3 companion: Image Compression ASIC

- **Wavelet compression - MPEG4 candidate**
- **Image size of 1024x768 pixels, supporting windows**
- **Pixel size from 8 to 12 unsigned bits per pixel**
- **High compression throughput**
- **Typical compression ratio between 3 and 40, user selectable**
- **Will store 100 compressed images (using a compression ratio of 10) in external memory protected by error correction code**
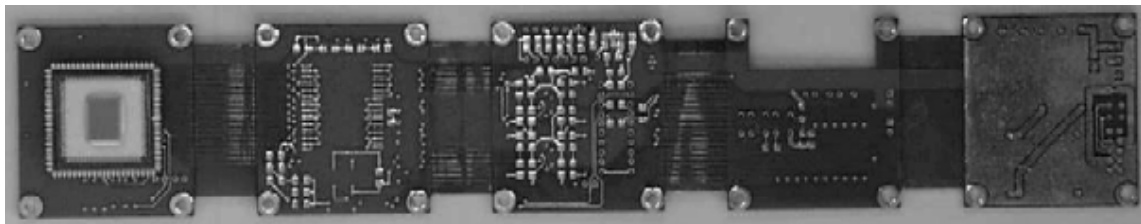- **Tightly coupled with IRIS-3**

IRIS

SRAM/SDRAM

ICA
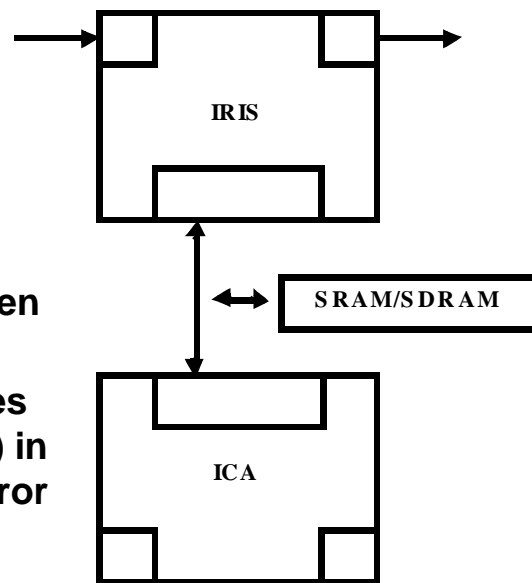
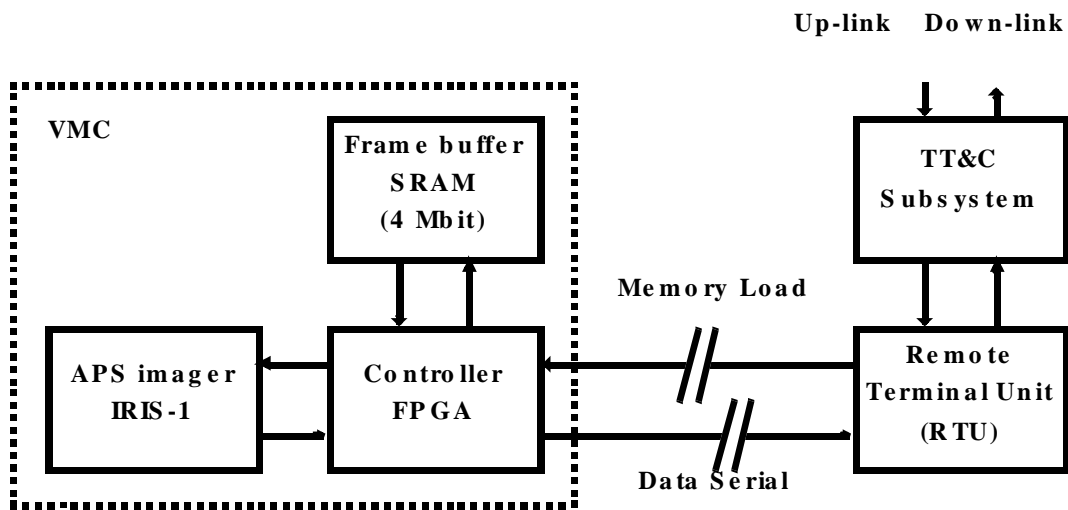
Visual Monitoring Camera

Sensor type: **IRIS-1 or FUGA15**

Image capture speed: **200ms**

Local buffer memory: **one image**

Interfaces: **TTC-B-01 to 1MHz or RS-422 to 3.125MHz**

Image download speed: one image per second

Power supply: either 28Vdc or 10Vdc

Power consumption: 5.0W & 28V or 2.0W @ 10V

Dimensions: 6x6x10 cm, 430 g

VMC Interfacing to Spacecraft

Up-link   Down-link

```
 ┌ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┐
 : VMC                         :                      ┌──────────┐
 :           ┌──────────┐      :                      │  TT&C    │
 :           │Frame buffer│    :                      │Subsystem │
 :           │  SRAM    │      :                      └──────────┘
 :           │ (4 Mbit) │      :                           │ ↑
 :           └──────────┘      :    Memory Load            ↓ │
 :  ┌─────────┐  ┌──────────┐  :                      ┌──────────┐
 :  │APS imager│ │Controller│  :  ─//─                │ Remote   │
 :  │ IRIS-1  │  │  FPGA    │  :                      │Terminal Unit│
 :  └─────────┘  └──────────┘  :  ─//─                │  (RTU)   │
 :                             :    Data Serial       └──────────┘
 └ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┘
```

VMC/IRIS-1: XMM-Newton
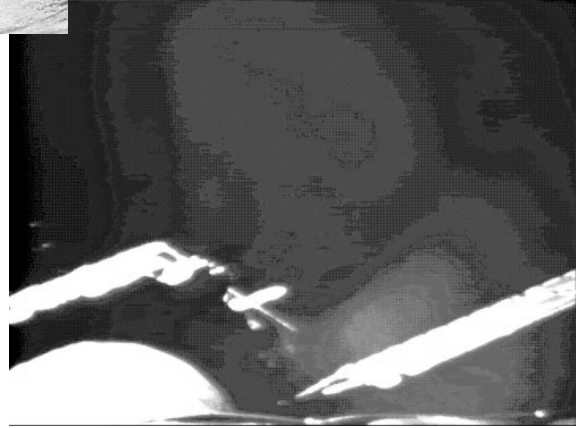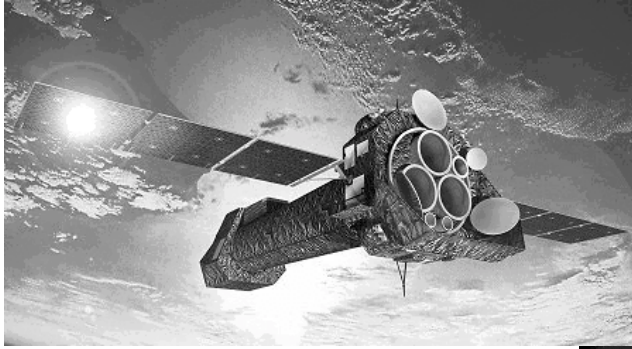
VMC/IRIS-1: Over-exposed image of Earth

During commissioning phase of the XMM-Newton X-ray space observatory, the two small Visual Monitoring Cameras snapped a picture of Earth at 45000 km distance.
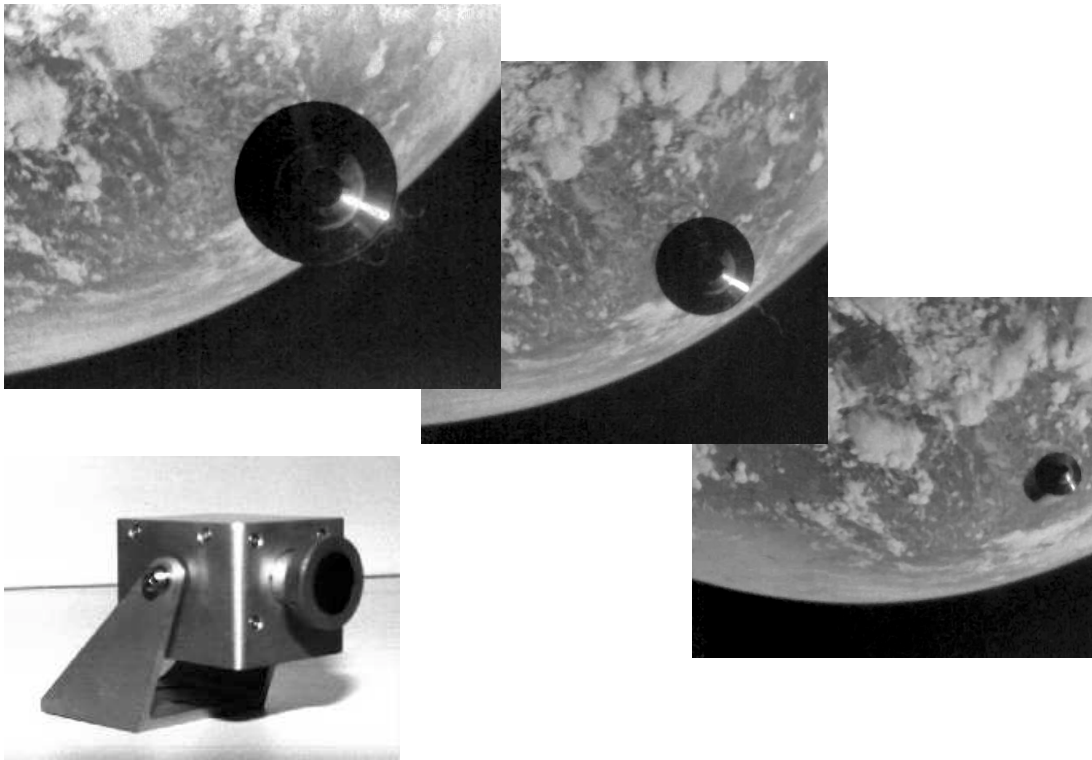
VMC/FUGA15 image of Earth

VMC/IRIS-1: Image of thruster plume

VTS/FUGA15 images from Ariane 502

CCD Based Microimager

Resolution: **1024 x 1024 pixels**

A/D conversion: **10 bits/pixels**

Power: **2.7 W, 3 supplies**

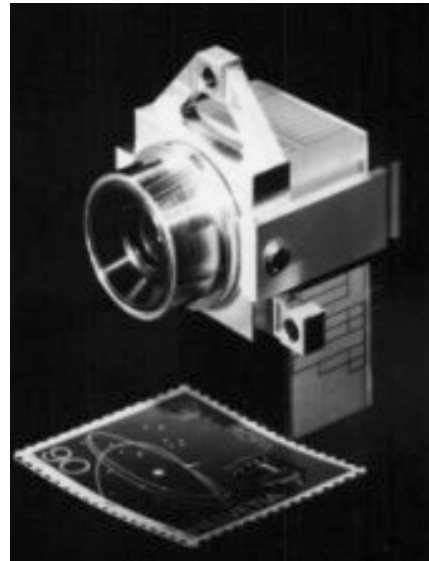**Serial RS422:**   **10 Mbit/s, or**
                       57600 bauds

Total weight: **35 g, optics and**
                       electronics

Field of view :   **41°, F:14**

Characteristics:

- **Integrated electronics comprising sequencer, converter, local picture storage.**
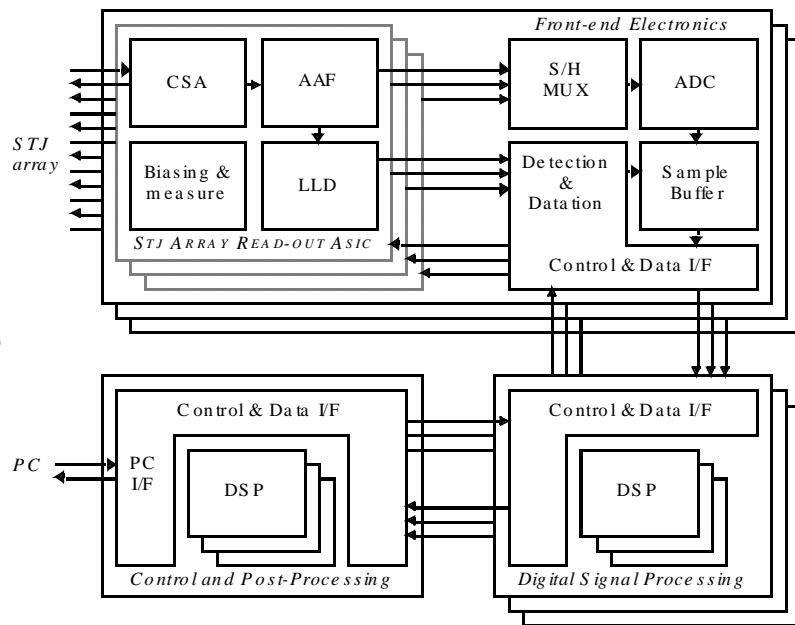
- **Easy operation and data acquisition.**

Microimager Architecture

- **Based on TH 7888 frame transfer CCD, with a dedicated packaging suited to be incorporated in the 3D technology.**

- **CCD driving interfaces and CCD output buffering board.**

- **CCD video signal sampling and A/D conversion board. This processing board includes two twin circuits: a Correlated Double Sampler TH 7982, and a A/D converter TS 83510.**

- **CCD clocks generator board, based on an Altera FPGA.**

- **I/O and control board, including a 16Mbit DRAM for image storage, RS-422 drivers for the serial links and an Actel FPGA for camera control and data throughput.**

- **The design is based on some 30 electrical components.**

- **Developed by CSEM (CH) and 3D-Plus (F).**

Payload Application Examples

Particle Detector Front-Ends

Particle Detector Front-End

- **Main channel: charge amp, pulse shape, base-line restorer, peak detector, S/H**
- **Coincidence channel for gating**
- **8-bit discriminators**
- **Gain adjust**
- **Linear 8-bit ADC**
- **Event driven**
- **Cascadable serial control interface**
- **Protected registers**
- **0.7 μm CMOS**

STJ Array Read-out Asic (SARA)

Superconducting Tunnel Junction array read-out ASIC:

- **Programmable biasing and bias measurement of STJ detectors**
- **Charge Sensitive Amplifier**
- **Anti-Aliasing Filter**
- **Low Level Discriminator w. programmable threshold**

Conclusions