DESIGNER'S INTERFACE

USING SYNTHESIZABLE CORES

(Contributed by Sandi Habinc of ESA)

The European Space Agency (ESA) has been developing, acquiring, and integrating synthesizable cores or intellectual property (IP) blocks for several years. The complexity of integrated circuits continues to grow with the increase in the manufacturing capability of silicon foundries. Hence, designers are increasingly reusing prebuilt blocks that have already been verified. For this method to be successful, it is desirable to have not only the hardware description language (HDL) model in source code format but also extensive documentation and even test stimuli and responses (known as testbenches). However, in the past, the space industry has been reluctant to provide HDL models for fear that the information would become available to competitors.

Increasingly, HDL cores are now made available to European space companies to reduce their dependency on one silicon foundry and also to assist them in designing their own custom system-on-a-chip (SOC) solutions. When space industry under ESA contract acquires HDL cores from IP suppliers, the HDL code is usually licensed to ESA for space-related activities. In some cases, ESA negotiates to reuse the HDL code should the developed device cease to be sold. For example, the first European radiation-hard Reed-Solomon encoder was developed in the 1980s and belongs to the original developer. When it was announced that the manufacturing of the component would be discontinued, new development was initiated in-house by ESA at its European Space Research and Technology Centre (ESTEC). These HDL models were then provided to external contractors who performed extensive verification of the new HDL models versus the discontinued part. The property rights of the modified and verified code were retained by ESA.

Presently, ESA is developing in-house an optimized encoder for packet telemetry. The HDL core has been used for both an in-house programmable gate project and for an industrial SOC project. All of the previously developed testbenches used in verifying the corresponding discrete solution were reused. The telemetry encoder is currently being distributed to companies from ESA-member states In another project that involves a telecommand decoder, ESA will need access to the HDL core, so it is acquiring the rights to the code for European companies developing ASICs under ESA contracts.

In 1997, ESA initiated the SPARC V8 (LEON) project to develop a high-performance processor to be used in space projects. The objectives for the project were to provide an open, portable, and nonproprietary design that was capable of tolerating single event upsets (SEUs). To maintain correct operation in the presence of SEUs, extensive error-detection and error-handling functions are needed. The goals are to detect and tolerate one error in an arbitrary register without software intervention as well as to suppress SEU errors in combinational logic.

The LEON processor is based on a new SPARC V8 core developed in-house at ESTEC. The core will include an arithmetic unit capable of executing both single- and floating-point operations. For performance reasons, a data and instruction cache is used. To allow rapid prototyping and porting, the processor has been described in a foundry-independent, synthesizable HDL. It does not require any custom macro-cells apart from SRAM used for the caches and register file. The design is extensively parametrizable: register window size, cache size, fault-tolerance functions, and clocking scheme can be defined through a single configuration file. The HDL will be made available in two versions: a basic model that is freely available on the net and a second model that will incorporate the fault-tolerance features. By freely distributing the basic model, thereby increasing the user base, it is believed that any correction to the design will be contributed the same way as with open-source software.

For additional information, contact: Sandi Habinc (sandi@ws.estec.esa.nl), Jiri Gaisler (jgais@ws.estec.esa.nl) or http://www.estec.esa.nl/wsmwww/leon

Donald Bouldin, Editor