QC/172/RdM Issue 1, June 1992

ESA ASIC DESIGN AND ASSURANCE REQUIREMENTS

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Preface

This document represents the precursor of a specification of the same scope and objectives intended for issue within the ESA PSS-01 series of specifications. The present document and its planned successor are supplementary to the ESA PSS-01-60 specification 'Component selection, procurement and control for ESA space systems'.

The objective associated with this intermediate specification is to complete and refine the catalog of minimum requirements through practical application and discussion in the user community.

However, the intermediate nature of this document does not imply optional or limited applicability of the stated requirements unless agreed with ESA.

ABSTRACT

This specification establishes the basic requirements for the development of ASIC (Application Specific Integrated Circuit) components, related ASIC specific quality assurance requirements, prototype manufacture, testing and validation which are to be applied by contractors and subcontractors involved in the design and manufacture of ESA space craft and associated equipment in which the use of ASICs with specific reliability and quality requirements is mandatory.

This document shall be read in conjunction with PSS-01-60, "Component Selection and Control for ESA Space Systems".

Requirements which are specific to user programmable or configurable logic devices such as PLDs and FPGAs are not covered by this specification.

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Page	Change Item	Approved DCR No.

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SECTION 1. SCOPE

This specification establishes the basic requirements for the development of ASIC (Application Specific Integrated Circuit) components, related ASIC specific quality assurance requirements, prototype manufacture, testing and validation which are to be applied by contractors and subcontractors involved in the design and manufacture of ESA space craft and associated equipment in which the use of ASICs with specific reliability and quality requirements is mandatory.

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SECTION 2. GENERAL

2.1 APPLICABLE DOCUMENTS

The following documents are applicable to the extent specified herein:

ESA PSS-01-60 Component Selection and Control for ESA space systems.

ESA/SCC Specification system (Basic, Sectional, Generic, Detail).

Note: The ESA/SCC Specification System is considered part of the ESA PSS-01 specification system.

2.2 DEFINITIONS

The definitions listed in Annex A shall apply.

2.3 DESIGN INITIATION

2.3.1 GENERAL

The contractor shall be responsible for the preparation of the ASIC development activity. Prior to the start of the ASIC development programme the contractor shall confirm that the requirements of ESA PSS-01-60 paragraph 4.1 can be met by an ASIC implementation.

2.3.2 APPLICATION FOR DESIGN INITIATION

The contractor shall complete an ASIC Design Initiation Document (ADID) in accordance with the format given in Annex B for all ASIC component types requested to be developed for use in flight standard hardware. It is the responsibility of the contractor to ensure that all information necessary to obtain approval of the ADID is supplied to ESA before the development is initiated. A minimum of twenty working days shall be included in the contractor's schedule to allow for the ESA review of the ADID. ESA approval of the ADID does not imply the subsequent approval of the resulting Part Approval Document required per ESA PSS-01-60 after completion of the development activity.

2.3.3 FEASIBILITY STUDY

If necessitated by the extent of the ASIC requirements the justification to be provided within the ADID shall be substantiated by a feasibility study.

2.3.4 ASIC REQUIREMENT SPECIFICATION

The ASIC Requirement Specification shall specify in written form as a minimum the following design objectives:

ASIC Function and Interfaces
Function and interfaces of the ASIC shall be specified with explanatory figures, tables, block and/or flow diagrams in sufficient detail to proceed with the architectural design.
For components providing software programmability associated software requirements shall be specified.

Performance Requirements
Performance requirements shall define the essential and critical target component characteristics and parameters such as power supply and consumption, performance, environmental operating conditions including radiation tolerance, reliability and others as relevant.

Testability Requirements
Testability requirements resulting from the system level shall be identified.

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SECTION 3. ASIC PROGRAMME MANAGEMENT

3.1 GENERAL

The contractor shall establish and implement throughout the duration of the contract an ASIC management programme which ensures full compliance with the requirements of this specification. The ASIC management programme forms part of the component control programme required per ESA PSS-01-60. The following requirements define additional conditions applicable to the development and use of ASIC components.

3.2 ASIC CONTROL PLAN

In addition to the requirements of ESA PSS-01-60 the ASIC control plan shall address in detail the following items:

- the ASIC Development Plan as defined in section 4 herein;
- ASIC specific quality assurance activities;
- design risk assessment and risk management.

3.3 EXPERIENCE SUMMARY REPORT

To improve the quality and reliability of ASIC components and to establish economic and efficient development and test requirements for future projects, the contractor shall collect, evaluate and present in an experience summary report any relevant information resulting from the experience gained during the execution of the ASIC development programme.

This report shall include:
- a summary of the major design objectives and constraints;
- an assessment of the actual development programme (e.g. controls, schedule, design iterations, communications);
- an assessment of EDA tool suitability and performance;
- an assessment of the manufacturer support;
- a presentation of nonconformances and problem areas;
- recommendations.

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SECTION 4 ASIC ENGINEERING

4.1 GENERAL

This section covers the contractor's responsibilities for the implementation of the engineering programme required for the development and procurement of ASIC prototypes to achieve the objectives defined in the ASIC requirement specification.

Section 4 of ESA PSS-01-60 shall apply.

4.2 ASIC DEVELOPMENT PLAN

4.2.1 GENERAL

The contractor shall prepare and maintain a detailed ASIC development plan in accordance with the general development flow defined below. This plan shall cover at least all phases of the ASIC development and major activities therein identifying milestones, interfaces, dependencies, decision points, type and number of design reviews, risk assessment, documents to be produced and the allocation of responsibilities.

4.2.2 ARCHITECTURAL DESIGN

This phase encompasses the architectural and algorithmic design, modelling and simulation and the definition of the test strategy. Adhering to a hierarchical and modular design style, partitioning shall be applied in consideration of performance, power consumption, size and cost requirements and constraints.

By default, VHDL shall be used for high level hardware description and simulation. Alternative high level hardware description languages and simulators shall only be used with ESA agreement.

Functionality and performance of the architecture shall be demonstrated by simulations to satisfy the ASIC requirement specification.

The test strategy shall be specified in accordance with the testability requirements.

The ASIC requirement specification shall be updated as necessary. The additional documentation to be produced (architectural design document) shall include as a minimum:
- the hardware description model,
- a description of the simulations performed and results obtained,
- the test strategy and associated hardware elements,
- block and state diagrams,
- timing information,
- the gate count estimate.

The architectural design phase shall be completed by a design review.

4.2.3 SELECTION OF TECHNOLOGY

Paragraph 4.7 of ESA PSS-01-60 shall apply.

4.2.4 DETAILED DESIGN IMPLEMENTATION

A structured and hierarchical decomposition of the high level design into a structural description on the level of elementary cells and fully defined circuit modules shall be completed and the associated netlist produced.

In the case that ESA/SCC capability approved technologies are used the relevant capability domain restrictions apply. Special circuits may be used according to the rules specified for the individual capability domain and in agreement with the manufacturer.

If other technologies are used exclusively those design tools and libraries shall be employed for which full foundry support exists and as far as they have been covered and approved in the technology evaluation programme. The use of special circuits outside of the standard library(-ies) supported by the manufacturer requires the manufacturer's agreement and ESA approval.

Digital ASICs shall adhere to the principle of synchronous design unless otherwise justified and agreed with ESA. Metastability shall be calculated and the resulting level shall not be lower than 100 years MTBF.

Circuit simulations shall be completed which incorporate adequate performance margins to cover as a minimum for worst case manufacturing spreads and power supply variations. The design shall be performed and simulated for the full Mil. temperature range. Radiation effects shall be simulated as required, possibly by means of dedicated simulation tools. The critical path(s) shall be simulated and specifically identified in the documentation.

The test stimuli set(s) shall be produced and the test documentation shall be prepared. By default fault simulation shall be performed to verify the required fault coverage level. Alternative methods of fault coverage computation require ESA agreement.

Constraints and any information necessary to achieve an efficient layout in the following phase shall be recorded. This should include, where it is required, floorplan information to minimise potential problems such as critical nets, clock and power distribution networks.

All previously established documentation shall be updated as required. The additional design information to be included in existing or new (detailed design document) documents shall cover at least:

- a schematic representation over all hierarchy levels according to international drawing standards (e.g. ISO/ANSI),
- the detailed pin description,
- major dc/ac electrical parameters as simulated or calculated,
- the netlist in EDIF format,
- the test stimuli,
- the gate count and (estimated) die size,
- the selected package type(s).

The detailed design implementation phase shall be completed by a design review.

4.2.5 ASIC LAYOUT AND FINAL SIMULATION

The ASIC layout shall be produced. Checking tools, such as LVS, DRC and ERC, shall be used.

Post layout circuit simulations, taking account of layout detail, shall confirm adequate performance margins which shall be agreed with the ASIC manufacturer and with ESA.

Die size, pin-out, and choice of package shall be confirmed. The bonding diagram shall be produced.

All existing documentation shall be updated and completed as required. The additional design information to be included in existing or new (detailed design document) documents shall cover at least:

- a layout verification and post layout simulation report,
- the floorplan, a layout plot, the bonding diagram,
- the component detail specification in ESA/SCC format.

The layout and final simulation phase shall be completed by a design review.

4.2.6 DESIGN RELEASE FOR PROTOTYPE MANUFACTURING

The release of the completed design for prototype manufacturing shall be authorised under the following conditions:

- all design simulations demonstrate that the requirement specification is met in all respects;
- the final design has been fully verified and passed at least the following checks:
  * Layout versus Schematic (LVS) check or Netlist Comparison Check (NCC);
  * Design Rule Check (DRC);
  * Electrical Rule Check (ERC);
- the foundry has issued a statement of compliance. In case of an ESA/SCC capability approved technology in the format agreed in the Process Identification Document (PID). For other technologies the form sheet provided in Annex C of this document shall be used;
- all relevant documentation as required by the development plan has been updated and approved;
- the layout design review has been successfully completed.

4.2.7 PROTOTYPE MANUFACTURE AND TEST

Prototype manufacture and test shall include the conversion of the test documentation into the test program, mask fabrication, wafer processing, assembly and testing.

A minimum of ten prototypes for each ASIC type shall be produced and tested.

The selected manufacturer shall be responsible for the preparation of a production test report to be delivered with the prototypes. Testing of the prototypes shall be performed against the draft ESA/SCC component detail specification. In agreement with ESA testing may be reduced but shall cover at least full table 2 measurements.

The manufacturer shall be responsible for the storage of all pattern generation files, associated data, test program(s) and the mask set(s) used for at least five years.

4.2.8 DESIGN VALIDATION

Design validation shall be performed to confirm the achievement of all functional, performance, interface and compatibility requirements. For this purpose an appropriate test set up or system breadboard shall be employed.

Design validation shall include radiation testing as required for the selected technology and per requirement specification.

The validation test set up shall be documented and the test scope, sequence and results shall be recorded in a validation test report.

After successful completion of the validation testing a component detail specification in ESA/SCC format shall be finalised.

4.3 TESTABILITY AND TESTING

Testing shall be functional, parametric and dynamic with due allowances for supply voltage variations, the temperature and radiation requirements.

Functional testing of digital components shall have, as a target, 100% fault coverage with respect to the stuck at fixed state fault model. Where this is not achievable 95% fault coverage is the normal acceptable minimum, with less than this being permissible only in exceptional circumstances. In all cases where fault coverage is less than 100% a justification shall be provided and untested circuit elements shall be documented.

100% toggle tests shall be performed.

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SECTION 5 ASIC QUALITY ASSURANCE

5.1 GENERAL

The quality assurance requirements defined in ESA PSS-01-60 shall apply.
It shall be the objective of the ASIC quality assurance programme to ensure the development of reliable, manufacturable, testable and reproducible ASIC components for Space application.

5.2 CAD TOOLS AND FORMATS

The tools to be used shall be specified by the contractor and require ESA approval unless covered within an ESA/SCC approved capability domain.

All technology independent CAD tools to be employed during the development shall be mature and fit for their purpose.

All technology dependant CAD tools shall be used as approved and supported by the selected manufacturer.

Preference shall be given to the use of established international standards. For example, VHDL as defined in IEEE 1076 and EDIF.

5.3 PORTABILITY

For ASICs with long term availability or multiple usage requirements prospective design portability shall be maximised as economically feasible. This shall include both design and manufacturing. Factors to be taken into account shall include but not be restricted to;

- alternative technologies and manufacturers,
- package and die size compatibility,
- compatibility of CAD Tools,
- effort/cost of design portation,
- interchangeability of processes and cell libraries,
- test stimuli description (high level language),
- simulation approach (hierarchical, block oriented),
- safe keeping of intermediate design files.

5.4 DESIGN REVIEWS

The contractor shall be responsible for the scheduling and performance of design reviews. They shall be defined along with the criteria for their successful completion in the development plan. Suitable representation, from design and quality assurance, from all relevant organisations shall be defined (ESA, system contractor, ASIC design contractor and ASIC manufacturer).

The contractor shall produce and circulate in advance of each design review a design review package containing a checklist based on the established acceptance criteria and the data necessary for the particular review.

The completion of the following design reviews is mandatory:

Feasibility Review

This review shall confirm the results of the feasibility study and result in the approval of the ASIC Requirement Specification and basic development plan. Direct or delegated ESA participation is mandatory.

Architectural Design Review

This review shall result in the authorization to proceed with the detailed design implementation. As a minimum it shall cover and approve the chosen architecture and algorithms, the testability concept, the documentation produced and updated in this phase and the technology selection.

Detailed Design Review

This review shall result in the authorization to proceed with the component layout phase. As a minimum it shall cover and approve the design decisions taken during the detailed implementation phase, the results of simulation, the conformance to testability requirements, the extend and results from simulation, the documentation produced and updated in this phase.

Post Layout Design Review

This review shall result in the approval for design release for prototype manufacturing. As a minimum it shall cover the chip layout and final simulations, the test plan and all documentation produced and updated in this phase. Direct or delegated ESA participation and manufacturer participation is mandatory.

Design Acceptance Review

This design review shall result in the final acceptance of the ASIC(s). As a minimum it shall cover the production test and design validation test results and all documentation produced and updated in this phase. Direct or delegated ESA participation shall be mandatory.

Additional design reviews shall be performed as needed.

A design review is completed and authorization to proceed may be given upon fulfilment of all acceptance criteria as defined in the development plan.

A design review identifying a limited number of only minor discrepancies can be completed after successful implementation of the corrective actions defined during the review.

A design review failing major acceptance criteria and resulting in a design iteration shall be repeated in full.

All design reviews shall be minuted.

5.5 DESIGN RISK ASSESSMENT AND RISK MANAGEMENT

The design risk for the timely and successful completion of the development activity shall be assessed. This shall include but not be limited to the following aspects:
- maturity and version stability of CAD tools used;
- technology availability;
- designer experience and training status;
- change of requirements during the development;
- design iterations and documentation consistency.

Extraordinary risks shall be covered by a contingency plan identifying alternative or back-up solutions.

5.6 DOCUMENTATION

At all stages of the ASIC development the contractor shall be responsible for the production, maintenance, control and archiving of all related documentation as defined in the ASIC development plan. This shall include as a minimum:
- the ASIC development plan;
- a record of CAD tools, libraries and associated data used and respective versions thereof;
- the ASIC requirement specification;
- the hardware description model and associated simulation results;
- the circuit block diagrams, circuit schematics, netlist(s) and associated simulation results;

- the design verification results as per paragraph 4.2.6 of this specification;
- the floorplan and detailed layout;
- the manufacturer statement of compliance;
- the test documentation;
- the prototype test and validation records and associated documents;
- the component detail specification in ESA/SCC format;
- all design review reports;

All documentation shall be produced in English, except where tool specific languages are used. Documentation may be stored on electronic media and delivered on the same as appropriate.

All documents shall be archived for a minimum period of five years after the completion of the development activity or as specified in the contract.

ANNEX A

DEFINITIONS

The definitions given below apply to the terms as they are used in this document.

Application Specific Integrated Circuit (ASIC)

The term ASIC (Application Specific Integrated Circuit) refers to a custom or semi-custom designed and manufactured monolithic integrated circuit.
An ASIC may be digital, analog or a mixture of both (mixed function).

ASIC Technology

An ASIC technology is the totality of all elements required for the design, manufacture and test of ASIC components (e.g.EDA tools, cell libraries and associated data, procedures, process technology).

Block Diagram

An abstract, graphical presentation of interconnected, named boxes (blocks) representing an architectural/functional drawing.

Cell

A specific circuit function.

Cell Library

A controlled and computerised library of mutually compatible cells which conform to a set of common constraints standardised interfaces.

Component Detail Specification

Procurement specification.

Data Sheet

A detailed functional, operational, and parametric description of a component including block diagram, truth table, pin/signal description, environmental, electrical and performance parameters, tolerances, timing information, package description etc.

Design Iteration

Design iterations are design changes which occur in any single phase or between two consecutive phases as defined in the ASIC development plan, before the design has been released for prototype manufacturing.

EDA

Electronic Design Automation

Fault Coverage

A measure, expressed in percentage terms, of the proportion of actually detectable versus all possible faults in a digital circuit, for a given set of test stimuli and with respect to a specific fault model.

Floorplan

An abstracted, scaled layout drawing of the die, outlining the form, size and position of the major functional blocks and pads.

Flow Diagram

An abstract, graphical presentation of interconnected, named boxes representing a flow of instructions, actions, events or operations.

HDL

Hardware Description Language (e.g. VHDL, Verilog).

HDL Model

A textual model based on a hardware description language suitable for the behavioral description and simulation of (digital) component.

Netlist

A formatted list of cells (basic circuits) and their interconnections.

Redesign

Design changes which affect more than two consecutive phases of the ASIC development plan or design changes which are implemented after release for prototyping.

Stuck-At-1/0 Level Fault Model

A fault model for digital circuits which distinguishes between the two failure modes of node stuck-at-(logic)1 or node stuck-at-(logic)0.

Testability

A design quality indicator based on the criteria of accessability, controllability and observability of all nodes in a circuit and the efficiency of test stimuli. Theoretical upper limit for fault coverage.

Test Stimuli

The binary test patterns used for simulation and test.

Test Vectors

The test patterns formated for the specific VLSI tester used for production/acceptance testing and complemented by test conditions.

Toggle Test

A test which switches every accessible node of a digital component from one logic state to the other.

VHDL

VHSIC Hardware Description Language, as defined in IEEE 1076.

VHSIC

Very High Speed Integrated Circuit (US Government research programme).

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ANNEX B

FORMAT FOR ASIC DESIGN INITIATION DOCUMENT

ASIC DESIGN INITIATION DOCUMENT

Sheet 1 of [ ]	Doc. No.: Issue : Date :
Project:	
Requester: Usage: ASIC ID: Req. Spec. Ref.:	
Complexity: Rad. Tolerance:	
Designer: Technology: Possible Mfr(s): Techn./Mfr. Eval.: Related ADID(s):	
Justification: Feasibility Study:	

ASIC DESIGN INITIATION DOCUMENT

Sheet 2 of [ ]	Doc. No.: Issue : Date :
Project:	
Layout by:	
Software Development:	
Development Schedule Start Date: Design Release Date: Prototype Fab.-out Date: End Date:	
Development Effort:	
Development Cost Design: Foundry: Validation: Techn./Mfr. Eval.:	Number of Prototypes:
Approval Prime Contractor: Approval ESA:	Date: Date:

GUIDANCE NOTE FOR COMPLETION OF

ASIC DESIGN INITIATION DOCUMENT

One ADID shall be completed per ASIC type.

Doc. No.:	Sequential unique number
Issue:	Sequential unique issue number/letter
Date:	Date of issue
Project:	Name of project intending to use the ASIC
Requester:	Name of company submitting the ADID
Usage:	Reference to equipment or system using the ASIC
ASIC ID:	Preliminary ASIC component identification, must include reference to ASIC function
Req.Spec.Ref.:	Document reference for requirement specification
Complexity:	Estimated gate count/die size, RAM-, ROM-, PLA size, pin count
Rad.Tolerance:	Minimum total dose radiation level and planned operational life, Single Event Upset tolerance
Designer:	Name of company designing the ASIC
Technology:	Identification of type of ASIC technology to be used (e.g. 1.0 micron CMOS SOS)
Possible Mfr(s):	Name(s) of manufacturer(s) for target technology
Techn./Mfr.Eval.:	State if the target technology and the manufacturer have been evaluated (ref.) or evaluation will be required (yes/no), plan ref.
Related ADID(s):	Provide reference to other ADIDs in case of interdependent ASIC developments (chipset) or previous ADID in case of Redesign
Justification:	State reasons or provide reference to separate justification document
Feasibility Study:	State reference to feasibility study report if existing
Layout by:	Name of company producing the layout
Software Development:	Reference to associated SW development activity (e.g. application, assembler)
Development Schedule:	State planned start date, design release date, prototype fab. out, end date
Development Effort:	Estimated design effort in man years
Development Cost:	Estimated design cost, prototyping cost, validation cost, technology/manufacturer evaluation cost
Number of Prototypes:	Required number of prototypes

ANNEX C

FORMAT FOR STATEMENT OF COMPLIANCE

STATEMENT OF COMPLIANCE

		Certificate No.:	
		Date :	
Manufacturer:			
ASIC ID:			
Designer ID:		Manufacturer ID:	
Designer:			
ASIC Technology:			
Process:	Version:	Release Date:	
Library:	Version:	Release Date:	
Netlist ID:	PG Tape No.:	Mask Set No.:	
Design Verification Tool	Run Set	Doc.Ref.	Pass Date
DRC:			
ERC:			
NCC/LVS:			
Other:			
Test			
Test Stimuli:		Test Program:	
Design Release Review			
Place:	Date:	Report:	
The design verification steps listed have been successfully completed. Netlist and Layout are fully compatible. The design is fully compatible with the referenced process.			
Certified		Date:	

GUIDANCE NOTE FOR COMPLETION OF

STATEMENT OF COMPLIANCE

One statement of compliance shall be completed for each ASIC before the design is released for prototyping.

Certificate No.:	Sequential unique number
Date:	Date of issue
Manufacturer:	Manufacturer name and address
ASIC ID:	ASIC component identification, must include reference to its function
Designer ID:	ASIC identification used by designing company if different from ASIC ID
Manufacturer ID:	ASIC identification used by manufacturer if different from ASIC ID
Designer:	Designer name and address
ASIC Technology:	Identification of manufacturing process and cell library with version letter and release date
Netlist ID:	Document/file/tape reference
PG Tape No.:	PG tape reference number
Mask Set No.:	Mask set reference number
Design Verification:	State name of the tool used to perform the design checks listed along with support files/run set references, reference to output document/files and the date of successful completion of the check
Test:	State reference numbers for test stimuli document/file and test program
Design Release Review:	Place and date of design release meeting and report document reference