GR740 User Day - Announcements

28 November 2019
Erasmus Auditorium - ESTEC
GR740 SBC Reference Design
Press release
GR-VPX-GR740 & GR-VPX-BM-MEZZ
CoRA Development Board for VPX

- **Processor board: GR-VPX-GR740**
  - GR740 Quad-Core LEON4FT Processor
    - 512 MiB SDRAM
    - 128 KiB MRAM
    - 32 MiB SPI Flash
  - Backplane I/F: 6x SpaceWire
  - Frontplane I/F and drivers:
    - Mil-Std-1553B, Ethernet, GPIO
    - USB/FTDI UART/JTAG Links
  - SpaceVPX / OpenVPX compatible

- **Mezzanine board: GR-VPX-BM-MEZZ**
  - NX1H35S BRAVE NG-Medium FPGA
    - 256 MiB SDRAM
    - 32 MiB SPI Flash
  - GR718B 18-port SpaceWire Router
  - Backplane I/F: 10x SpaceWire
  - Frontplane I/F and drivers:
    - SpFi (eSATA)
    - 2x SpaceWire
    - USB/FTDI UART/JTAG Links

Available in Q1 2020!
• GOMX-5 mission will consist of two 12U nano-satellites in the 20kg class with an improved platform for increased power handling and reliability.

• The purpose of the mission is to demonstrate new nanosatellite capabilities for the next generation of constellations requiring high speed communications links and high levels of maneuverability.

• The satellites will be equipped with advanced payloads which were announced in July 2019 to be:
  • Cobham Gaisler AB (SE) and LIRMM (FR) with powerful and radiation tolerant on-board computers

• Launch for the GOMX-5 mission is foreseen to be in 2021 which is subject to further ESA funding.
GR740 in Organic Package
Press release
Market transformation
GEO to LEO/MEO

- Change of Mission profiles
  - Traditional GEO market significantly declining
  - Fundamental shift to LEO & MEO including constellations
  - Shift away from GEO architectures and move towards smallsat-based systems
  - User need more diversified

- Unique environmental related space requirements
  - Radiation
  - Vacuum, microgravity and outgassing
  - No change

- Customer’s trade-off acknowledged;
  - SWaP
  - Performance
  - Cost
  - Lifetime
  - Time to market
  - Stock strategy
• Existing GR740 dice
  • Electrical performance and radiation characteristics already extensively validated

• Plastic Ball Grid Array (PBGA) package
  • 625 balls, having 1 mm solder ball pitch

• Evaluation, screening and qualification
  • Based on ECSS-Q-ST-60-13C for class 2 components

• Project kick-off in December 2019
  • Prototypes in August 2020
GR740 Software and Tools
GR740 software ecosystem

Operating systems
• BCC - Bare-metal environment
  • GCC/LLVM C11/C++11, Binutils, Newlib C
  • Open-source license
• Linux 4.9 (LTS/LTSI)
  • LEON build environment with buildroot
  • Toolchain with GCC, Binutils, GLIBC
  • LEON3/4 with GRLIB device drivers
  • Open-source license
• RCC - RTEMS-4.10, RTEMS-4.12, RTEMS-5
  • Prebuilt toolchain GCC, Binutils, Newlib C
  • Open-source license
• ThreadX
  • Small footprint thread handler
  • Commercial from Xpresslogic
• VxWorks
  • 6.9 and 7
  • GCC, Binutils toolchain. MMU protection.
  • Commercial from WindRiver

Simulators
• TSIM2 (single core)
• GRSIM (multi-core)
• TSIM3 (multi-core made right)

Hardware debuggers
• GRMON3
  • Tcl scripted command line interface
  • LEON2, LEON3, LEON4 based chips
  • JTAG, Ethernet, USB, UART, SpaceWire
  • GDB connection for C/C++-level dbg
  • GUI

Compiler Toolchains
• GCC
• LLVM

Boot loaders
• MKPROM
• GRBOOT (JUICE boot SW equivalent)
GRBOOT - Flight Software Boot Loader
ECSS and SAVOIR compliant

• Features
  • ESA “SAVOIR Flight Computer Initialisation Sequence” (SAVOIR-GS-002)
  • ECSS-E-ST-40C & ECSS-Q-ST-80C, criticality category B
  • Multi-processor support (SMP, AMP)
  • Initialization: CPU, FPU, caches, peripherals, etc.
  • System self-tests: CPU, L1/L2 caches, ROM, external memories, etc.
  • Self-test results are recorded in a Boot report, available to the loaded application
  • Separation of Boot Memory and Application Storage Memory:
    • Updating application does not require updating the boot loader
  • Application images can be stored in local non-volatile memory, including parallel memories & SPI Flash
  • ELF-like application image format with support for in-flight patching
  • Optional application compression
  • Application images are integrity checked before execution, with failover on failure
  • User extension points for custom initialization and user defined Standby Mode
  • Prepares environment compatible with multiple operating system:
    • RTEMS, VxWorks, Linux, BCC, SMP, AMP, etc.

• Portability
  • Currently GR740 and GR712RC devices are supported
  • Architecture allows additional systems to be added
  • Ports available for GR-CPCI-GR740 and GR712RC development boards
  • Boot memory options include parallel PROM, Flash and similar
  • Application images can be loaded from memory mapped memory or from SPI flash memory
  • Several main memory options are possible
TSIM3 LEON4 – GR740
Beta release for all current TSIM2 and GRSIM customers

- TSIM3 LEON4/GR740 beta release simulates:
  - **GR740** LEON4 quad-core device

- TSIM3 2019-Q4 release:
  - Focus on default configuration and basic timing, no fault-tolerance
  - LEON4 with 128-bit AMBA AHB CPU bus model
  - L2-cache model
    - 2MiB copy-back, LRU policy, MTRR regions
    - Register interface for emulated functionality
  - SDRAM model, fixed to 64-bit wide external memory bus, configurable frequency
  - I/O support, new models and existing adapted for GR740
    - 4xSpW AHB DMA, CAN, SPI, Ethernet, UART, GPIO, Timers, IRQCtrl, etc.
    - SpW router, 1553 and PCI not part of release

- TSIM3 2020-Q1 release:
  - Improved multi-core timing with AHB split modelled in L2-cache, AHB bus and LEON4
  - SDRAM model with 32-bit external data bus

- Road-map for TSIM3 during 2020 include:
  - More GR740 I/O models
  - Fault-tolerance modeling with error injection
  - Performance Optimization, AMP support, Library interface (automation now possible with Tcl)
Roadmap processor IP cores
Primary goals:
• SPARC V8 32-bit compliant processor core
• Improved performance over LEON4
• Superscalar – dual issue
• Goal is to have modes with deterministic, or bounded timing performance
• Reduction of configuration options
• Hardware support for virtualization
• SEU tolerance
• Leverage existing software support, maintain binary compatibility with LEON3 and LEON4

Primary feature set:
• SPARC V8e
• AHB and AXI4 bus support
• HW support for virtualization
• Local RAM (TCM)
• Copy-back cache (subject to performance evaluation in combination with multi-ported memory controllers with striped ports)
• Little endian support

Target technologies:
• ASIC implementations for space applications
• High-end space FPGAs: Kintex UltraSCALE

Target applications:
• General purpose payload processing
• Mixed platform and payload applications

Complemented by:
• New DDR2 and DDR3 SDRAM controller (FTADDR23), specifically targeted for space applications
• Multi-port L2 cache extensions allowing bandwidth extensions from L1 to off-chip memory devices
NOEL-V Processor Core
Release on 25 December 2019

Primary goals:
• RISC-V 64-bit compliant processor core
• **Superscalar – dual issue**
• Fault Tolerance - Error Correction Codes (ECC)
• **Cybersecurity** (proprietary solutions)
• Enabled for RTCA/DO-254 (Design Assurance Guidance for Airborne Electronic Hardware)
• Enable ISO 26262/FUSA certification (Road vehicles – Functional safety)
• **Leverage** foreseen uptake of **RISC-V software** and tool support in the commercial domain
• **Compatible with GRLIB IP Core library**

Primary feature set:
• **RISC-V RV64GC**
• AHB and AXI4 bus support

Supportive activities
• RISC-V Foundation Membership in 2019
• RISC-V PhD position at University of Delft with ESA

We have added RISC-V to our portfolio
Cobham Gaisler develops products based on the RISC-V ISA in parallel with the LEON SPARC processor line. The first RISC-V product is the NOEL-V RV64GC processor.
Roadmap processor components
GR7x5 – Octa-Core LEON5FT
Baseline specification – to be influenced by launch customers

Baseline specification

- Quad-core rad-tolerant SoC device
  - 8x LEON5FT with dedicated FPU and MMU
  - 128 KiB L1 caches connected to 128-bit bus
  - 2 MiB L2 cache, 256-bit cache line, 4-ways
  - DDR2/3 SDRAM memory I/F (+32 checkbits)
  - 8-port SpaceWire router with +4 internal ports
  - 32-bit 33 MHz PCI interface
  - 2x 10/100/1000 Mbit Ethernet
  - Debug links: Ethernet, JTAG, SpaceWire
  - 2x MIL-STD-1553B, 2x CAN-FD, 2 x UART
  - SPI master/slave, GPIO, Timers & Watchdog
  - I²C interface
  - NAND Flash controller interface
  - SpaceFibre & SRI0 x4+ lanes 6.25 Gbit/s
- LGA1752 package – ceramic and organic version
- No pin sharing
- 65nm/28nm technology
- Worst-case frequency of 350 MHz
- Target 9’000 DMIPS

Under consideration

- Architectural changes: Multi-layer connection to L2C with processors and IO on separate ports
- TM/TC functions on-chip
- Target technology change
- Extended support for HW-in-the-loop simulation
- Multi-core separation

Processing Solutions for Space

SPARC Compliant

LEON5
Baseline SoC specification

- Hexa-core radiation-tolerant SoC
  - 16x RISC-V RV64GC with dedicated FPU and MMU
  - Islands of 4 processors each with dedicated L2 cache
  - DDR2/3/4 SDRAM memory I/F (+32 checkbits)
  - SpaceFibre, PCIe, (SRIO TBD) eight lanes 6.25 Gbit/s
  - JESD204B/C support
  - 8-port SpaceWire router with +4 internal ports
  - 2x 10/100/1000 Mbit Ethernet (GMII, SGMII TBD)
  - 32-bit 33 MHz PCI interface (TBD)
  - MIL-STD-1553B, CAN-FD, 8 x UART with DMA
  - SPI master/slave, I2C master/slave
  - GPIO, Timers & Watchdog
  - CCSDS TM/TC functions on-chip
  - Debug links: Ethernet, JTAG, SpaceWire
  - NAND Flash controller interface
  - Interfaces for connecting COTS accelerators (MIPI?)
- Package – ceramic and organic versions
- 22/16/12/7nm technology
- Target 20'000 DMIPS
- Need to identify interfaces for leveraging COTS accelerators
- Increased focus on cyber-security and isolation (processor and SoC design features)
- Input on accelerators is welcome
- Input processing performance is welcome (int, fp, ..)

GR7xV – Deep-Submicron Hexa-Core RISC-V
Closer to COTS – make do with what technology exists now, optimize later
Welcome back in the next decade!