THALES ALENIA SPACE IN ITALY EXPERIENCE WITH GR740

GR740 USER DAY - ESA-ESTEC - 28TH NOV. 2019

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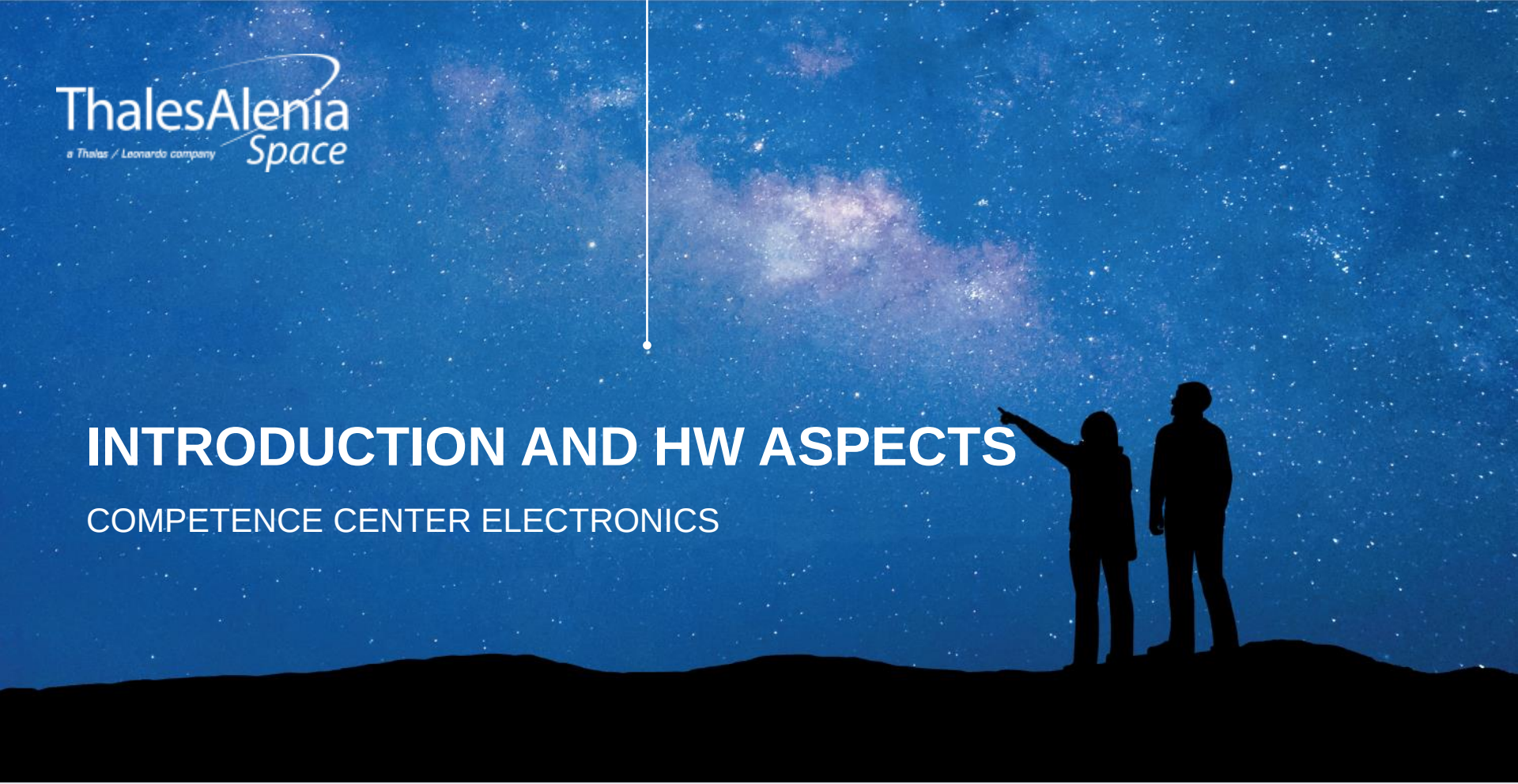

INTRODUCTION AND HW ASPECTS

COMPETENCE CENTER ELECTRONICS

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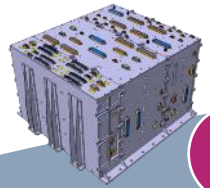
INTRODUCTION – WHY GR740 in the OBC Next Gen Roadmap?

/// Thales Alenia Space in Italy decided to adopt the NGMP as core of the Platform OBC Product since 2013

/// This was considered as the “natural” evolution in the Platform OBC roadmap based on ESA supported processors

2000
LEONARDO
SPARC-V7 ERC32 TSC-695F 20DMIPS
62 satellite in orbit
ESA programs: CryoSat-2, GOCE, SWARM, Sentinel-1A&B

2010
LEONARDO-3G
SPARC-V8 Leon3FT
EPICA-NEXT SoC 80DMIPS
75 satellite in orbit
ESA programs: Sentinel-1C&D



2018
IPAC
SPARC-V8 Quad-Core Leon4FT
GR740 SoC 1700 DMIPS
Including GNSS RX

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CRONOLOGY 1/3

/// In **2010** TAS-in-Italy started the **definition of a new generation of avionics computer** based on **multi-core processor** in the frame of Italian National programs and internal R&D, in order to **integrate several processing tasks** previously distributed among many computers around the satellite (e.g. Star Tracker processing, GNSS Navigation processing, AOCS Data Fusion) with **benefit in term of avionics platform competitiveness**

/// In **2013** the **ESA NGMP (Next Generation Microprocessor) has been selected by TAS-in-I as major building block for the new computer generation family**

/// May 2013: preliminary draft datasheet of LEON4-NGMP available

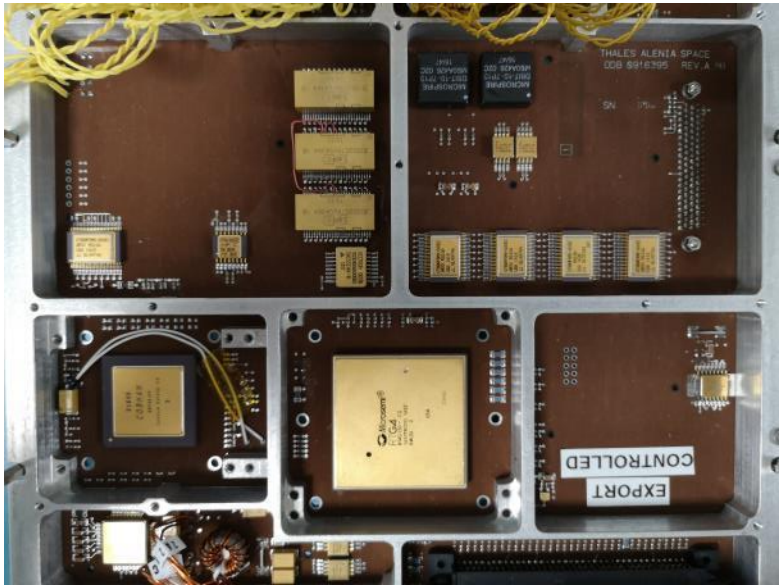
/// A trade off was activated in order to compare a solution based on the GR740 SoC from Cobham-Gaisler or on a custom FPGA solution based on use of NGMP IP Core. The final **solution based on GR740 was in the end selected mid 2016**, and detailed board design started.

/// Adopted board name is **Multi-Core Processor Module (MCPM)**

CRONOLOGY 2/3

///First MCPM based on GR740 has been designed by TAS-in-Italy Competence Center Electronics in **2016** targeted to Platform On-Board Computer with HIREL EEE components

///**TAS-in-Italy GR740 HI-REL board assembled and tested mid 2017**



CRONOLOGY 3/3

///A **new version “COTS” of the board has been developed in 2017/18**, targeted to low cost missions

///**TAS-in-Italy GR740 COTS board assembled and tested early 2018**

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MCPM BOARD CHARACTERISTICS

/// MCPM is targeted to Platform Avionics Computer functions. According to some limitations imposed by GR740 (not all the SoC functions can be used due to Pin Multiplexing), it has been necessary to help the SoC with an additional companion reprogrammable FPGA (allowing flexibility and configurability).

/// GR740 provided interfaces:

- 8 SPW links (from GR740 router to external users)
- 1 PCI (bridge to companion FPGA)
- 1 MIL-STD-1553B Bus
- 2 CAN Bus
- 2 UART
- JTAG, DSU SPW

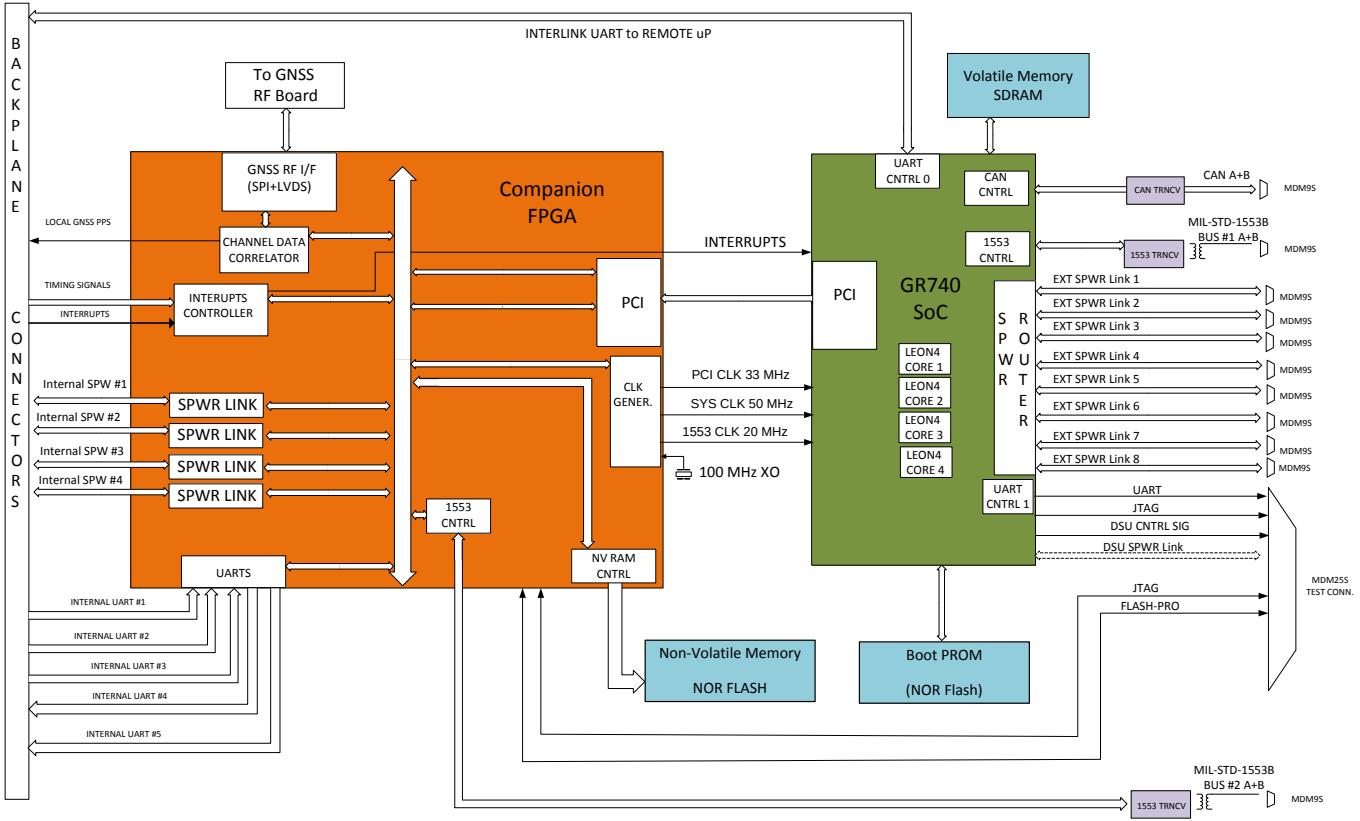
/// Companion FPGA provided Interfaces:

- Interface to non-volatile large memory (NOR FLASH)
- Clocks generation & Timings management
- GR740 reset and additional Interrupt Controller
- 4 SPW links (for high rate TM/TC/RM internal connection)
- 5 serial link (for low rate TM/TC/RM internal connection)
- Interface to GNSS RF and GNSS Receiver correlators
- Second MIL-STD-1553B Bus

/// MCPM implements following memory budget:

- 64kbyte Non-Volatile Boot Memory (maximum allowed due to GR740 Pin Multiplexing limitation)
- 32Mbyte Non-Volatile Memory (supported by Companion FPGA)
- 512Mbyte Volatile SDRAM (128MByte in COTS version)

MCPM BOARD BLOCK DIAGRAM



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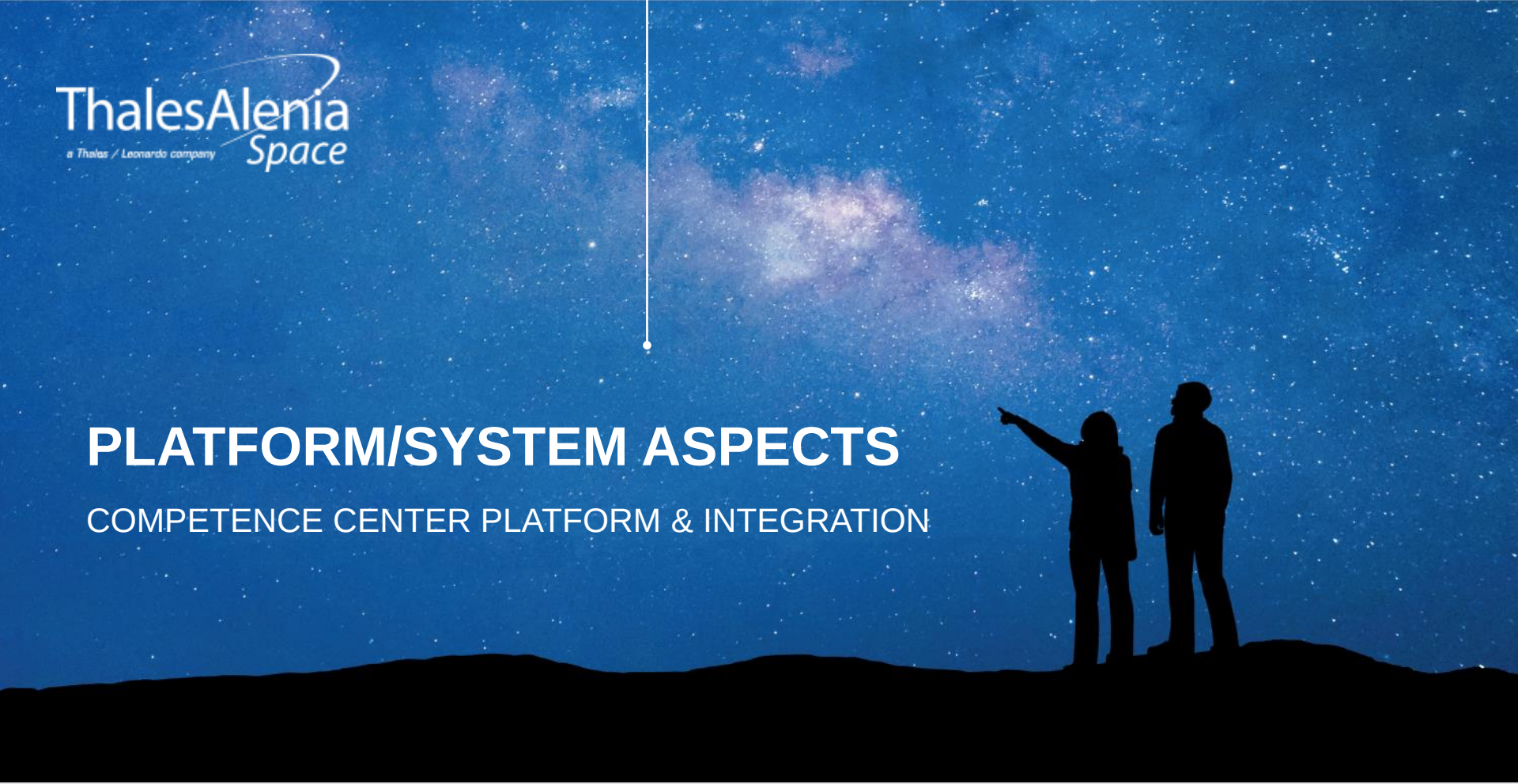


PLATFORM/SYSTEM ASPECTS

COMPETENCE CENTER PLATFORM & INTEGRATION

ROAD TO «MULTICORE SYSTEM»

EMC² - Embedded Multi-Core systems for Mixed Criticality applications (ARTEMIS Joint Undertaking project)

The **objective** of EMC² is to establish Multi-Core technology in all relevant Embedded Systems domains

2014 NGMP **2015** LEON4-N2X **2018** GR740

- Analysis and study of Multi-Core processors in the aerospace domain
- Benchmark activities

- First attempt to exploit para-virtualization on Cobham-Gaisler LEON4
- Tradeoff vs hypervisor on the market.

- Developing of flight software for an Institutional Italian Program

SPACECRAFT PLATFORM COMPUTER

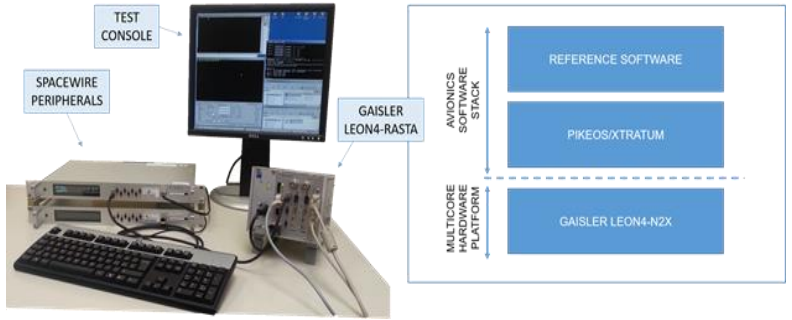
TAS-in-Italy has implemented a reference Spacecraft Platform based on a next-generation multicore processing architecture which supports Mixed Criticality applications.

OBJECTIVE

- To evaluate multi-core platform (Cobham Gaisler **LEON4**) for the aerospace domain
- To evaluate the virtualization-based software architectures (*SYSGO **PikeOS*** and *FentISS **XtratuM**)*
- To analyse the performance of the platform with respect to real world applications
- To evaluate the hypervisor capabilities in reusing legacy code (Star Tracker Software)

OVERVIEW

- The designed system aims to model:
  - The satellite's telecommand and telemetry function.
  - The management of peripheral devices.
  - The management of mixed-criticality application.



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KEY POINTS

Achievements

- Multicore processors (e.g. **LEON4**) provide better **cost** and **power dissipation** than single-core solutions of comparable computing power.
- The Hypervisor allows the development of **Time** and **Space Partitioning Systems** supporting mixed-criticality applications. (e.g. Symmetric Multi-Processing)
- The **latency** introduced by the hypervisor is minimal and it doesn't forbid the execution of Avionic Applications.
- The re-use of **Legacy Code** is fundamental feature of virtualization
- SYSGO **PikeOS** and FentISS **XtratuM** are interesting solution for the aerospace domain. Both hypervisors ensure time and space partitioning on multicore system with mixed criticality applications

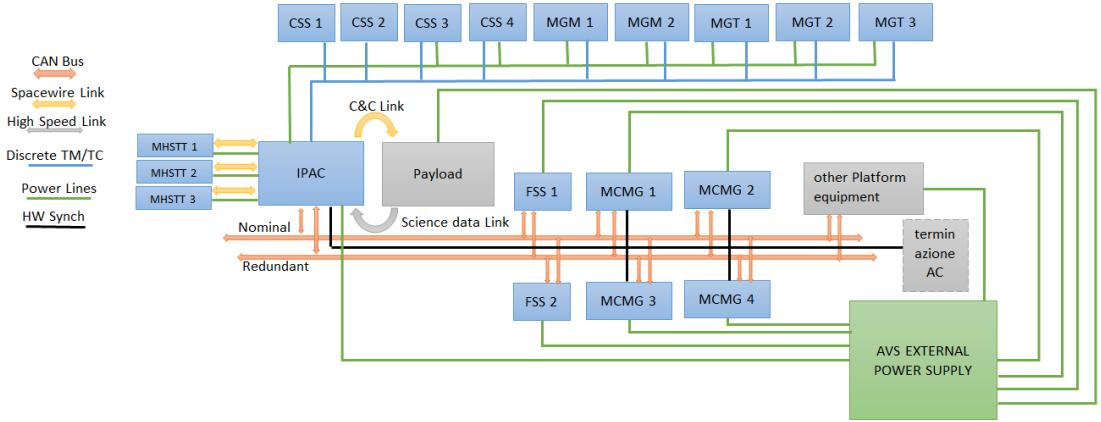
A little effort on…

- Improvement of predictability and determinism (Both are minor w.r.t. single core processor due to contention of shared resources)

NEW AVIONIC ARCHITECTURE: IPAC OVERVIEW

/// New Avionic architecture is based on new OBC: the **I**ntegrated **P**rocessing & **A**OCS **C**ontroller (**IPAC**)

- Enhanced compactness with respect to the actual OBC
- Processor capability up to 1700 DMIPS
- Flash memory capacity (for platform and payload data storage) up to 5 Tbit
- Reduced mass thanks to the fusion of many different functions in the same board



OBC

Mass: 18 Kg
Power: 53 W
Volume: 38 dm3

+

GNSS Receiver

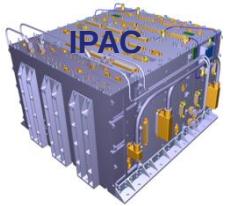
Mass: 3 Kg
Power: 15 W
Volume: 5.4 dm3

+

Payload Mass Memory

Mass: 27.6 Kg
Power: 160 W
Volume: 36 dm3

=



Mass: 16 Kg
Power: 95 W
Volume: 32 dm3

NEW AVIONIC ARCHITECTURE: IPAC EFFECT

- GNSS integration

OBC

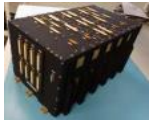
GNSS receiver

- PDHT integration

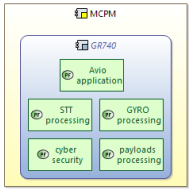
OBC

Payload Mass Memory

- STT processing integration



OBC



- Mass reduction
- Volume reduction
- Component reduction
- Cost reduction

SW ASPECTS

COMPETENCE CENTER SOFTWARE SOLUTIONS

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MIGRATION TOWARDS A MULTICORE ARCHITECTURE

- Integration of multiple SW on the same multi-core processor
  - Reduce HW bill of material and SW qualification effort, Increases SW complexity
- Need to manage different SW cat. level sharing the same resources
  - Needs to isolate failure of less critical SW to prevent error propagation
  - Time and space partitioning management

HYPERVISOR

- **An Hypervisor grants time and space partitioning**
  - At the start of our activity none hypervisor is qualified for GR740
  - Open contact with vendor
- Currently we are using XtratuM by FentISS
  - None formal qualification but grants compatibility for GR740
  - Just qualified under ESA contract on LEON 3. Probably it will be in 2020 for multicore in GR740
  - We have performed an internal validation campaign for XM4 on GR740.

SW DEVELOPMENT FOR GR740 BASED ON BOARD COMPUTER

- **SW Development for OnBoard Computer**
  - Dedicated HW aspect can’t be managed until OBC availability
  - The use of a GR740 development board can’t be enough for some aspect

FULL SW SIMULATOR

- **A completely SW simulator permits to develop SW without HW availability**
  - GR740 emulator are currently in beta version
  - Open contact with vendor
- At this time there isn’t a GR740 emulator

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RETURN OF EXPERIENCE

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POSITIVE FEEDBACK

- Map of memory suitable for SW implementations
  - all registers of each function are grouped to a block aligned to 4KB. This allow an easy segregation of memory using MMU (that works on a minimum amount of memory (page) that is exactly 4KB)
- Cache system with the L2
- Controllers of peripherals
  - suitable in exchange data, using DMA bursts to access SDRAM. Improvement of functionality (for example the CAN controller, with its buffering potentiality, is better respect the one on UT699)
- Powerful HW utility
  - one for all, scrubbing of SDRAM
- IOMMU also allows spatial segregation also in presence of DMA peripherals.

IMPROVEMENTS AREAS AND SUGGESTIONS 1/2

- Multiplexing of signals
  - The PROM lines are multiplexed with standard avionics resources such CAN, MIL-STD-1553, UART → this penalized specifically the Platform Computer application scenario where large Non-Volatile memory and standard avionics interfaces are requested at the same time. This imposes additional companion FPGA.
  - multiplexing of interrupt inputs

- Only one MIL-STD1553B bus
  - Many applications (also several ESA missions) require the presence of two MIL-BUS-1553 busses

- SDRAM Controller
  - SDRAM are obsolete → difficult to guarantee manufacturability of equipment based on GR740 for more than 5/6 years and imposes the maintenance of compatible SDRAM part stock

IMPROVEMENTS AREAS AND SUGGESTIONS 2/2

- Interrupt controller
  - most of the interrupt of first level are dedicated to timers.
  - Only one interrupt is the collector of other 16 interrupts coming from peripheral.
  - No «first level» interrupt for external signal GPIO (the only GPIO are «second level» interrupt but anyway multiplexed).
  - 4 «first level» interrupt unassigned.

  This create a «bottle neck» for redistribute interrupt toward different applications.
- PCI DMA engine
  - only 1 PCI DMA engine present (GRPCI2) → One per core could be a better solution to extend the potentiality of this bus to all applications running on different cores