Data Device Corporation

SCS3740™ 3U SpaceVPX Single Board Computer using GR740 Processor

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GR740 Users Day, November 28, 2019

DDC™ Connectivity Power Control

SCS3740™ Overview

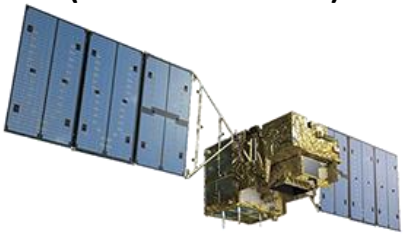
- **DDC's latest SCS (Supercomputer for Space): SCS3740**
  - **Based on Cobham Gaisler GR740 Quad-Core Processor**
  - **Standard Single Board Computer (SBC) Product**
  - **3U SpaceVPX form factor**
    - Optimized for size, weight, power, radiation and cost
  - **Flight boards with all ceramic/hermetic components**
    - Screening levels up to EEE-INST-002 Level 1
  - **Available now with full Development Kit**
  - **Board level Board Support Package (BSP) for VxWorks 7**
  - **Datalight high reliability Flash File system integrated**

Accelerates System Development!

SCS750 Flight Heritage

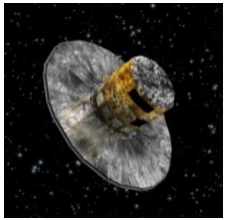
SCS750 shipping since 2005

SCS750s on GOSAT on key environmental sensor (launch: Oct. 2018)

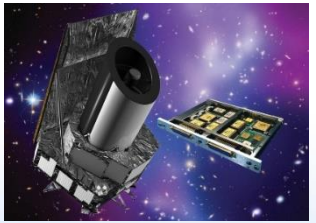


SCS750s on NRL RSGS Robotic Servicing of Geosynchronous Satellites

SCS750s on ESA Gaia spacecraft (launch: 2013)



SCS750s on 2 Instruments on EUCLID



SCS3740 – SWAP Optimized

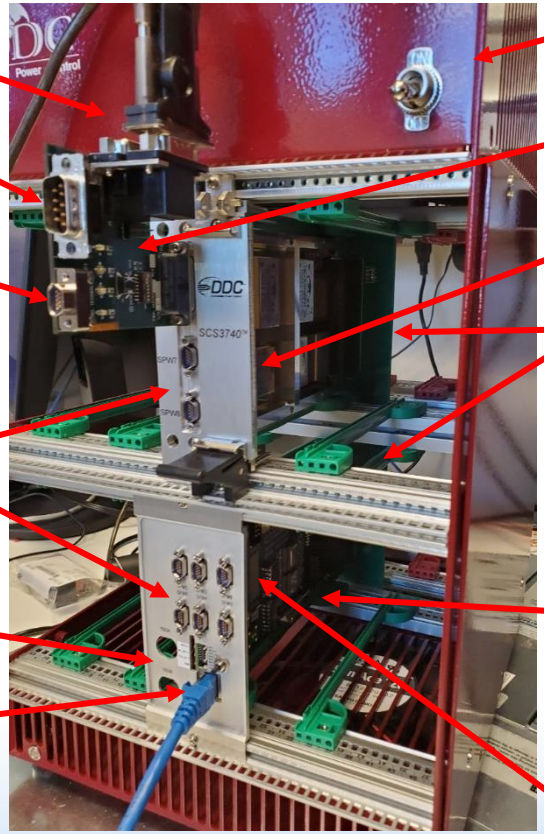
SCS750®

SCS3740™

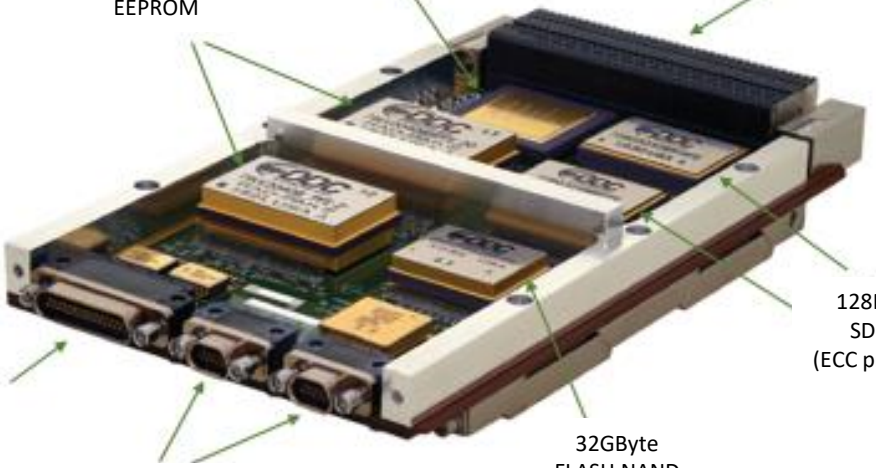
Category	SCS750	SCS3740
Form Factor	6U	3U
Backplane	cPCI	SpaceVPX
Processor	PowerPC 750FX	GR740 Quad Core
Processor Mitigation	SOI, TMR	Rad Hard ASIC
GEO Error Rate	1 in 80 years	1 in 150 years
MIPS Rating	1800	1700
Power (Watts)	18 to 35	4 to 10
SDRAM	256 MB	128 MB
FLASH	64 GB	32 GB
SPW Ports	4	8
TRL Level	9	Qual Q4/2020

SCS3740: Excellent addition to DDC Family

Lab Development Support – SCS3740 Dev Kit



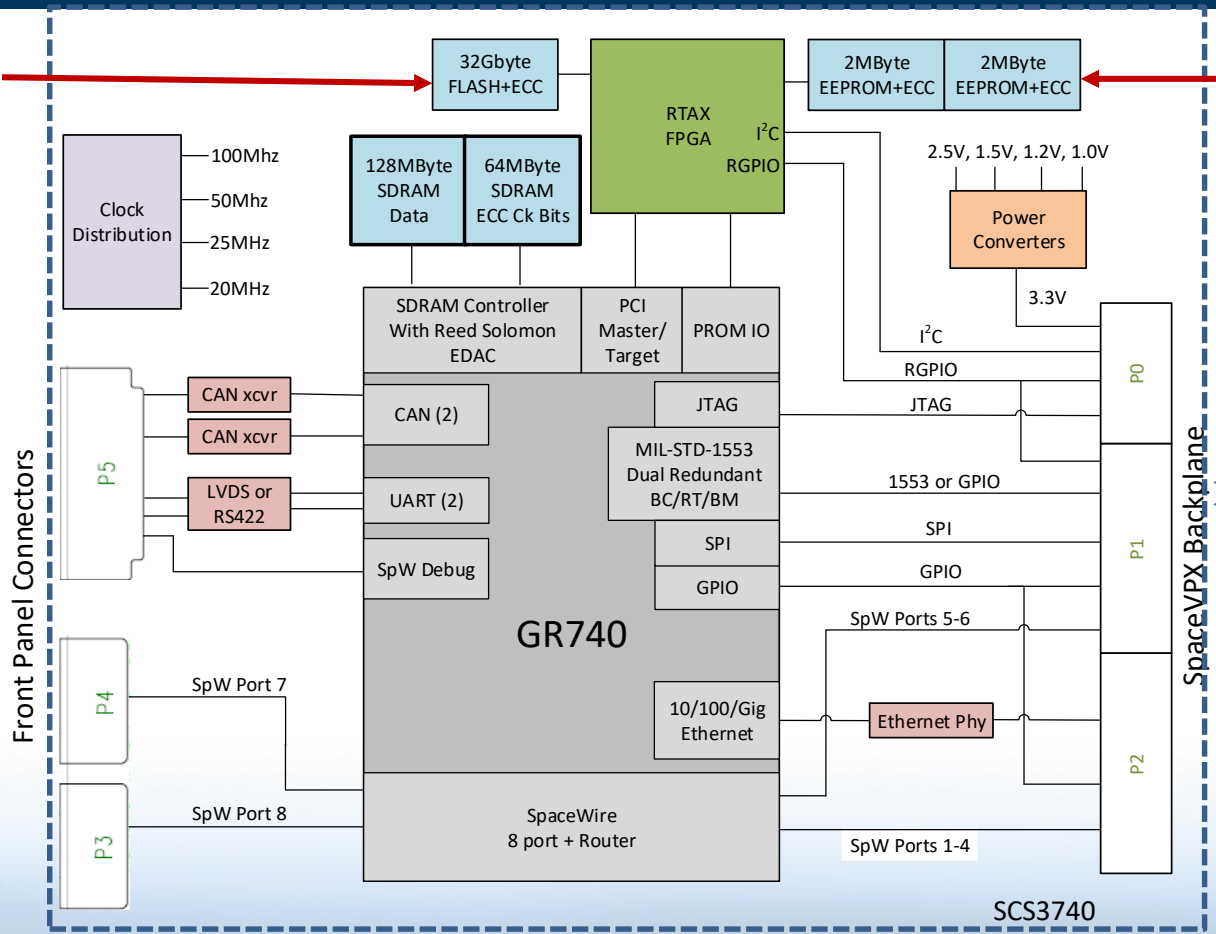
SCS3740 Architectural Overview



SCS3740 Block Diagram

FLASH
File System
OS Images

SuROM -2 Images
Primary/Secondary
Auto-Swap



External 1553
XCVR/XFMR

Best in-class TID Performance with Patented Rad-Pak® Technology

GR740 Design Challenges – 1 of 2

- **GR740 PCI - No PCI arbiter. Does not meet PCI timing specs.**
- **GR740 to FPGA Interface/Expansion Options**
  - **SpaceWire – Lose some generic SPW ports for application. Wanted to keep all 8 ports.**
  - **Enable PCI bus - Pin Sharing Challenges reduce SDRAM data width.**
- **SDRAM Clock Rate**
  - **Unable to run at 100MHz SDRAM due to GR740 timing specs under worst-case analysis.**

GR740 Design Challenges – 2 of 2

- **Signal Integrity**
  - **Overshoot/undershoot specs are very tight for PCI and SDRAM.**
  - **This affects DC input voltage Vmax.**
- **SpaceWire Data Rate**
  - **WCA at system level will typically be ~ 200Mbps. 300Mbps is possible on-board.**
- **PROM I/O Interface**
  - **Difficult to boot from when interfacing through FPGA and Handshaking.**

SI Overshoot/Undershoot

PCI and SDRAM overshoot/undershoot:

- **+/-300mV overshoot/undershoot standard DC voltage <=3.6V**
- **+/-500mV overshoot/undershoot if DC voltage <= 3.4V**
- **Investigating options to meet 300mV SI on GR740**

Difficult for system level power supply to be <=3.4V

SDRAM Timing – From GR740 Datasheet

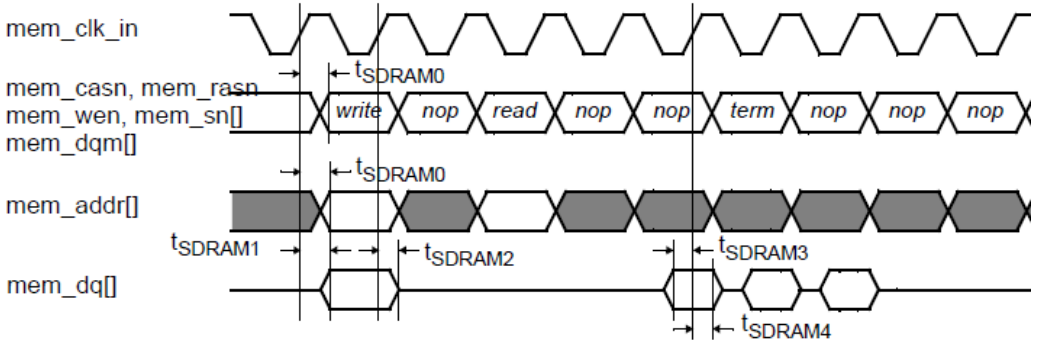


Figure 60. Timing waveforms - SDRAM accesses

Table 581. Timing parameters - SDRAM accesses

Name	Parameter	Reference edge	Min	Max	Unit
t_{SDRAM0}	clock to output delay	rising mem_clk_in edge	2.5	12.0	ns

SDRAM interface is not capable of running at 100MHz with worst-case analysis, even if 2T Timing and Double chip select mode are enabled.

SpaceWire Maximum Bitrate

From ECSS-E-ST-50-12C Rev 1 (Example):

Table 5-10 Example calculation of maximum bit rate

Factor	Abbreviation	Value (ps)	Sum (ps)
Maximum, worst case, source unit output D-S skew	$DSskew_{OUT}$	1234	1234
Maximum, worst case, cable assembly differential D-S skew (e.g. 5 m cable)	$DSskew_{CA}$	500	1734
Maximum, worst case, data or strobe jitter in the cable assembly	$Jitter_{CA}$	500	2234
Receiving unit minimum tolerated separation between signal edges	$Minsep_{IN}$	1384	3618
10% Margin	Margin	362	3980
Minimum Bit Unit Interval	T_{UIMIN}		3980
Maximum bit rate			251 Mbps

From GR740-UM-DS-2-3

Table 586. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPW0}	transmit clock period	-	see Table 578		
t_{SPW1}	clock to output delay	-	-	-	not applicable
t_{SPW2}	input to clock hold	-	-	-	not applicable
t_{SPW3}	input to clock setup	-	-	-	not applicable
t_{SPW4}	output data bit period	-	2.5 [2]	-	ns
t_{SPW5}	input data bit period	-	2.5 [2]	-	ns
t_{SPW6}	data & strobe input edge separation	-	2.5 [2] [3]	-	ns
t_{SPW7}	data & strobe output skew	-	-0.3 [3]	0.3 [3]	ns

[1] Internal SpaceWire clock generated from PLL or from spw_clkin.

[2] Assuming SpaceWire PLL used in nominal configuration

[3] Edge separation and skew limits refer to each pair of data/strobe signals separately. Global skew and separation over the entire set of eight pairs is not specified.

SCS3740 Max Bit rate example

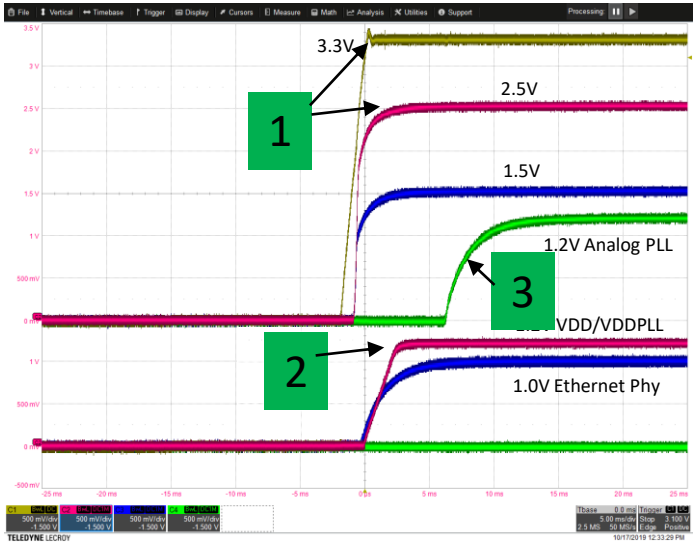
Factor	Value	Sum	units
Maximum worst case source unit output D-S skew	300	300	
Maximum worst case cable assembly differential D-S skew	500	800	
max worst case data or strobe jitter in the cable assembly	500	1300	
receiving unit minimum tolerated separation between signal edges	2500	3800	
Margin	380	4180	
Minimum bit Unit Interval		4180	
Maximum bit rate		239	Mbps

SCS3740 WCA can support systems with SPW at 200-250Mbps.

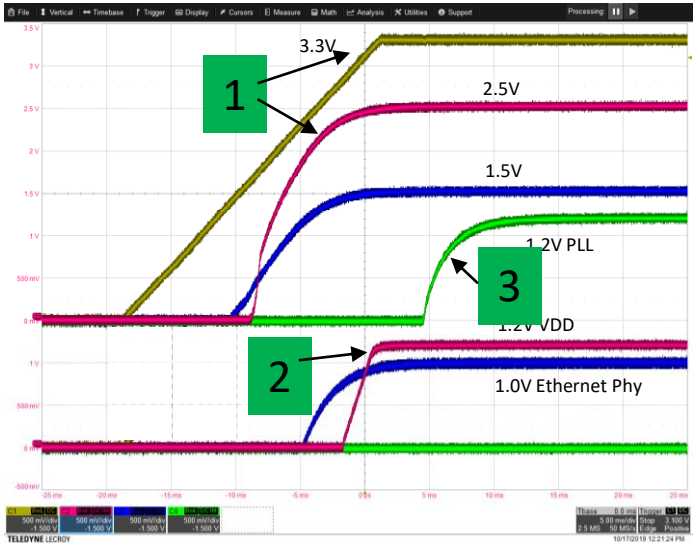
Higher bit rates may be possible, depending on system level budget.

Example Design Verification Test – Power Sequencing

2ms 3.3V power on



20ms 3.3V power on



1. 3.3V and 2.5V Power up First
2. 1.2V VDD/VDDPLL Power up
3. 1.2V Analog PLL

Example Design Verification Testing of SCS3740/GR740 Power Sequence. Power up at 2ms and 20ms meets all power sequencing requirements.

Future Interests

- **Processor – higher performance (MIPS)**
- **Memory**
  - **SDRAM – upgrade to DDR2/3/4**
    - Supporting higher performance and higher density
  - **Built in FLASH controller with advanced ECC (BCH/LDPC)**
- **Interfaces**
  - **SRIO interfaces with switch**
  - **Expansion port for on-board communication (Gigabit+)**
  - **Higher speed SpaceWire**

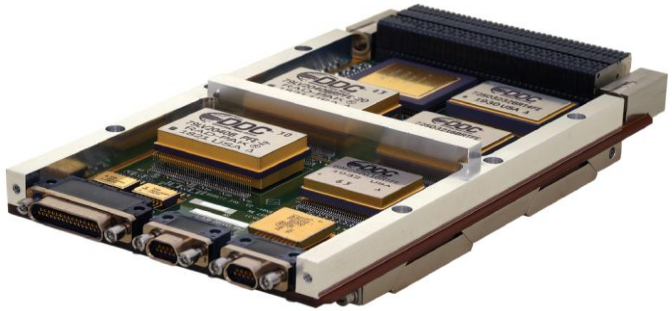
SCS3740 Availability

Ordering Options:

- **SCS3740DK6-CBUF - Development Chassis with power, User Test Board & Front Panel Test Board**
- **SCS3740RSE/LVE "E"- Engineering Model (EM) level components, Room Temp Tested**
- **SCS3740RSA/LVA "A" - Components screened to DDC Class A flow**
- **SCS3740RSB/LVB "B" - Components screened to 883 Class B or equivalent**
- **SCS3740RSS/LVS "S" - Components screened to Class S or equivalent**

Schedule:

- **Engineering Model: Now**
- **Development Kit: Now**
- **Flight: Q4 2020**



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