GR740 User Day

From concept to product

NGMP to GR740

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ESA/ESTEC
TEC-EDM
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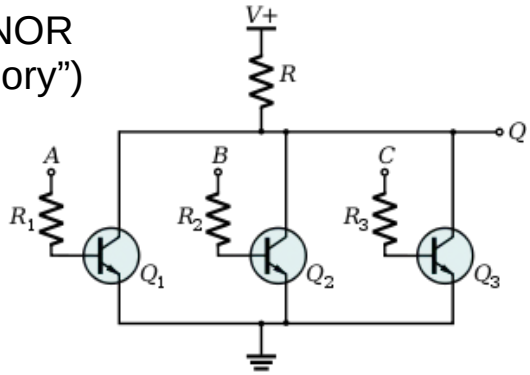
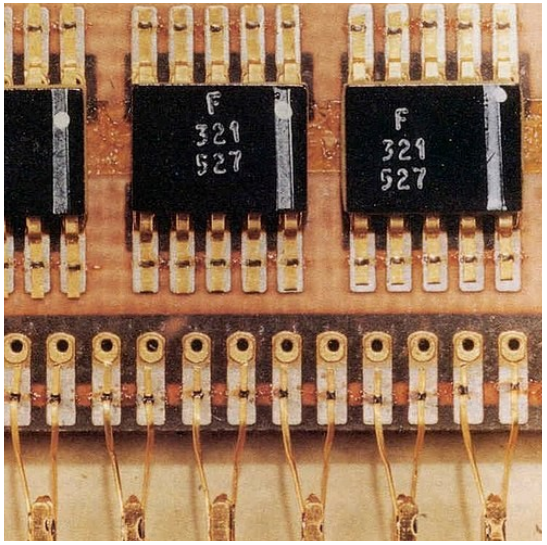
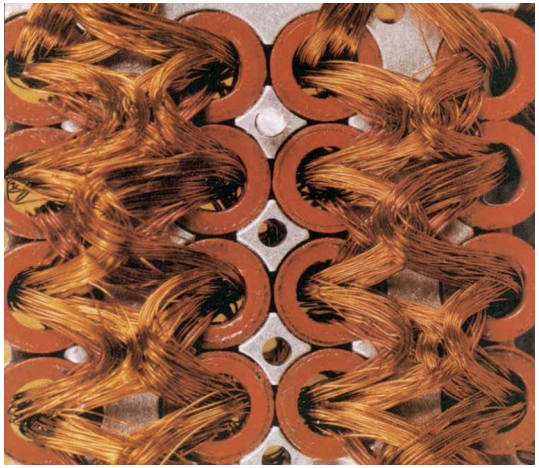
History: Apollo Guidance Computer (AGC)

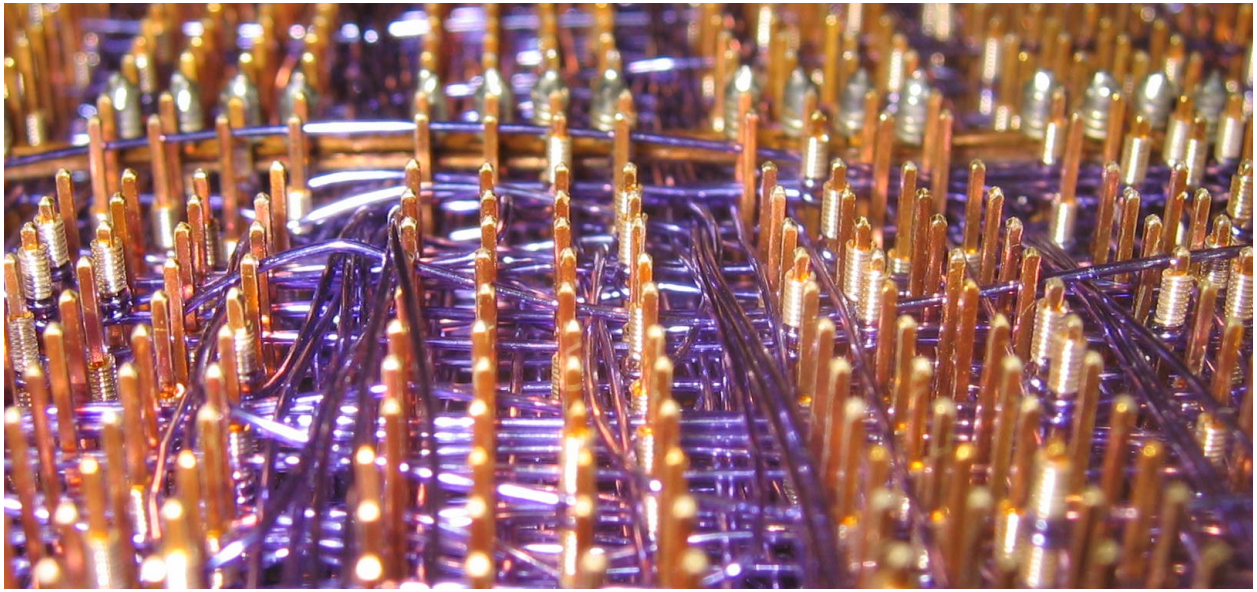
Development ~1961 - 1969

- 2800 Micrologic IC's = 5600 3-input NOR
- 4 KiB RAM, 72 KiB ROM ("rope memory")
- 15-bit word-length (1's complement)
- Proprietary instruction set
- Wire-wrap interconnect
- 2 MHz clock, 11.7 µs memory cycle
- 30l volume (1ft³), 31kg (70lb), 55W





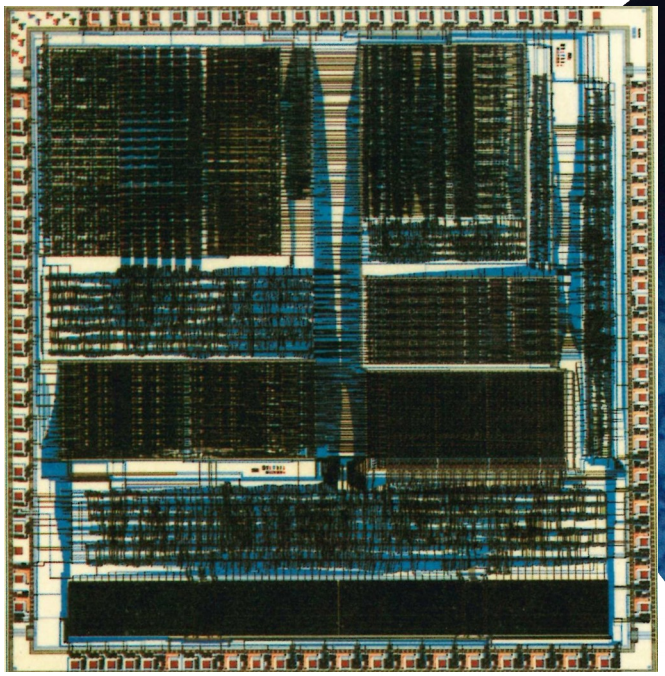


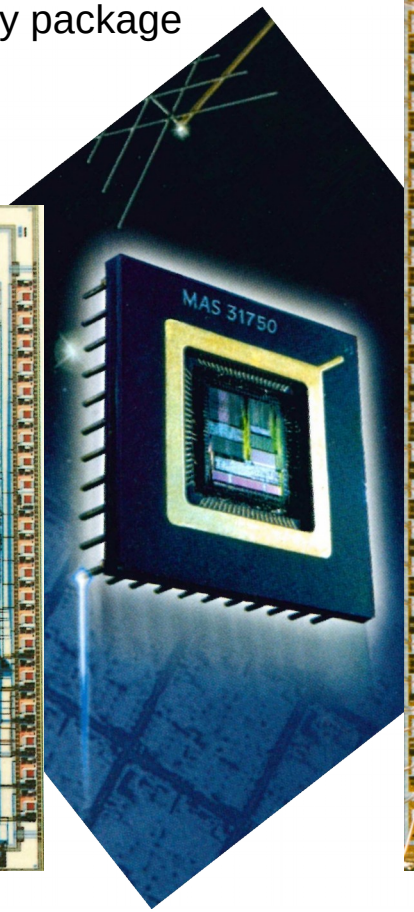


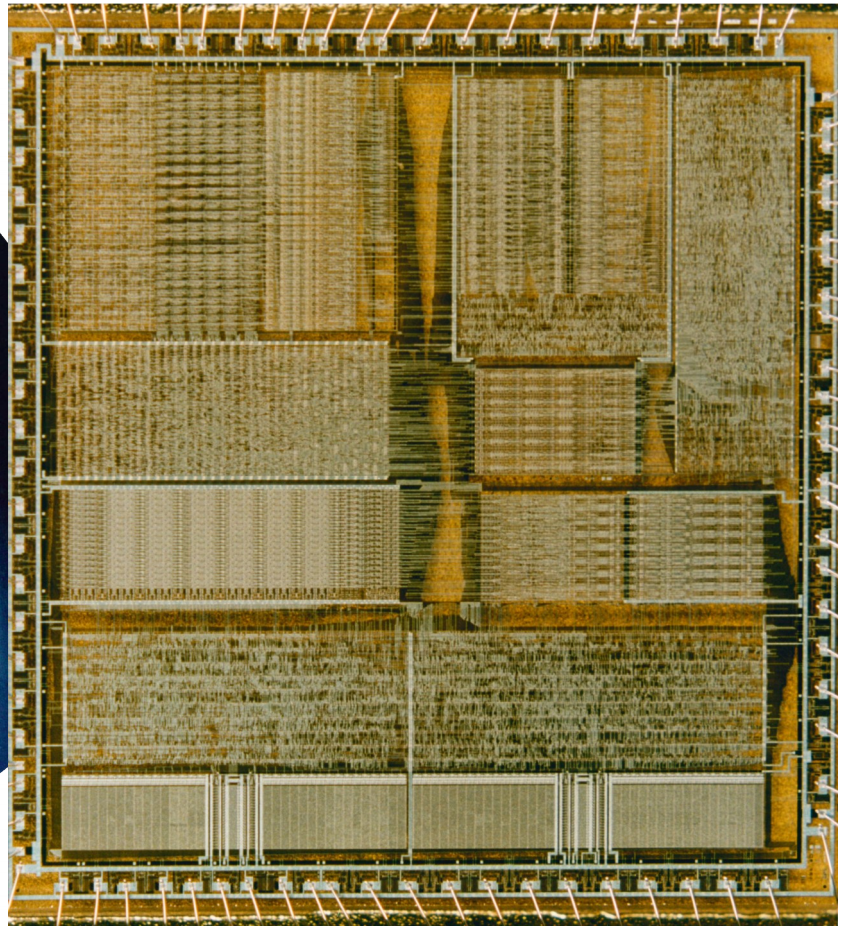
History: Dynex MA31750

First ESA space microprocessor (beg. 90's)

- 1.25 µm CMOS MEDL/GEC-Plessey/Mitel/Dynex
- SOS (Silicon-On-Saphire) = rad-hard by process
- 84-pin flat-pack / pin-grid array package
- 16-bit MIL-STD-1750 CISC
- 2 chip-set (CPU/MMU)
- 16 MHz / 2 MIPS







History: ERC32 Chip-Set

First ESA SPARC microprocessor (1991 - 1997, obsolete 2002)

- **32**-bit **E**mbedded **R**eal-time **C**omputing core
- Commercial IP-core, basic SEU protection: parity on all registers
- 0.8 µm CMOS Temic/Atmel fab (now Microchip)
- Used on DMS-R (Zvezda module of ISS)
- 256-pin quad-flat-pack (MQFP) package
- 3 chip-set (CPU/FPU/MEC)
- 32-bit SPARC-V7 RISC
- 14 MHz / 10 MIPS

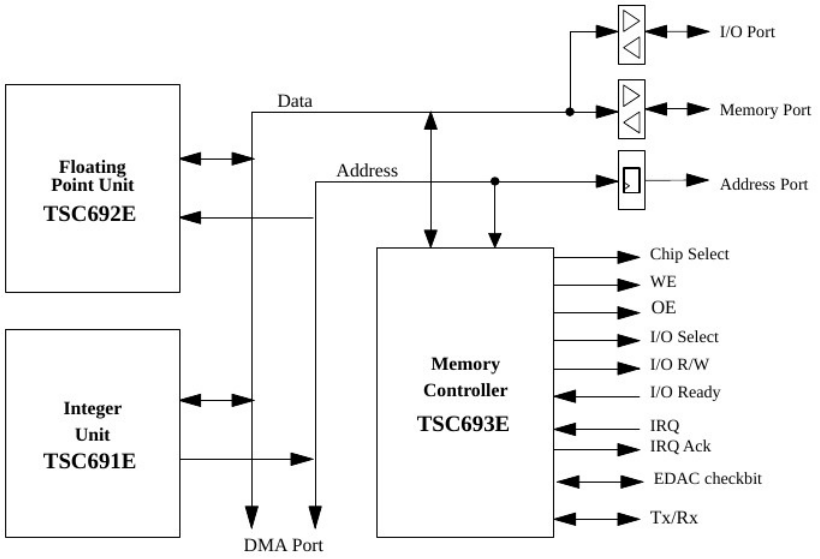
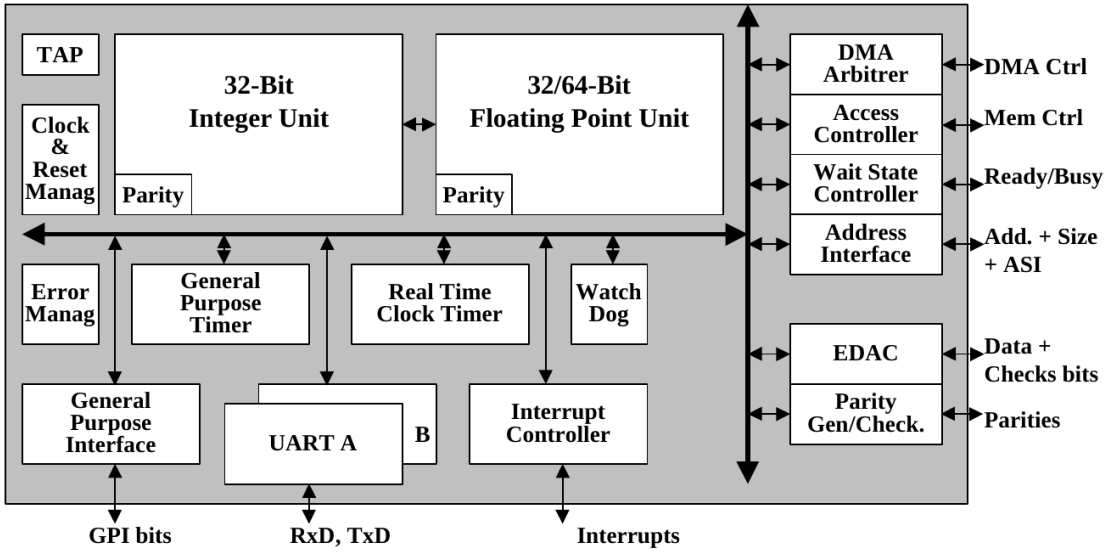


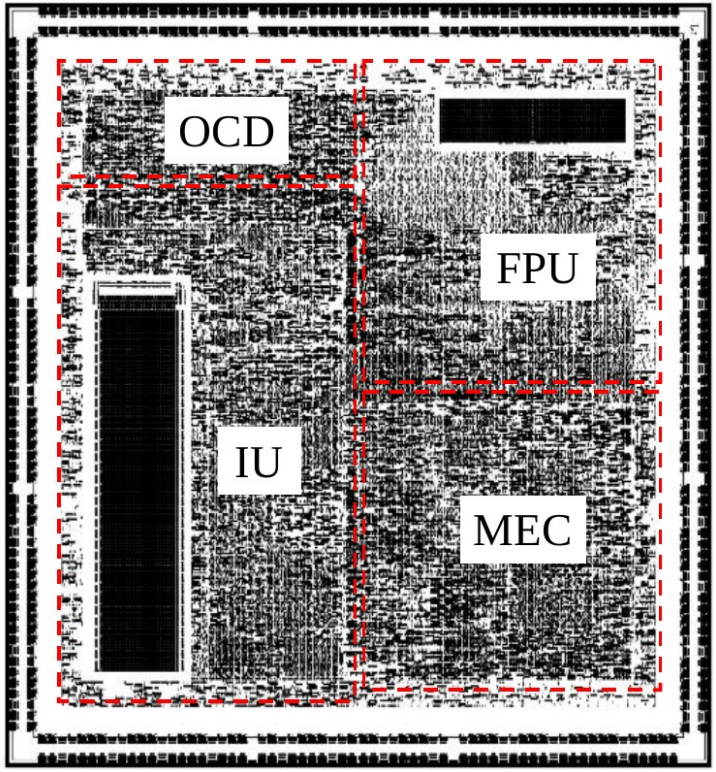
Figure 1. ERC32 Architecture

History: ERC32 Single Chip

Second generation ESA SPARC microprocessor (end 90's, still on Microchip catalog)

- 0.5 µm CMOS Temic/Atmel fab (now Microchip)
- Shrink: same design and IP as ERC32 chip-set, but now in one chip
- Extended SEU protection, parity + hardened flip-flops (HDFF)
- Widely used across many ESA projects Ariane 5 IMU, GOCE, AEOLUS, CRYOSAT...
- 256-pin quad-flat-pack (MQFP) package
- 32-bit SPARC-V7 RISC
- 25 MHz / 20 MIPS

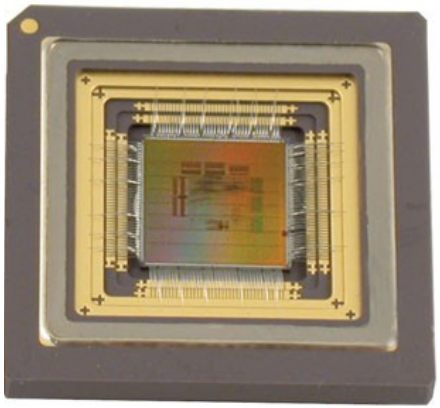


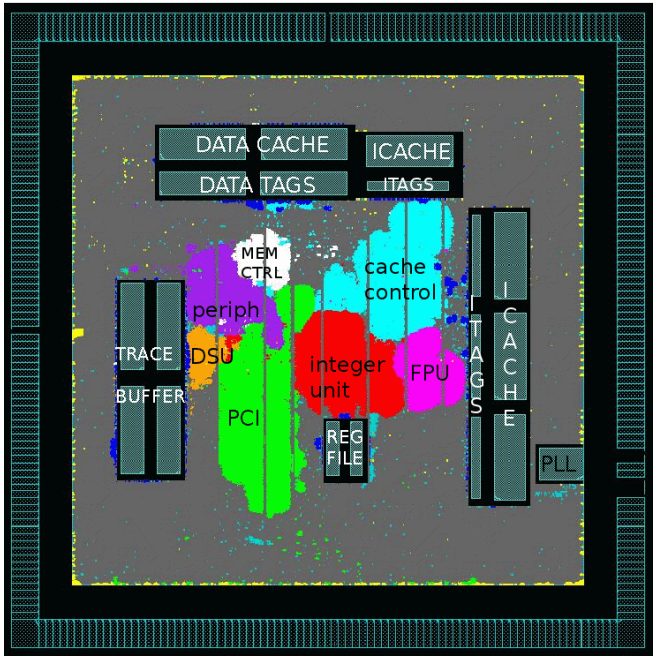


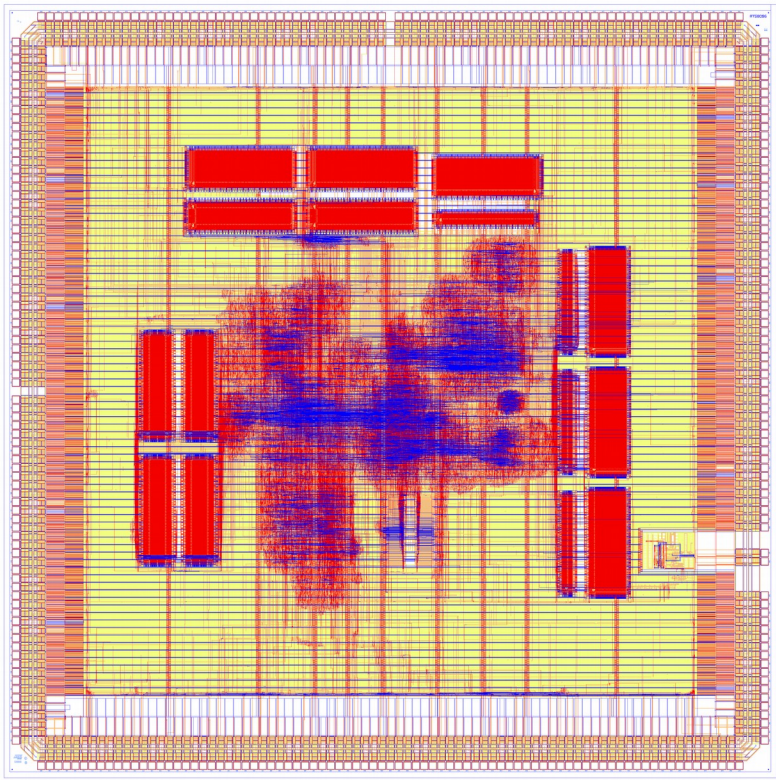
History: AT697E / AT697F LEON2-FT based

First generation ESA LEON-SPARC microprocessor (on Microchip catalog)

- 0.18 µm CMOS Temic/Atmel fab, later ported to UMC fab
- Based on ESA LEON2-FT IP core, SRAM/SDRAM port, PCI 2.3 interface
- SEU protection: cache parity, reg-file EDAC, TMR flip-flops + skewed clocks, *no HDFF*
- First launches: Airbus Ernobox on ISS (March 2008), PROBA-2 OBC (Nov. 2009)
- MCGA/LGA 349 and 256-pin MQFP package
- 32-bit SPARC-V8 RISC, 100 MHz / 86 (D)MIPS







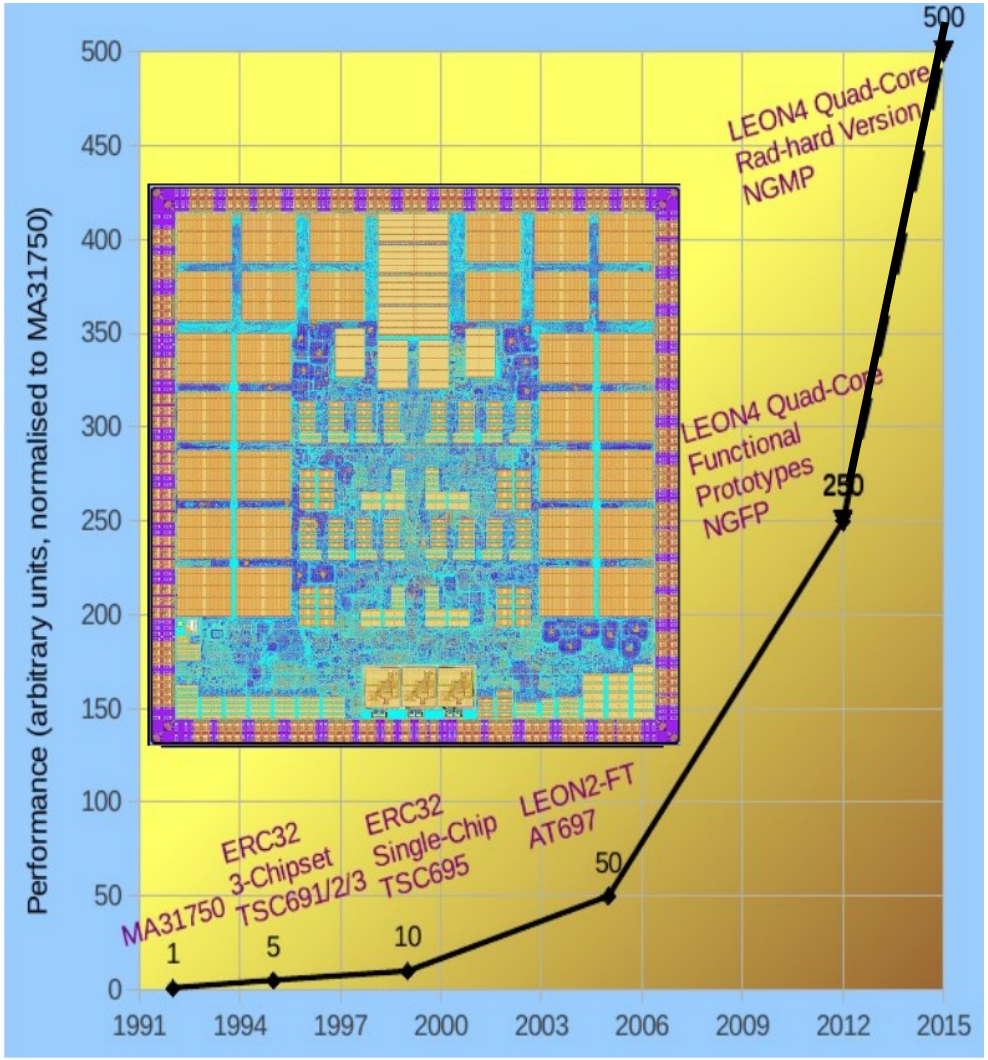
NGMP / GR740: Objectives

The NGMP Programme

- = Next Generation Multi-Purpose (µP)
- = Next Generation Micro-Processor
- = Next Generation Multi-core Processor
- Initiated by ESA (A. Pouponnot) ~ 2006
  - while MA31750 was (still) used
  - while ERC32 was heavily used
  - while AT697 was still to be qualified

NGMP Objectives:

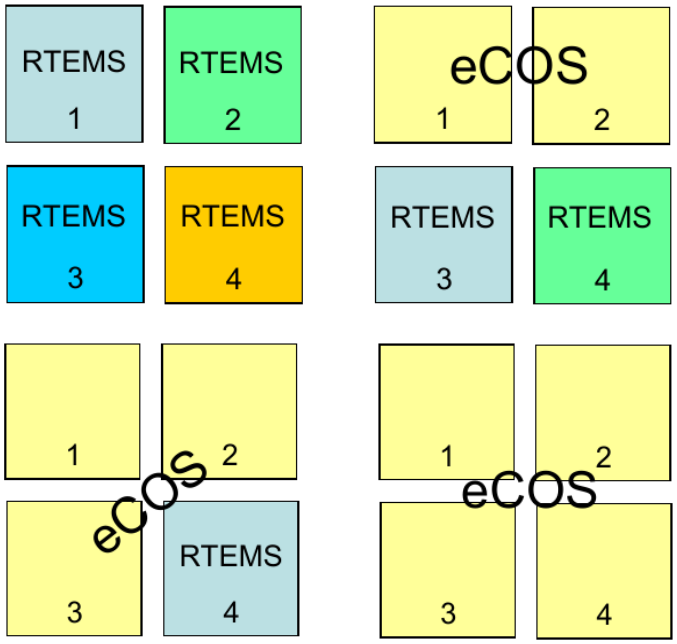
- **Multi-Core SPARC**
  Round-table 2006: consensus with industry
- **10x performance increase**
  compared to previous generation AT697
- **Define, develop, manufacture, validate**
  in advanced (deep-sub-micron) technology
- **Commercially available to all users**
  in ESA member states (and world-wide)
  = off-the-shelf standard component
  = technical support
- **Space qualified**
  QML-V, ESCC-9000



NGMP Phase 0: GINA

Phase 0: GINA (Giga-Instruction New Architecture)

- 2006, multi-core study, LEON3-FT quad-core system, FPGA demonstrator (Virtex4-LX200)
- 2-bus system (CPU/peripheral bus) – bottleneck in the 32-bit CPU bus
- Virtex4, high utilisation, FPGA tool issues: 40 MHz (4-cores) / 80 MHz (1-core)
- Estimate: 266 MHz (90 nm techn)
- ASMP operation: 4 x RTEMS
- SMP operation: eCOS only
- Mixed mode configurations



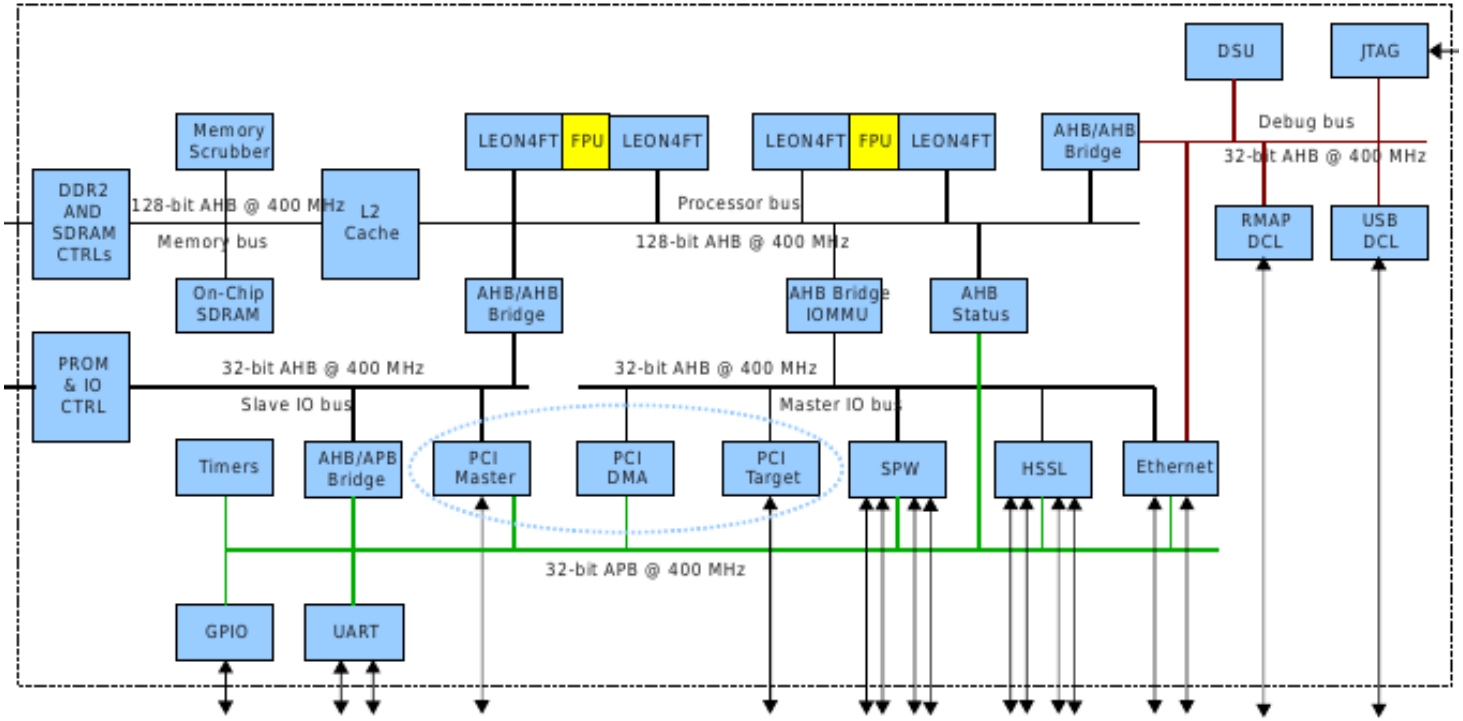
NGMP Phase 1: SRR / PDR / N2X-Prototype

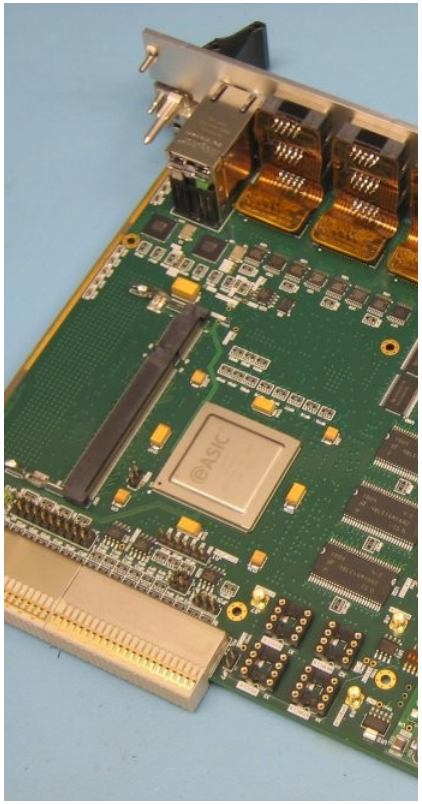
Phase 1: Definition and Architectural Design of Multi-core SPARC NGMP

- Competitive ITT in 2008 won by (Aeroflex) Gaisler, contract signed 2009
- Mandatory use of ST 65 nm space platform (under ESA development), LEON not mandatory
- Spec published in 2010: LEON4, L2-Cache, 128-bit CPU bus, DDR2, Serdes, debug and 2 I/O busses
- FPGA demonstrator boards released to users in 2010

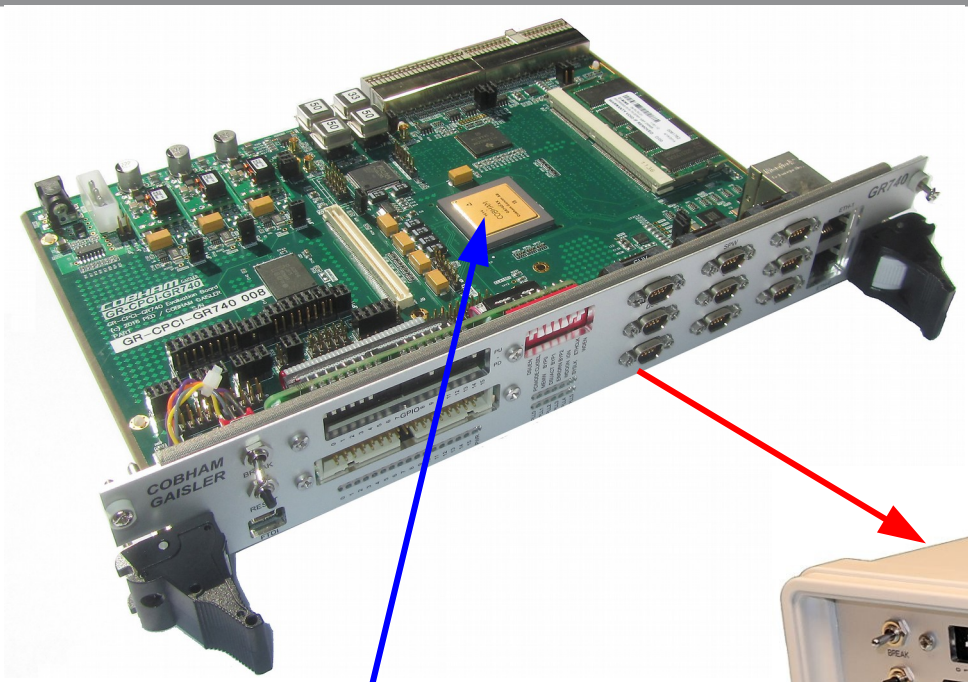
On-hold for 3 years (waiting for ST 65nm readiness and access)

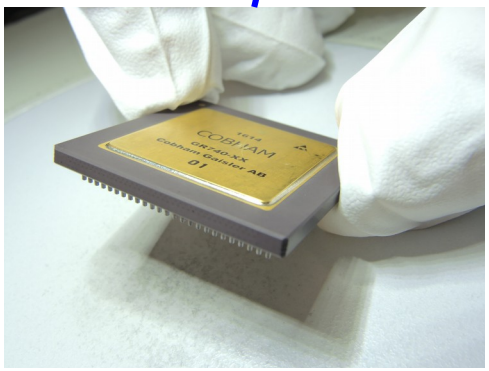
- LEON4-N2X: prototypes in commercial eASIC in 2013





NGMP Phase 2: GR740 Prototypes

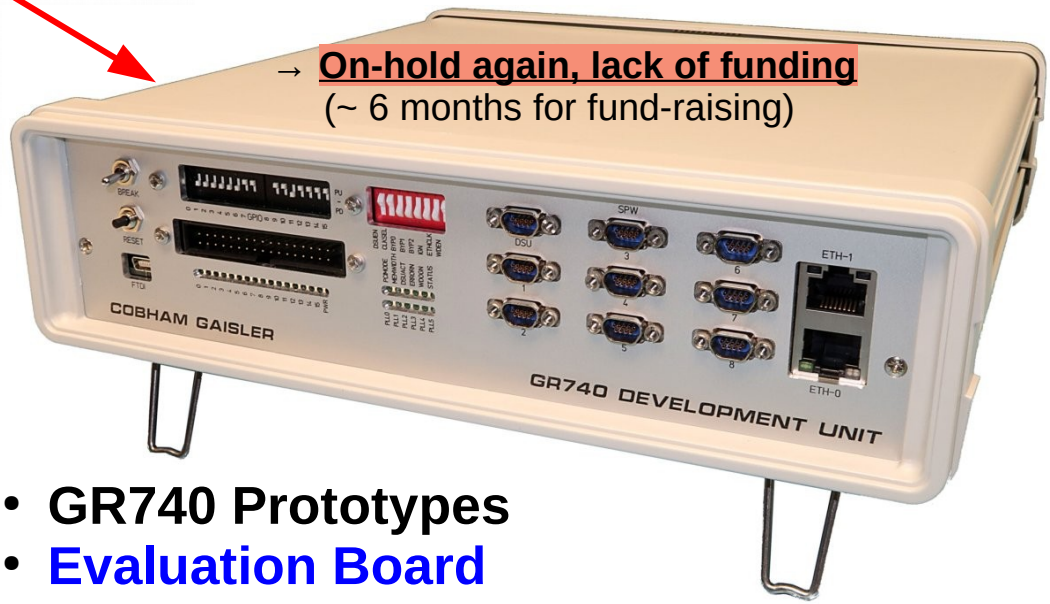




Phase 2: GR740 Prototypes (resumed 2014)

- Added split-support to L2-cache, SPW router
- DDR2 SDRAM removed (no IO's / PHY)
- Flip-chip was high risk, use wire-bond instead
- → SERDES removed (IP for flip-chip only)
- Sign-off, ready for ST fab: June 2015
- First Prototypes delivered by ST in Jan. 2016
- Functional validation + radiation testing
- Evaluation board released (June 2016)
- EM and boards out of stock in autumn 2016

→ **On-hold again, lack of funding**
(~ 6 months for fund-raising)

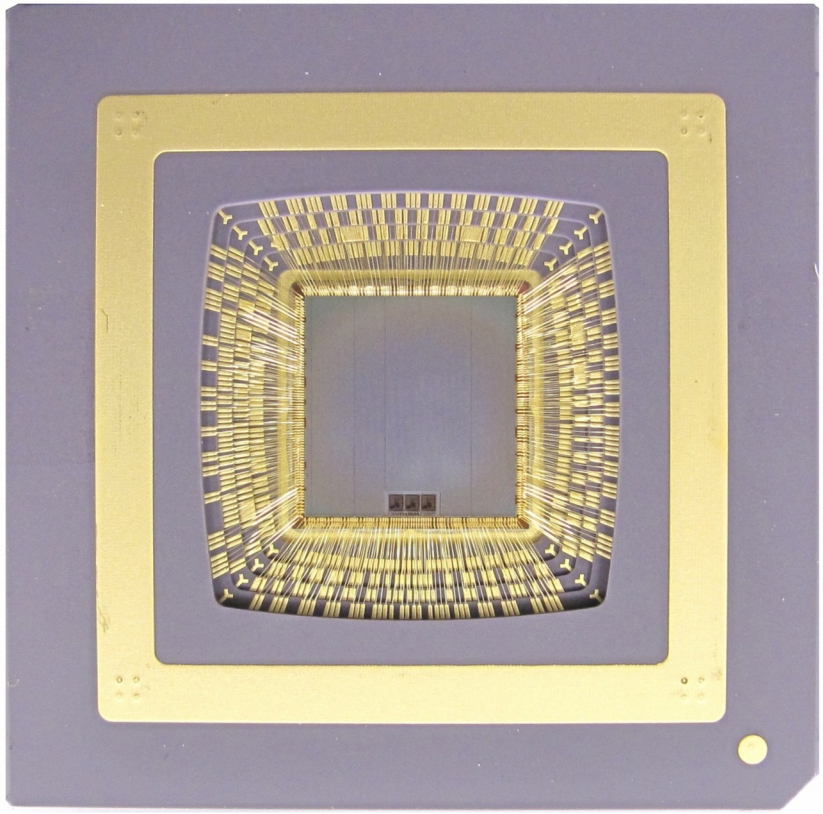


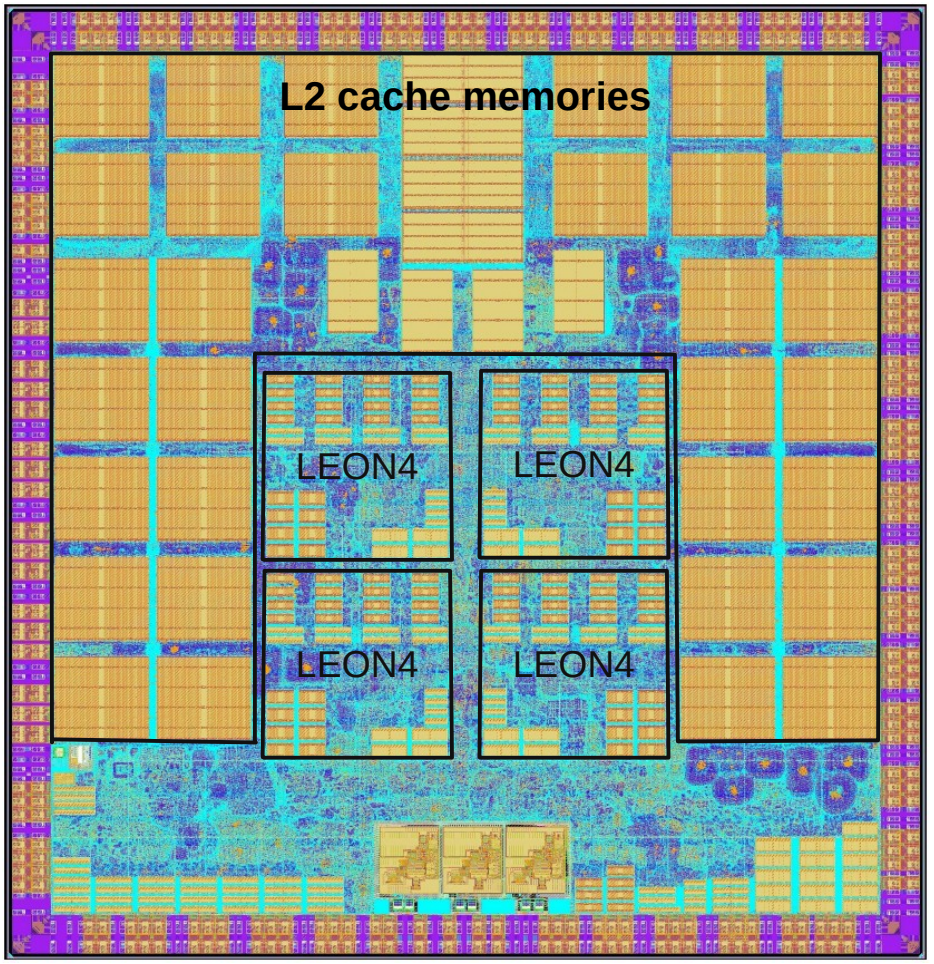
- **GR740 Prototypes**
- **Evaluation Board**
- **Development Box**

European Space Agency

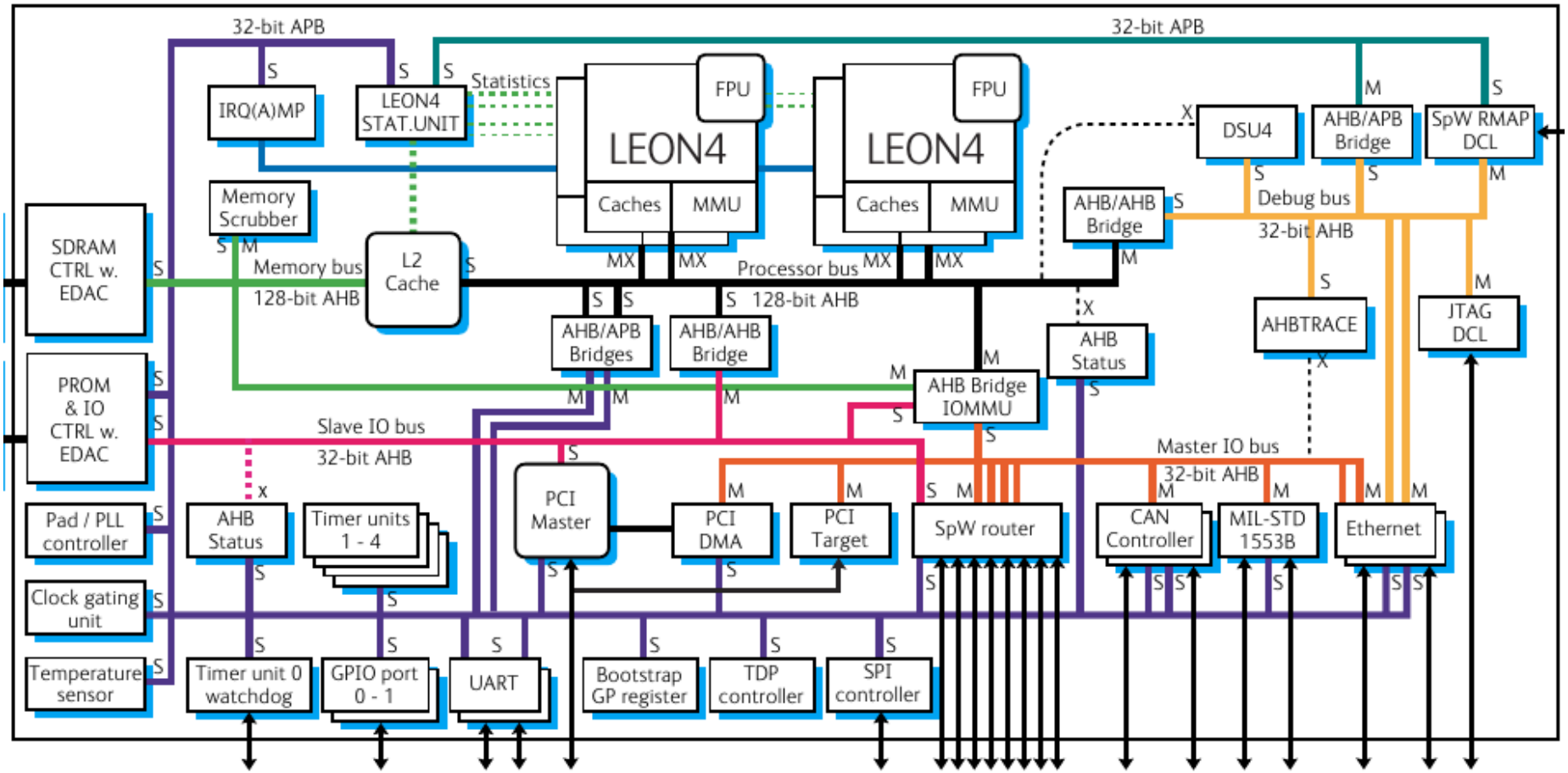
NGMP Phase 3: GR740 Flight Models

- Design updates and fixes (2017)
- Flight silicon manufactured (Q1/2018)
- Functional validation + radiation testing
- Packaging challenge (OPM, wire-bonding)
- Qualification in progress (FM delivery Q3/2020)





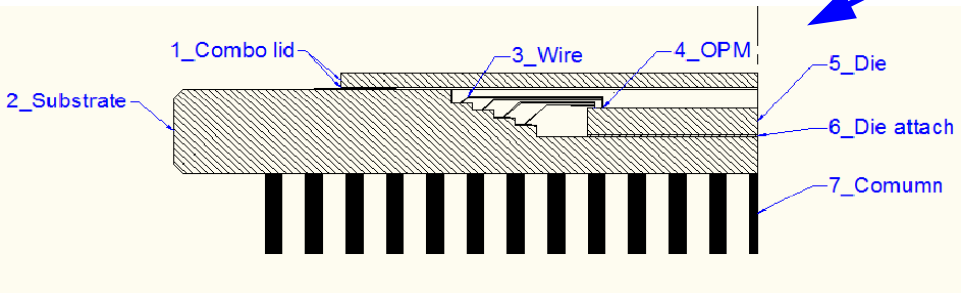
GR740 Block Diagram

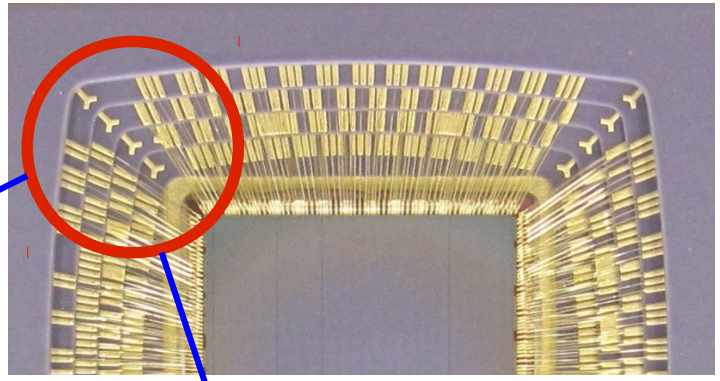


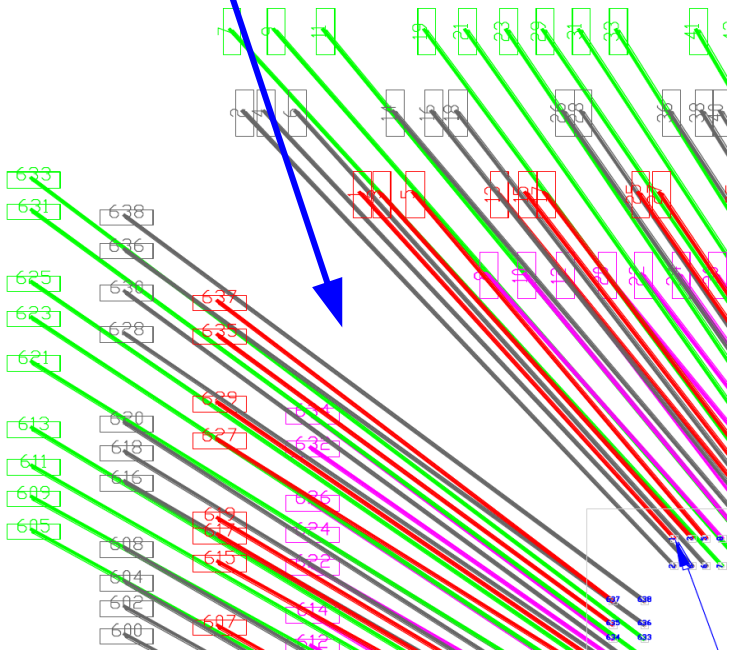
Qualification of wire-bond packaging

Complex Package

- 625 pins CGA (column-grid-array)
- Double pad-ring
- Long / crossing bond-wires
- Al-Au (chip-wire) metal interface:
  → OPM (Over-Pad-Metalisation)







- Flip-chip was not ready in time
- E2V has stopped wire-bond assembly
- STMicroelectronics had to develop a new package and qualify the assembly flow
- Column attach – possible suppliers:
  → HCM (FR), copper-wrapped columns
  → Micross (UK), IBM type columns
- OPM: ST had to develop new flow

Package area, power consumption

MA31750 Chip Set
2825 mm2
152 leads

MA31750
84-Lead Flatpack
40x40 mm

MA31751
68-Lead Flatpack
35x35 mm

ERC32 Chip Set
5139 mm2
672 leads

TSC691
256-lead MQFP
45x45 mm

TSC692
160-lead
MQFP
33x33 mm

TSC693
256-lead MQFP
45x45 mm

ERC32 Single Set
2025 mm2

1W / 20 MIPS
50 nW / inst

TSC695
256-lead MQFP
45x45 mm

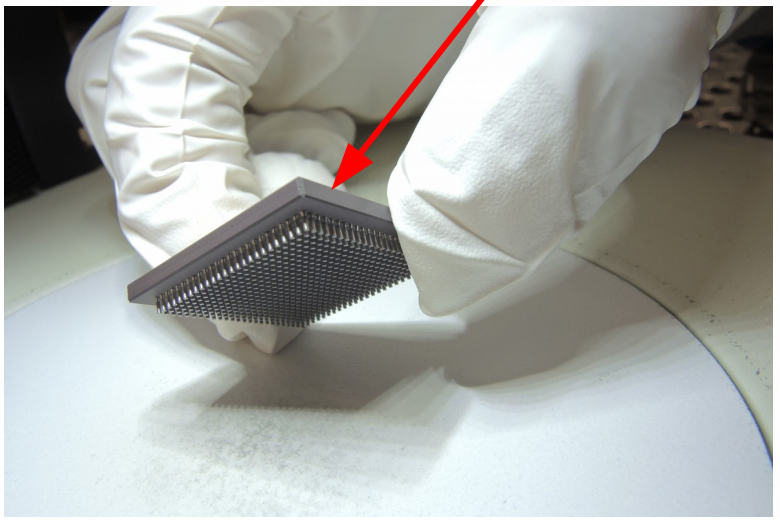
LEON2-FT
625 mm2
349 columns
1W / 86 DMIPS
10 nW / inst

AT697
MCGA 349
25x25 mm

GR740
841 mm²
625 columns

1.8W
1800 DMIPS
1 nW/inst

GR740
CCGA625
29x29 mm



Note: Areas without leads / columns

QFP: 8 mm² / lead
CGA: 1.8 mm² / col

NGMP / GR740 Related ESA Activities

SW ecosystem activities (201x = completion year)

- SIDMS (System Impact of Distributed Multicore Systems: XtratuM Hypervisor (fentiSS, Astrium, 2012)
- Multicore OS Benchmark project (BSC, 2012)
- Proxima for space (BSC, Rapita, various ESA and EU activities)
- AIR : Hypervisor (GMV 2015) (*)
- HAIR - Emulators of Future NGMP Multicore Processors (GMV, BSC, Rapita Systems, 2015)
- RTEMS Multi-Core and GAIA VPU demonstrator (Airbus, OAR, Gaisler, 2015)
- RTEMS Multi-Core and PROBA OBSW demonstrator (SpaceBel, Embedded Brains, U. Padova, 2015)
- RTEMS Symmetric Multiprocessing Optimization and Improvement for LEON Multi-core (Embedded Brains GmbH, completed in 2017)
- Parallel Programming Models For Space Systems (BSC, Evidence), 2016
- HP4S : High Performance Parallel Payload Processing f. Space (OpenMP, BSC, ADS, in progress) (*)
- Debug & trace tools for RTOSes on GR740 / TSP Demo of Linux for XtratuM, (ENEA, 2019)
- IMA Separation Kernel Qualification; XtratuM on GR712 (Teletel, 2019), GR740 port planned
- RTEMS-SMP qualification (in progress, Edisoft, Embedded Brains, Cister, Lero, Jena Opt.) (*)
- LeanOS Operating system (TU-Vienna, in progress) (*)
- Image processing on multi-core MTAPI/LEON4-N2X (2018) / OpenMP/GR740 starting (ENEA) (*)

Board-level activities

- GR740 Single Board Computer Reference Design (start Q4/2019, Gaisler, RUAG, ADS/TAS/OHB) (*)
- Surface Mount Technology (SMT): verification of columns qualification of soldering process (TAS Italy)
- CORA (HW, GR740 + BRAVE-FPGA and HW/SW co-design, TAS, ADS, Gaisler) (*)
- GR740 plastic packaging (starting now) (*)

(*) presented / announced today

Welcome

WELCOME

and enjoy the GR740 User Day