SMPW - Detailed Flow

MPW Workshop - ESTEC
June 17th, 2004
Summary

- Preliminary Quotation
- Firm Quotation
- Design Flow
- SMPW foundry
- Prototyping
- Flight Models Manufacturing
Preliminary Quotation (1)

- Mono-project flow
  - Request For Quotation
  - 1er level of feasibility
  - Preliminary Quote

Yellow = Customer
Green = Atmel
Blue = ESA
Dark green = Customer + Atmel
Pink = Everyone
**RTE: Request To Embark**

- Specific to SMPW
- On top of the technical information for feasibility study
- Customer provides to Atmel necessary information for quotation on SMPW
  - Space project
  - Target SMPW run
- If eligible to a reserved SMPW ESA, Customer and Atmel request for ESA approval
• Atmel requested information at RFQ
  ➢ ASIC name, project name
    ▪ ESA, non ESA
  ➢ Overall description of the functions
  ➢ Estimated number of logic gates
  ➢ Number, size and types of memory blocks
  ➢ Number of I/Os without supply (number of LVDS buffers if requested)
  ➢ Number of supply pads
  ➢ Expected operating frequencies
  ➢ Package
  ➢ Design review and prototypes availability date
    ▪ MPW or not
  ➢ Quantity of extra prototypes
  ➢ Quantity of FM
• ELAP: ESA Eligibility Approval
  ➢ Specific to SMPW
  ➢ ESA accepts to embark the design on an ESA run
  ➢ Written agreement from ESA to confirm the eligibility
  ➢ Firm commitment to be on a specific run number latest at “Logic Review Closing Date”

Flowchart:
- RFQ ➔ RTE
- 1er level feasibility ➔ ELAP
- ELAP ➔ Preliminary Quote
Preliminary Quote

- Technical Proposal based on the first level of Feasibility Study
- Quote includes ESA eligibility (if approved)
- Quote includes tentative planning with references to SMPW milestones
- Firm commitment to be on a specific run number latest at “Logic Review Closing Date”
Firm quotation (1)

- **DSR: Design Start Review**
  - Formal Review (Atmel + Customer) re-enforced on the following points
    - Matrix size
    - Detailed functionality review
    - Critical paths
    - Risks analysis
    - Power consumption
    - IO pads distribution
    - Resources analysis
      - Back-end design
      - Assembly and test
    - Prototypes (qty)
    - Flight Models (quality level, qty)
    - Planning
    - SMPW run on which to embark
  - DSR results are used to anticipate
    - Reticule organization
    - Wafers assignment plan
Firm quotation (2)

- Firm Quotation
  - Updated Technical Proposal based on DSR results
  - Quote includes updated planning with references to SMPW milestones
  - Firm commitment to be on a specific run number latest at “Logic Review Closing Date”
• Mono-project flow
  - Logic design (Customer)
  - Logic Review (Customer + Atmel)
  - Place and Route (Atmel)
    - Post layout simulations (Customer)
    - Design Review (Customer + Atmel)
Design Flow (2)

- Several designs running in parallel
  - Need for synchronization

Order Design n

<table>
<thead>
<tr>
<th>Logic Design</th>
<th>Logic design</th>
</tr>
</thead>
<tbody>
<tr>
<td>LR</td>
<td>LR</td>
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</table>

Order Design 1

<table>
<thead>
<tr>
<th>Place &amp; Route</th>
<th>Place &amp; Route</th>
</tr>
</thead>
<tbody>
<tr>
<td>Post layout simulations</td>
<td>Post layout simulations</td>
</tr>
<tr>
<td>DR</td>
<td>DR</td>
</tr>
</tbody>
</table>
Design Flow (3)

- LRCD: Logic Review Closing Date
  - Specific to SMPW
  - Fix date, made public in advance
  - All Logic Reviews have to be completed
  - "LR Closing Date" is the latest date for confirming
    - SMPW embarking approval (ESA)
    - Commitment to embark on the agreed planning (Customer + Atmel)
  - Reticule organization is frozen
  - Cancellation charges apply
Design Flow (4)

- **DRCD: Design Review Closing Date**
  - Specific to SMPW
  - Fix date, made public in advance
  - All Design Reviews have to be completed
  - Start of the reticule and wafers manufacturing
  - 4 months between “LR Closing Date” and “DR Closing Date”
On top of these 2 major fix dates, it is needed to re-enforce the standard management flow:

- During the Logic Design phase
- During the Place and Route
PLR: Pre Logic Review

- Intermediate milestone specific to SMPW (Atmel + Customer)
- No formal meeting requested, but at least a written report agreed by the customer
- To secure technical activities before “LR Closing Date”
- First net list transferred to Atmel for first trial of Place&Route
- Focus on
  - Technical issues
  - Planning issues
  - Resources issues
- Alternative solutions can be prepared
• LR: Logic Review
  ➢ Formal Review (Atmel + Customer) re-enforced on the following points
    ▪ Risks on the matrix size have to be identified
    ▪ P & R risks have to be identified
    ▪ Contingency plan has to be decided (when risks identified)
    ▪ Schedule has to be confirmed compliant with “DR Closing Date”
    ▪ Parts deliveries have to be confirmed
**Design Flow (8)**

- LR is completed
- Commitments from all the parties are firm
- Contingent plan to minimize the risks has been decided
• PDR: Pre Design Review

- Intermediate milestone specific to SMPW (Atmel + Customer)
- No formal meeting requested, but at least a written report agreed by the customer
- To secure technical activities before “DR Closing Date”
- Atmel has a priori completed the final layout
- Customer has to run and verify post layout simulations
- Focus on
  - Technical issues
  - Planning issues
**DR: Design Review**

- Formal Design Review (Atmel + Customer)
- Industrialization review if FM
- Post layout simulations are successfully completed
- Test oriented simulations (TOS) are successfully completed
- If Flight Models, procurement specification (preview) is available
From the “DR Closing Date” starts the SMPW service, that is:

- Reticule manufacturing
- Wafers manufacturing

- Design n
- Design 1

DRCD

SMPW
Reticule Manufacturing

SMPW
Wafers Manufacturing

Split in sub-lots mono-Project

Sub-lot for prototypes
Design n

Sub-lot for prototypes
Design 1

Remaining Wafers for Flight Models
• **SMPW-Reticule Manufacturing**
  - For each design, standard mask data-preparation
  - Anticipation possible if some DR completed before “DR Closing Date”
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SMPW foundry (3)

- SMPW-Reticule Manufacturing (cont’d)
  - Merge of all the designs in the SMPW Reticule
    - Frame building
    - Respect of the positioning rules defined for Space compatibility
    - Space inter dice filling to be compliant with space wafer fab requirements

Diagram:

1. Design n
2. Design 1
3. DRCD
4. Design finishing
5. SMPW Reticule Manufacturing
6. SMPW Wafers Manufacturing
7. Split in sub-lots mono-Project
- SMPW-Wafers Manufacturing
  - Launch of 1 lot (25 wafers) with SMPW reticule
  - Process AT58KRHA
  - Launched in Space quality level
Split in sub-lots mono-Project

- At Wafer Out, before probing, wafers individually assigned to each design for prototyping
- Remaining wafers are stored and can be used for Flight Models
Only 1 design type produced per wafer

- 5 parts
  - Engineering assembly
  - With datalog @-55°C, 25°C, +125°C

Delivered to customer 16 to 20 weeks after “DR Closing Date”

Extra prototypes possible
- Tested at 25°C only
- No data-log
Flight Models Manufacturing (1)

- Customer prototype approval (AGR)
- Individual assignment of Wafers for Flight Models
  - Only 1 design type produced per wafer
  - Depending on FM quantity
    - Assignment of remaining wafers to design 1 (if any remaining wafers)
    - Launch of a new lot for design n at no additional cost
Flight Models Manufacturing (2)

- **Probes and Assembly**
  - Same process as mono-project wafers
  - Some additional management rules to treat the wafer in mono-project mode

- **Test**
  - Same process as mono-project wafers