ATC18RHA - Offering Overview

MPW Workshop - ESTEC
June 17th, 2004
Summary

- ATC18RHA Features
- Standard Cell Library
- I/Os Libraries
- Memory Libraries
- Die sizes
- Assembly and Packages
- ATC18RHA availability
ATC18RHA Features

- **Technology**
  - 0.18µm CMOS Rad Hard technology
  - 5 metal layers
  - 1.8V power supply for the core
  - 1.8V and 3.3V power supply for the periphery

- **Libraries**
  - Standard Logic and IO Cells Libraries
  - Memory libraries
  - PLL (480MHz)

- **Space standards**
  - High Reliability
  - Radiation
    - TID better than 200Krad
    - SEL better than 70MeV.cm²/mg
Standard Cell library

- Buffers and Gates
- Multiplexers
- Standard and SEU Hardened Flip-flops
- Standard and SEU Hardened Scan Flip-flops
- Latches
- Adders and Subtractors
• 2 libraries
  ➢ IO18 : 1.65 to 1.95V
  ➢ IO33 : 3.0V to 3.6V

• Buffer types
  ➢ Bidirectional
  ➢ Tristate Output
  ➢ Output Only
  ➢ Input Only (Inverting, Non-Inverting, Schmitt Trigger)

• Additional buffers of IO33 library
  ➢ 3.3V PCI Bidirectional, Tristate Output and Output Only
  ➢ LVDS Transmitter and Receiver differential (based on the ANSI/TIA/EIA-644 Standard)
  ➢ LVPECL Receiver differential
• **IO33 and IO18 buffers are Cold Sparing**
  - When VCCB is “off” these pads have a negligible leakage current

• **Standard IO33 buffers are tolerant (PCI,LVDS,LVPECL excepted)**
  - When the pad is configured as an input, and VCCB is < 3.3V (ex 1.8V), the external signal can go up to 3.3V (max 3.6V) with negligible leakage current

• **An IO33 standard buffer with VCCB=1.8V can also be used as a 1.8V Compliant Output with degraded IOL,IOH and timing performances**
Memory libraries

- Compiled memories
  - VIRAGE compilers
    - SRAM (32kx16)
    - DPRAM (8kx32)
    - TP Register File (1kx16)
  - Synchronous only
  - EDAC VHDL

- Synthesized memories
  - Genesys Atmel software
    - RAM (4k)
    - TPRAM (4k)
    - DPRAM (2k)
  - Asynchronous
  - SEU hardened cells used
Die sizes

- 95µm pad pitch and pad width, except
  - LVDS transmitter
    - width= 3x95µm and pitch=190µm
  - LVDS Receiver and LVPECL Receiver
    - width=2x95µm and pitch=95µm

- Predefined die sizes
  - To allow re use of existing MH1RT packages
  - To ease the SMPW management
**Predefined die sizes**

<table>
<thead>
<tr>
<th>ATC18RHA95_216</th>
<th>Equivalent MH1 matrix size</th>
<th>Size (mm²)</th>
<th>Programmable pads</th>
<th>Buffer Power supply pads</th>
<th>Typical Nbr of Gates</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATC18RHA95_324</td>
<td>MH1099E</td>
<td>8.76x8.76</td>
<td>324</td>
<td>8</td>
<td>2.2M</td>
</tr>
<tr>
<td>ATC18RHA95_404</td>
<td>MH1156E</td>
<td>10.66x10.66</td>
<td>404</td>
<td>8</td>
<td>3.5M</td>
</tr>
<tr>
<td>ATC18RHA95_504</td>
<td>MH1242E</td>
<td>13.03x13.03</td>
<td>504</td>
<td>8</td>
<td>5.5M</td>
</tr>
</tbody>
</table>
### Preferred Hermetic Multi-layer Packages

<table>
<thead>
<tr>
<th>SMD / Package Variant</th>
<th>Number of leads</th>
<th>Marketing Code</th>
<th>ATC18RHA95_216</th>
<th>ATC18RHA95_324</th>
<th>ATC18RHA95_404</th>
<th>ATC18RHA95_504</th>
</tr>
</thead>
<tbody>
<tr>
<td>MQFPF</td>
<td>T352</td>
<td>YC</td>
<td>U88N (*)</td>
<td>U85N (*)</td>
<td>U80N (*)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>256</td>
<td>KZ</td>
<td>U89N (*)</td>
<td>U90N (*)</td>
<td>U76N (*)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>196</td>
<td>K9</td>
<td>X(*)</td>
<td></td>
<td>U92N</td>
<td></td>
</tr>
<tr>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCGA</td>
<td>625 (**)</td>
<td>2D</td>
<td></td>
<td></td>
<td></td>
<td>EF401 (*)</td>
</tr>
<tr>
<td></td>
<td>472</td>
<td>2C</td>
<td></td>
<td>H06N (*)</td>
<td>H05N (*)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>349</td>
<td>2E</td>
<td>H04N (*)</td>
<td>EF378 (*)</td>
<td>EF379(*)</td>
<td></td>
</tr>
<tr>
<td>Die</td>
<td>Die</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

(*) 4 decks package  
(**) fine pitch 1mm
Double pad ring

- Pad pitch 95µm (ceramic package limitation)
- Inner ring for core power supply
- Outer ring for buffer power supply and IOs
- ATC18RHA95_504 ‘matrix’
- Prototype level only

Future development
- Double pad ring for FM and any ‘matrix’
- Flip chip assembly
Development status

• Beta Design Kit available since end of March 2004
  - 2 CDROMs: ASIC Design Kit and SIGMA Design Kit
  - NDA requested for the SIGMA Design Kit

• Beta design
  - ATC18RHA95_504, MCGA472, double pad ring
  - Design Review, mid of July
  - 1st samples in November

• Final design kit to be released end of 2004
  - Results of V34 and V35 silicon (characterization and radiation)
  - On DVD