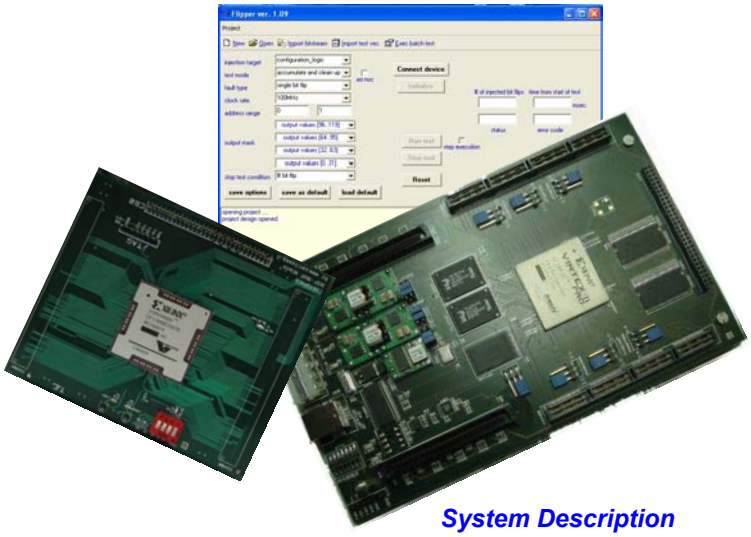


## *Overview*

FLIPPER* is a tool aimed at evaluating Single Event Upset (SEU) effects in Xilinx Virtex II SRAM-based Field Programmable Gate Arrays (FPGAs). SEUs are emulated by fault injection into the configuration memory and reconfiguration logic registers.

FLIPPER offers high flexibility in setting up fault injection tests, since the design under test is implemented in a separate DUT Board stacked on a Control Board. This allows to test different devices by implementing the corresponding DUT Board and to evaluate a single design on different devices. Besides, various test operating frequencies are available and the number of test signals can be defined in a wide range.

SEUs are injected by bitstream manipulation. Both single and multiple SEUs can be injected. In case of multiple SEUs, two adjacent bits in a frame are modified at one time. One single injection at a time is performed, after which the DUT is exercised for the whole set of test vectors. The effects of an injection always sum up to the effects of the previous ones.

The location in the bitstream of an injected SEU can be random, sequential, or user defined. Sequential means that every bit of the bitstream in the configuration memory or configuration control registers is accessed and modified in sequential order. In user defined mode, selected locations for injection are provided via text file.

FLIPPER provides features for importing test/gold vectors from Mentor Graphics ModelSim. Injection results from FLIPPER can be easily imported in a worksheet or data base.

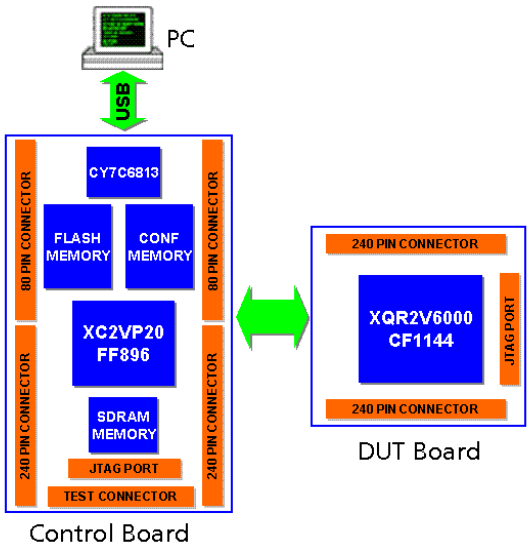
## *System Description*

The system comprises three main parts:

a flexible FPGA-based board (Control Board), that rules the fault injection procedure

a DUT (Device Under Test) board, that contains the FPGA to be tested, an XQ2VR6000 device

a Personal Computer.




FLIPPER manages up to 150 triplicated test signals, comprising one synchronous test clock, toward the DUT, and up to 120 triplicated signals from the DUT.
The maximum depth for a continuous run is 3.5k samples at 100 MHz clock rate. However, for full synchronous DUT design there is no limit in the maximum depth, as the test clock can be suspended.

* Patent Pending.

Besides, 50, 10, and 5 MHz frequencies are also allowed.

In order to implement triple-voted outputs based XTMR solution to the design under test, many pins of the DUT FPGA are wired together in triplets on the DUT board.

## *Features*

The Control Board houses an XC2VP20 FF896, a 128 Mbit FLASH memory, a 1 Gbit SDRAM memory, an 8051 microprocessor, a configuration PROM, a P160 expansion interface (Memec), and the DUT interface. The board in principle can fully test V2, V2 Pro, V4, and next generation devices with some limitations. There is a limit in the number of DUT I/O's that can be driven by the P20 device. The total number of I/O pins towards the DUT Board is 416.

XILINX VIRTEX-II PRO FPGA
XC2VP20-5 FF896
- 20.880 logic Cell (2 million gates equivalent)
- 56 x 46 CLB array
- 9.280 Slices
- 290 kbits Maximum Distributed RAM
- 88 Select RAM block (18-Kbit each) Tot 1584 kbits
- 88 Dedicated Multiplier (18x18)
- 8 DCM blocks freq (24MHz min 420MHz max)
- 2 Power PC processor
- 8 RocketIO Transceiver block 3.15Gbps (non connected)

DEDICATED USB 2.0 CONTROLLER
Cypress FX-2 CY7C68013-56PVC
- integrated 8051 CPU
- 48 MHz CPU clock
- up to 25 MByte/s constant data throughput
- with standard USB2 driver and firmware

TWO SDRAM MEMORY DEVICES (DDR multi footprint ready)
Micron MT48LC32M16A2TG-75
- Capacity 128 MByte
- Organization 32M x 32bit
- Cycle time 10 ns
- no shared pins

Ready to drive DDR memory
- Capacity up to 256 Mbyte
- X4 speed

TWO FLASH MEMORY DEVICES
Intel TE28F640J3C115 S L7GZ
- Capacity 16 MByte
- Organization 4M x 32bit
- Cycle time 10 ns
- no shared pins

XILINX PLATFORM FLASH
XCF08PV048C
- ISP

CHIP FOR TEMPERATURE CONTROL
National LM 83
- bus I2C
- flag threshold
- Ambient temperature
- Control FPGA temperature
- FPGA Under Test temperature

NON VOLATILE MEMORY
- 32 kByte I2C E2PROM for Cypress configuration

TWO INDEPENDENT OSCILLATORS
- two customizable frequencies

JTAG CONNECTOR
- Standard XILINX 14-pin JTAG header

TWO CONNECTOR P240
- DUT-Board Link high density high speed ( 0.5 mm,1.6GHz)
- 376 I/O user available

CONNECTOR P160
- Standard Memec connector for standard expansion boards
- shared pins with P240 CONN.

TEST CONNECTOR P60
- Accessible 2 mm test connector
- Ground and all power supply voltages including DC IN
- 40 I/O user available

LEDs
- Power LED
- FPGA configuration LED

DIMENSIONS
- 22 cm x 12 cm

SOFTWARE AND DRIVERS
- Standard USB2 driver included- Designed for Windows XP, Windows 2000
- Data communication via USB 2.0
- fault injection capability

SINGLE POWER SUPPLY
- Volt DC, 10A max.
- electrically isolated DC/DC converter
- 15A switching 1.5Volt voltage regulator
- 15A switching 2.5Volt voltage regulator
- 6A switching 3.3Volt voltage regulator
- 1.5A linear 1.8Volt voltage regulator

## *CONTACT*

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