astrium

Development and Tests Results of a System On a Chip for a Data Handling System

CONTENTS

1. **Contract and Studies presentation**
2. **Architecture and main IP blocks of the System On a Chip (SOC)**
3. **Development and Tests drivers**
   a. Overall architecture/performances assessment
   b. Interfaces standardisation
   c. Methodology
   d. Tools
   e. Documentation
4. **Results of the development**

© Astrium

STUDY OBJECTIVES

- Study of the integration of complex systems called « System On a Chip » within an ASIC intended for space flight
- Define and use a methodology based on IP VHDL blocks coming either :

PROCUREMENT SOURCE	CONSTRAINTS
Commercial vendors	➢ Easy access for other users
ESA	➢ Stay property of ESA
From the background of the company	➢ Stay property of ESA
Developed in this activity	➢ Become property of ESA with rights of use for the designer

© Astrium

DEVELOPMENT PLAN OF THE SOC

- **Initial analysis and requirement specification**

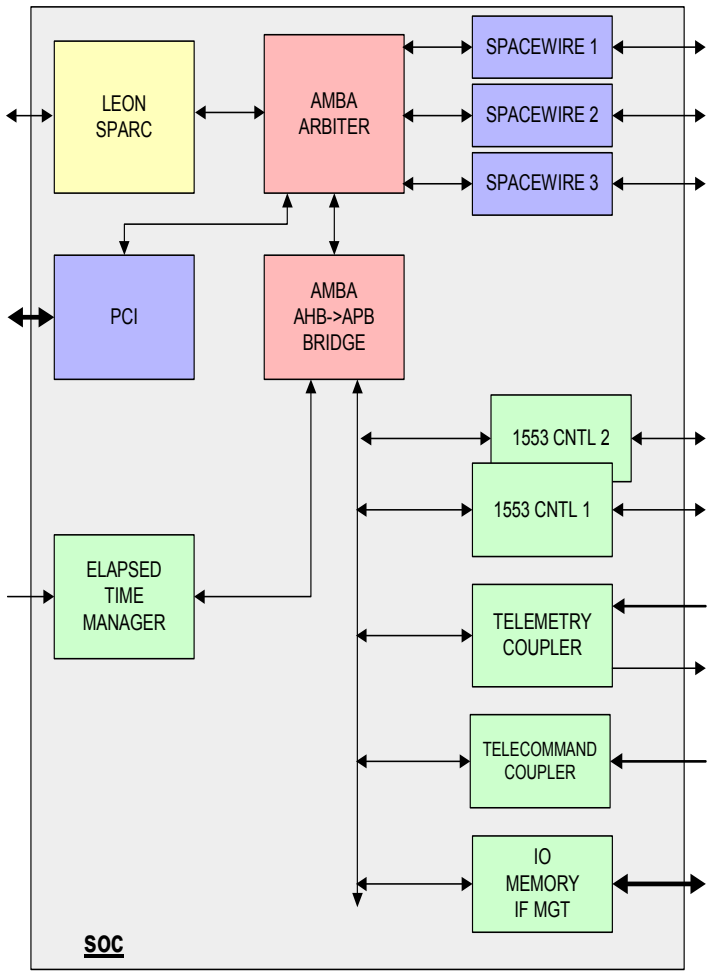
- **Architectural design consist in :**
  - Architecture study of block interconnect scheme
  - Functional specification of the IP macros with their HW/SW ICD
  - Low-Level software pre-study and ICD specification
  - Development / modification for adaptation of the IP macros
  - Simulation at VHDL RTL level / Environment developed in VHDL on a « standard » basis

- **SOC approach is verified / debugged on a demonstration board with SOC function integrated in a FPGA with limited low-level software**
  - Activity performed in parallel with the simulation
  - Progressive integration of the IP macros

© Astrium

SOC SIMPLIFIED BLOCK DIAGRAM

- **The SCoC includes the main digital functions necessary to perform the Data Handling of a Spacecraft :**
  - The CPU core based on LEON with its FPU
  - An internal SOC bus based on AMBA buses (ARM trademark)
  - A parallel PCI bus at board level
  - SpaceWire fast serial links
  - 1553 serial buses for control of remote equipments
  - An Elapsed Management Time function (RTC, Timers, Synchronisation)
  - A CCSDS TeleCommand function
  - A CCSDS Telemetry function



© Astrium

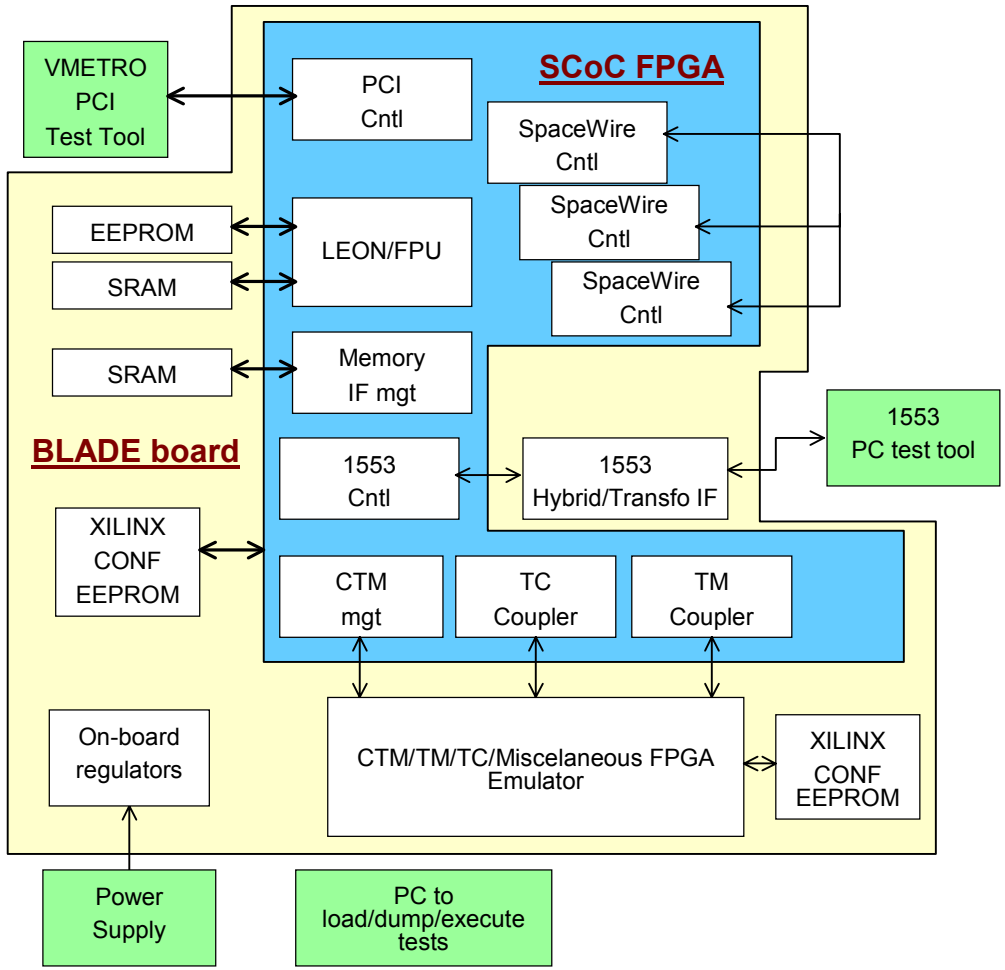
SOURCE OF THE IP MACROS

MACRO	SOURCE	Work at ASTRIUM
LEON	ESA	Configuration of the block
FPU	SUN / MEIKO	Extraction of the FPU from the SUN micro Sparc IP
PCI	InSilicon	ESA has developed a wrapper integrated in LEON
CTM	ESA	Integration in SCoC
IP1553	ASTRIUM	Modification of the existing MAT53 BC/BM/RT
PTCD	ASTRIUM	Modification of the existing CCSDS PTD controller
PTME	ESA	Integration in SCoC
HDMA	ASTRIUM	Full development
Spacewire	ASTRIUM	Development based on ESA work

© Astrium

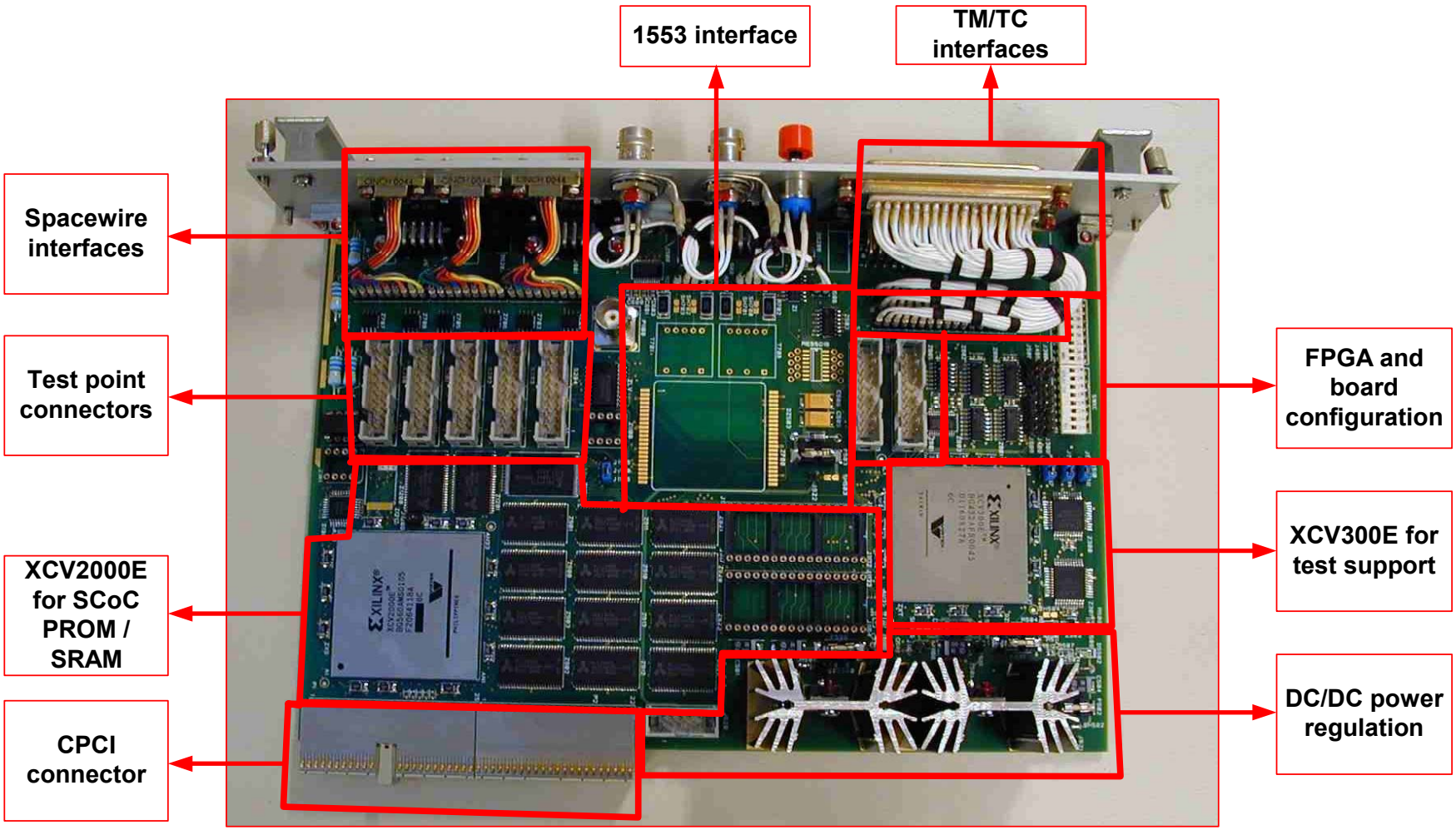
SCOC TESTS ENVIRONMENT

- **BLADE board including**
  - SCoC FPGA
  - Miscelaneous Memories
  - XILINX emulator
  - Power supplies regulators
- **BLADE board environment**
  - PCI test tool
  - 1553 test tool
  - Laboratory power supply
- **BLADE board test**
  - SpaceWire loopback
  - CTM/TM/TC with XILINX emulator
  - 1553 with 1553 test tool



© Astrium

BLADE BOARD DEFINITION



© Astrium

DEVELOPMENT AND TESTS DRIVERS : OVERALL ARCHI/PERFO ASSESSMENT

- **LARGE SYSTEM FOR MANY APPLICATIONS:**
  - To be clear with targeted applications in order to avoid conflict between requirements
  - To be clear with performance requirements applicable to various applications
  - To keep maximum CPU performances within the architecture whatever the traffic rate on IOs
  - To have a good evaluation of external & internal data flow performances
  - To be clear on hardware/software sharings
  - To implement programmability to match various applications

- **LEON PROCESSOR with CACHE MEMORY:**
  - Bus utilization is depending on software implementation
  - Bus analysis performance is based on statistics
  - Real time performances analyses for hardware performed without cache

© Astrium

DEVELOPMENT AND TESTS DRIVERS : INTERFACES STANDARDISATION

- **SOC DEVELOPMENT REQUIRES STANDARDISATION BECAUSE:**
  - SOC is based on re-use and integration of IP (Intellectual Property) cores coming from various sources to be adapted on a standard backbone
  - Standardization of internal interfaces ease the re-use of already developed IP
    - → Internal SCoC bus architecture developed here with ESA is based on the AMBA® AHB and APB busses standard
  - Standardization of external interfaces reduces the number of IP and increases IP re-use
    - → Main communication interfaces implemented in SCoC are Spacewire, 1553, PCI

© Astrium

DEVELOPMENT AND TESTS DRIVERS METHODOLOGY (1)

- **SOC IS MORE THAN A LARGE ASIC, IT IS A COMPLEX ASIC**
  - Architectural design : Main challenge is validation/simulation at RTL level
  - Deep simulation at block level - Simulation at top level oriented towards inter-IP communication and non regression for the IP
  - Progressive integration of the IP ease the validation of the SCoC
  - Methodology for test-bench reuse, from IP to upper board, unit & system levels

- **SIMULATION**
  - Make synchronous design – containment of asynchronisms if unavoidable at IP level
  - Static timing analysis
  - Do functional validation on hardware => development of a test board

© Astrium

DEVELOPMENT AND TESTS DRIVERS METHODOLOGY (2)

- **Validation of Scalable IP core VHDL description is limited**
  - Each IP is hardware configurable (from simple FIFO size to behavior on internal bus)
  - Definition of validation levels : IP level, SOC level, System level : for each level, a given set of configuration is validated
  - Reuse of IP for different configurations need additional validations in the new system definition

- **Need Traceability Of Validated IP Configurations**

- **Need Feedback Of IP Users & Software tests**

© Astrium

DEVELOPMENT AND TESTS DRIVERS - TOOLS

- **From the basics …**
  - Versions control is mandatory and is associated to the validation traceability

- **To the customs …**
  - Simulation of Hardware/Software interactions eased by the used of a customized interface for Software tracking
  - Automatic generation of constants for VHDL description and software => reduction of bugs related to HW/SW interfaces

- **To the most elaborated : Commercial industry drives the development of software tools for SOC development :**
  - We should use these tools if the return is important (and then the number of designs to produce)
  - We should use these tools If they are absolutely necessary (which is of course the case of e.g. simulator or synthesis tools)

© Astrium

DEVELOPMENT AND TESTS DRIVERS - DOCUMENTATION

- **Strategy of SCoC documentation = Board/Equipment documentation**
  - SOC = EQUIPMENT/BOARD
  - IP = BOARD/ASIC

- **SOC related documentation**
  - Synthesis of the SOC functionalities / ICD, Architecture
  - Refer to sub-level (IP) documentation for detailed description.
  - Necessity of a CIDL (Configuration Item Data List)

- **IP documentation includes :**
  - Specification/ICD : for the use of the IP at upper level (software, system)
  - Architecture description / Database description : for the maintenance of the IP
  - Hardware User's Manual for implementation of the IP

© Astrium

RESULTS OF THE SCoC DEVELOPMENT

- **CPU performances depends on Spacewire links usage**
- **Performance bottleneck identified at external RAM level**

- **SCoC implemented on the BLADE Board**
  - Development platform for avionics systems (hardware & software) with LEON, Spacewire, 1553, TM/TC

- **A number of IPs on AMBA available: Spacewire, TM, TC, 1553 IP BC/RT/BM, CTM, DMA, PCI**
  - Service to users for implementation, Adaptation to user applications
  -

- **3 x Boards used for Advanded Architecture of Avionics (A3M) study :**
  - Use of LEON / VxWorks OS
  - Inter Processor communication through Spacewire (3 nodes) and time synchronisation (CTM)

© Astrium