SCOC – A Spacecraft Controller On-a-chip

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Roland Weigand
European Space Agency
Control and Data Systems Division
Microelectronics Section TOS-ESM
Tel. +31-71-565-3298
Fax. +31-71-565-4295
Roland.Weigand@esa.int

Marc Souyri
Marc Lefebvre
Astrium SAS, Vélizy France
Tel. +33-1-34 88 43 14
Fax: +33-1-34 88 34 83
marc.souyri@astrium-space.com
marc.lefebvre@astrium-space.com

Overview

- ***System-On-Chip in Space***
  - Advanced microelectronic technologies improve performance vs. power/mass ratio
  - Increased reliability of on-chip interconnect allowing for reduced cross-strapping
- ***Spacecraft (Data Handling) Controller as a Standard Component***
  - Standard component for multiple missions to offset NRE cost
- ***Design Methodology***
  - System design aspects equivalent conventional board-based design
  - IP core based design with technical and legal consequences
- ***The SCOC Contract with Astrium Vélizy***
  - Definition phase and feasibility study
  - SCOC development for FPGA target
  - Demonstration board (“BLADE”)
- ***Future Steps***
  - Validation, refinement and settlement of specification (user involvement)
  - ASIC manufacturing, documentation, software drivers, qualification
  - Spin-off to a space qualified (PROM-based) FPGA device

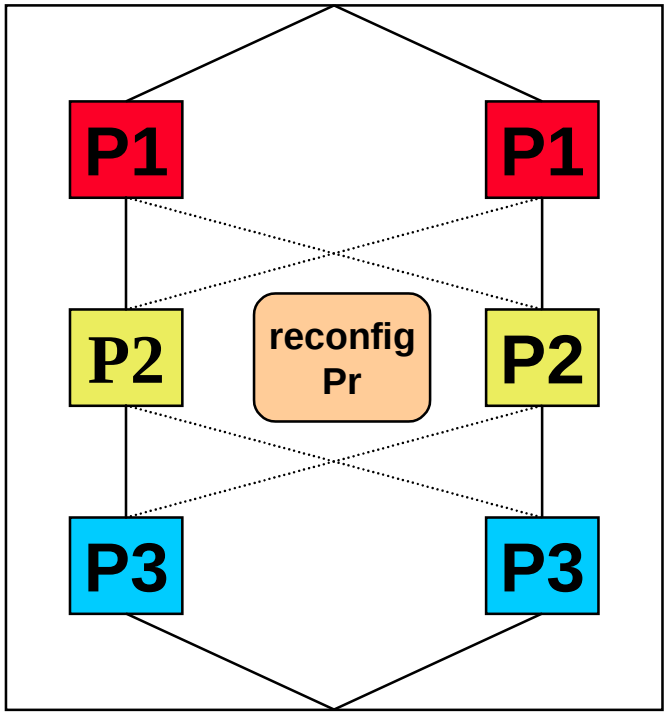
System-On-Chip in Space

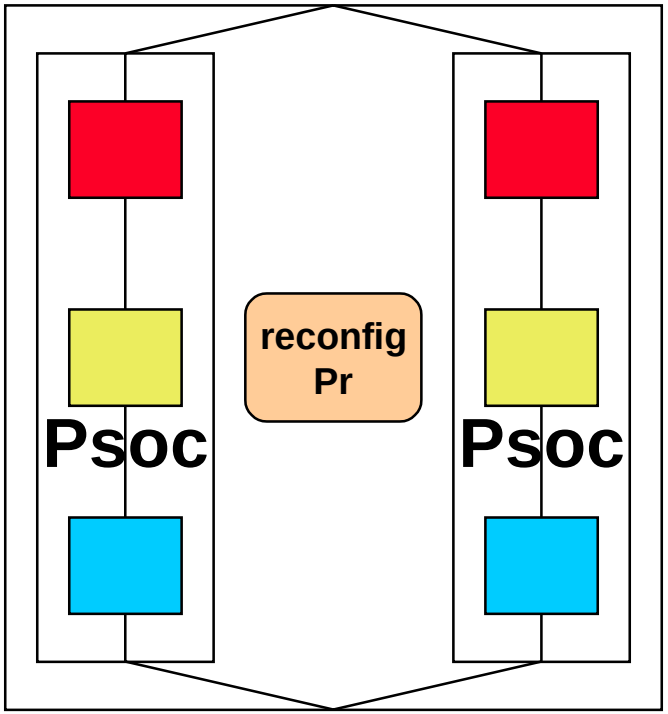
- ***State-of-the-art technologies in space***
  - Antifuse FPGA (RT54SX72S) ~ 36k ASIC equivalent gates (source Actel)
  - 0.5 µm and 0.35 µm ASIC is state of the art, allowing several 100 kGates
- ***Upcoming technologies***
  - Antifuse FPGA ~ 250 ASIC equivalent kGates announced (Actel RTAX)
  - 0.18 µm ASIC under development for space, allowing 1 Mgates or more
- ***Integration of multiple functions into a single chip***
  - External connections (board soldering) become on-chip interconnects
  - Reduced power consumption
  - Reduced component count (→ mass)
  - Increased performance
  - Increased reliability
  - Reduced accessibility of internal functions → testability issues
- ***SOC on ASIC requires careful system design at component level***
  - High NRE cost (several 100k)
  - Long design turnover times (months/years)
  - Expensive and long bug-fixing, spec changes, re-design

Fault Tolerance with SOC

- ***Conventional system***
  - Separate components for each function
  - Duplication of each component
  - Multiple cross-strapping
  - P(failure) = $P1^2 + P2^2 + P3^2 + Pr$

- ***SOC based system***
  - Single SOC component
  - Duplication of the SOC
  - Global cross-strapping
  - P(failure) = $Psoc^2 + Pr$





SCOC Definition

- ***The SCOC ASIC - a standard component ➔ offset high NRE cost***
  - Standard processor, known to the space community → LEON SPARC-V8
  - Flexible peripherals, which can be powered down
  - Telecommand and Telemetry (TM/TC) functionality → CCSDS
  - Housekeeping and CCSDS Time Management
- ***Multiple standard interfaces***
  - PCI parallel backbone
  - Spacewire (IEEE 1355.1)
  - MIL 1553 standard Bus Controller/Monitor (BC/BM) and Remote Terminal (RT)
- ***Dedicated data processing (not part of the current SCOC contract) e.g.***
  - Monitoring camera interface and image compression
  - GNSS navigation receiver
  - Star tracker pre-processor
  - Mathematical co-processor

SOC Design Methodology

- ***System design issues – but now at chip level***
  - CPU usage, data/interrupt rates and bus bandwidth analysis
  - Defining interfaces and bus architectures, arbitration schemes
- ***Design based on IP cores from various origins, having different…***
  - Hardwired configuration options
  - Clocks, resets, interface standards and standard-interpretation
  - Status of verification (existing testbenches, experience) and documentation
  - Description languages (VHDL, Verilog, SystemC…)
  - License conditions
- ***SOC integration of IP cores means***
  - Configuration of IP cores (and their verification)
  - Defining clock and reset strategy, homogenizing interfaces,
  - Complementing verification at block level
  - Editing (not only copy-paste) the data sheet
  - Overcome interface/tool problems in a multiple language environment
  - Ensuring the testability
  - Top level verification

The SCOC Contract

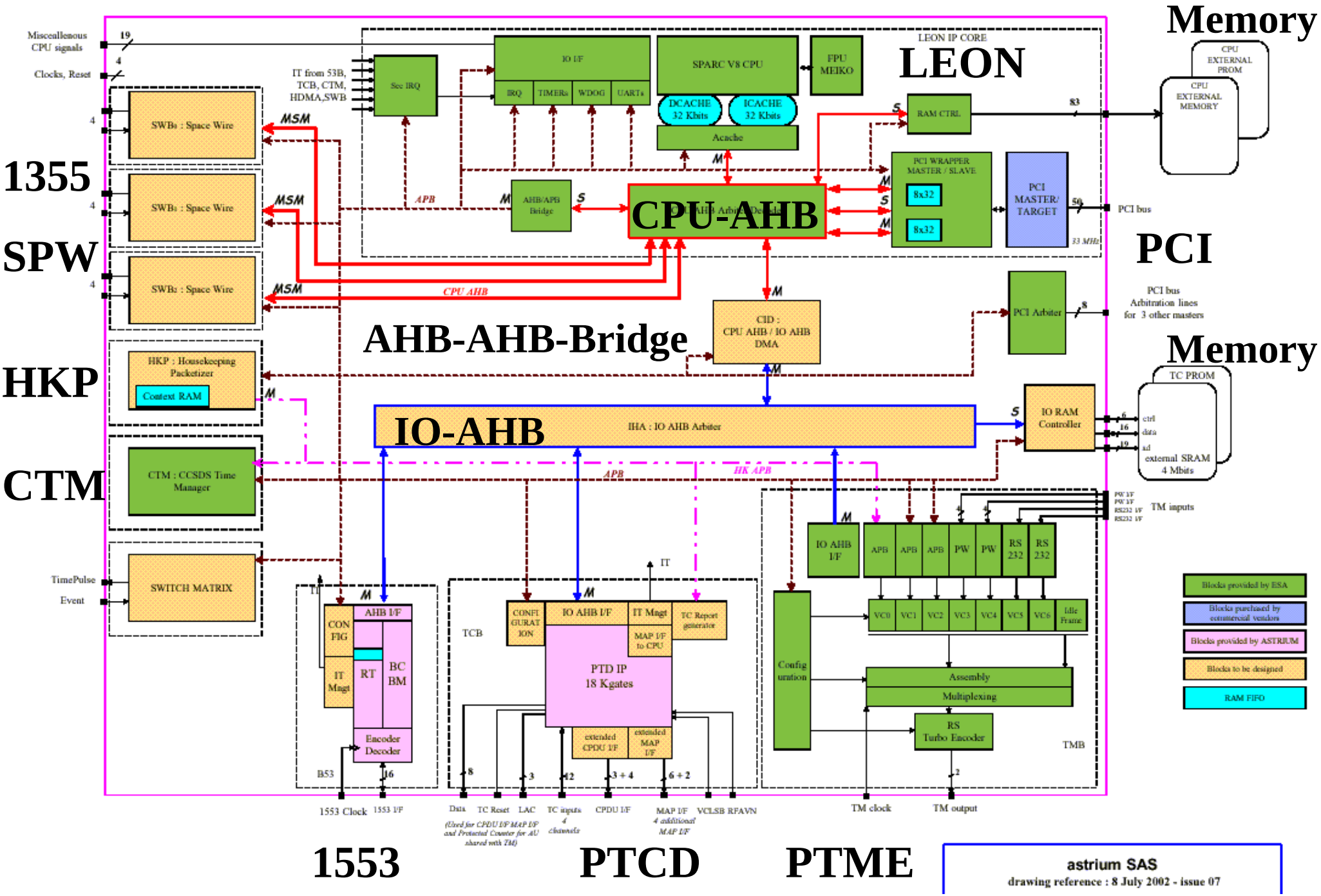
- ***ESA Contract 13345/98/NL/FM with Astrium SAS, Vélizy***
  - Initial ITT, initially targeting a SOC-ASIC Q3/1998
  - Kick off (1999) frame contract “Building Blocks for System-On-a-Chip”
    - » 3 call-off orders (COO)
    - » Defining a generic IPR model for the cores
  - COO 1: “EVI32 VME bus interface ASIC for ERC32” up to industrialisation
  - COO 2: “SCOC feasibility study and definition”
- ***COO3 “Development of a SOC Device”: kicked off in February 2002***
  - Update of feasibility study and specification
  - Adaptation of PTCD and 1553 ASIC designs to IP cores
  - Design of a Spacewire IP core
  - Blocks provided by ESA (PCI interface, CTM, PTME)
  - Design of SCOC into Xilinx Virtex 2000 target in two configurations:
    - » *LEON + FPU, PCI, 3 spacewire, 1553, (for A3M)*
    - » *LEON, PCI, 1 spacewire, 1553, TMTC (TMTC validation)*
  - Development of the Board for LEON and Avionics DEmonstration (BLADE)
  - Initial verification, partial validation in A2M activity
- ***End date***
  - Foreseen in 2003

IPR Core Licensing Model

- ***a) Developed in the frame of the present contract***
  - ESA property, contractor is granted license for his own purposes
- ***b) Derived from devices developed under previous ESA contracts***
  - Contractor property, ESA has right to distribute for ESA funded activities
- ***c) Considered as background information***
  - Contractor property, ESA has right to use internally
- ***d) Cores property of and delivered by ESA***
  - ESA property, contractor has right to use them only for present contract
- ***e) Commercial third-party cores***
  - ESA should be (prime-)licensee…
  - … allowed to grant sub-licenses for designing space devices
  - Contractor to be granted a license only for the present contract
  - Sub-license model has proven difficult to implement
  - Licensee has to warrant for the confidentiality of the source code!
  - ***Conclusion: better rely on own (or open) cores***

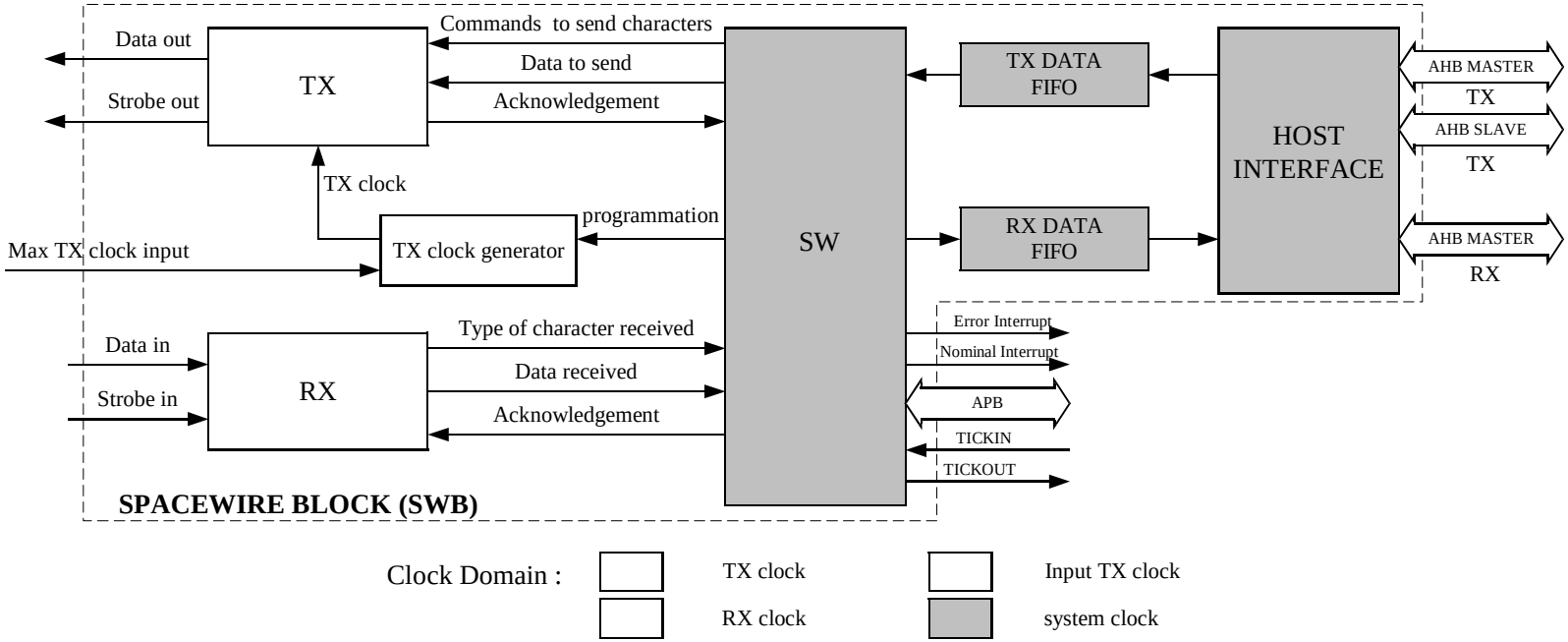
Spacecraft Controller-On-a-Chip Block Diagram

astrium SAS



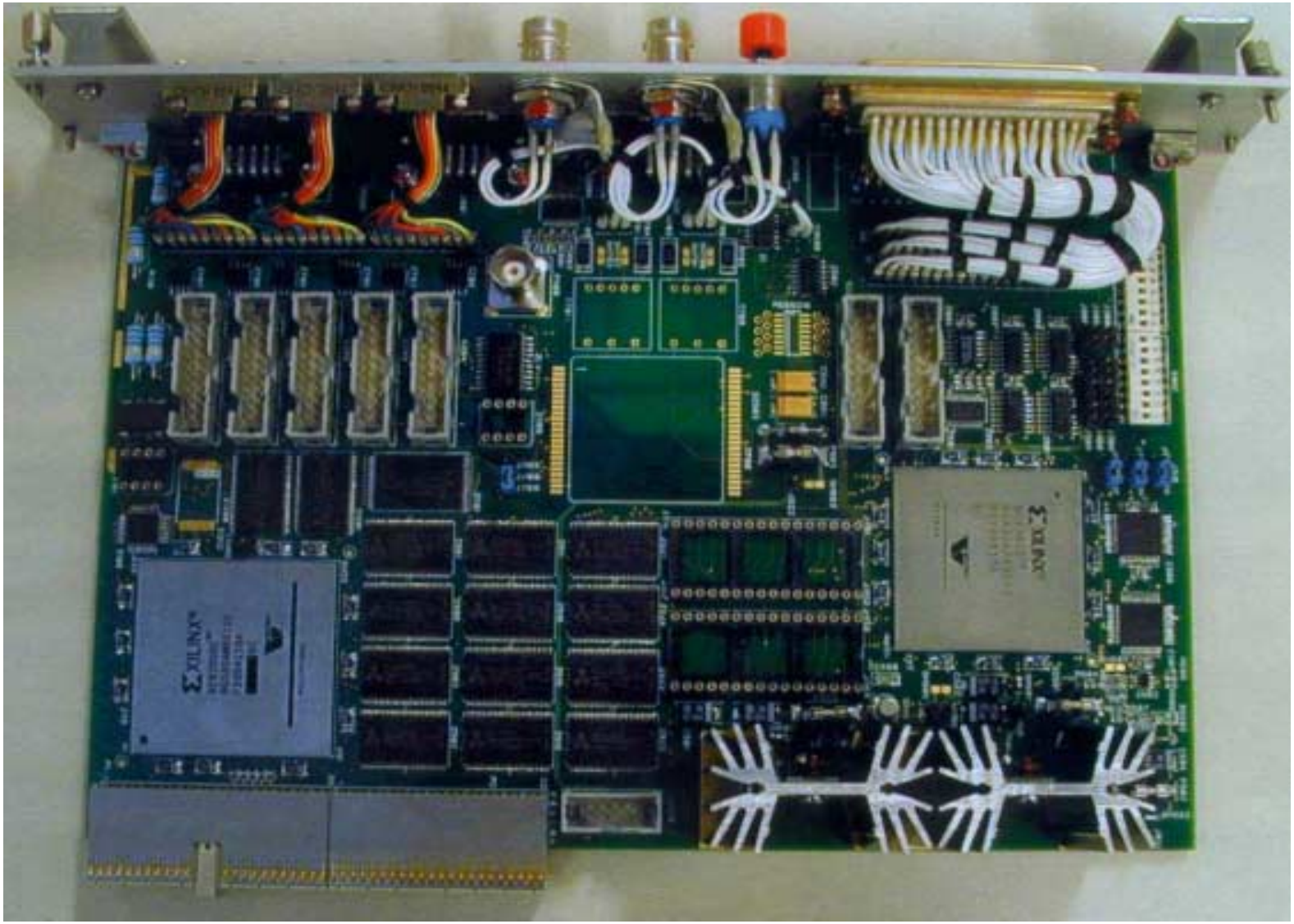
astrium SAS
drawing reference : 8 July 2002 - issue 07

The Spacewire IP Core



- ***Spacewire RX/TX functionality on separate clocks***
- ***FIFO synchronising to AMBA clock***
- ***TX functionality via AHB***
  - Memory mapped (AHB slave)
  - DMA (AHB master) from a linked list of packets in memory
- ***RX functionality via AHB master using ping-pong buffer***

The BLADE Demonstration Board



Future S(C)OC Steps

- ***Specification***
  - Refinement/settling of the specification
  - Adding additional blocks (AOCS/navigation, imaging, signal processing)
  - **User/application feedback required**
- ***Validation***
  - Validation of partial configurations with the BLADE board
  - Validation of a complete system in a larger FPGA
- ***Software***
  - Development of driver libraries for RTOS (VxWorks, RTEMS…)
  - SOC design tool selection (Summit, CoWare, Prosilog, …)
  - Fast simulation models for HW/SW co-simulation
  - Integration with or plug-ins to TSIM (LEON simulator)
- ***Implementation***
  - Mapping to SOC design tools
  - Implementation in a state-of-the art ASIC technology
  - Building up support know-how (industrialisation)
  - Implementation in Actel RTAX devices