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RISC-V Research and Development for Space and Safety Critical Systems at BSC

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Barcelona Supercomputing Center
Centro Nacional de Supercomputación

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- Introduction
- Space-specific and safety-critical developments
- Lagarto: BSC’s open source RISC-V core
- HPC designs with future applicability to space/safety critical systems
- Conclusion

Introduction

- European non-dependence in processors designs and chip making is more relevant than ever
  - HPC-class CPUs and accelerators
  - Microcontrollers and accelerators targeting automotive and other safety critical industries
  - CPUs and accelerators for the space-industry
- ITAR and export control restrictions
- RISC-V presents a unique opportunity to create new royalty-free designs to meet this need

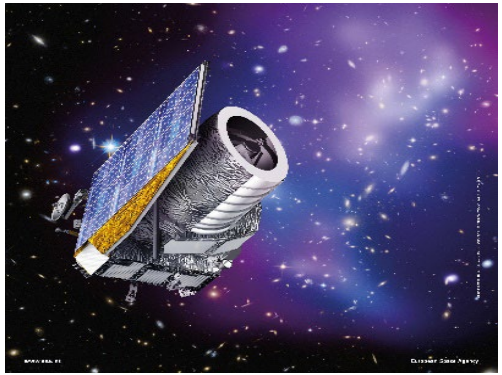
Introduction

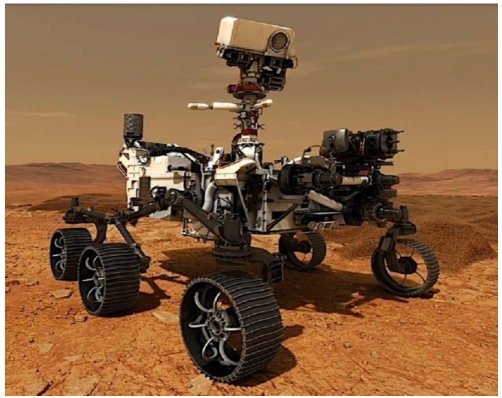
- At BSC we have invested significantly in all these topics, which are developed across many different groups in the Computer Sciences department, in several projects
  - High performance designs for next generation European supercomputers and automotive industry
  - Building know-how in chip design and educating next generation computer architects
  - Designs to increase the performance and the safety of space systems and other safety critical industries
- Several designs released and are going to be released as open source

Contents

Requirements for space designs

- Space is a harsh environment for electronic systems
- Radiation can introduce errors in their operation
- Fault-tolerance is essential for their reliability
- Space processors are simpler than high performance processors and need to be qualified for space use
- Provide limited performance
- Custom designs with very high NRE costs
- Reused for missions across several years/decades





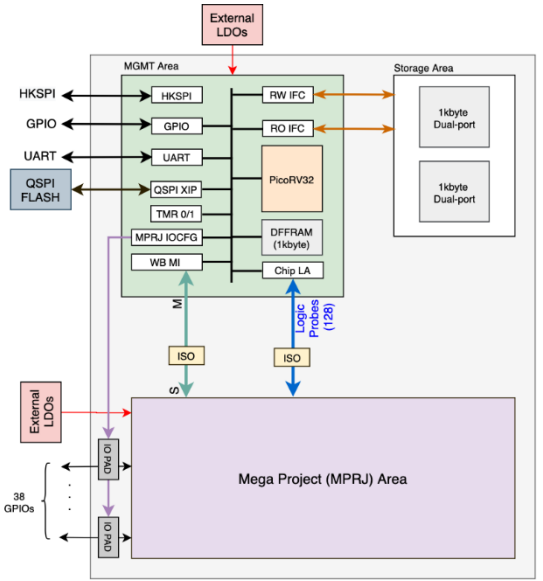
Custom ASIC Designs for Space

- Very high cost, mainly due to the prohibitive cost of commercial EDA tools
- Very low volumes compared to other embedded and safety critical domains
- Only few companies can afford that cost
- Limited innovation potential

- Recently there are several initiatives towards open source hardware
- Government funding for Open Source EDA toolchains:
  - OpenROAD/OpenLANE, CORIOLIS
- Open Source SkyWater 130nm PDK
- Google-sponsored shuttle runs through e-fabless to test the integration of the tools and increase their maturity
- Enable innovation

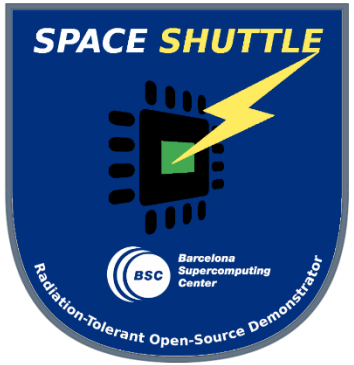
Designed ASICs

- Open Source projects designed for MPW Shuttle Program sponsored by Google on SkyWater 130nm
- Implemented using the open source RTL-to-GDSII OpenLane EDA toolchain
- Designs implemented within a harness RISC-V based SoC called Caravel, provided as part of the MPW
- Packaged chips and a test board for an FPGA to be provided too
- The harness contains a full RISC-V CPU (ibex) and runs the main code.
- This CPU is connected to the user design via:
  - 128 Input logic probes
  - 128 Output logic probes
  - 32 bit wide Wishbone interface
- The user design has 38 GPIOS to interface directly with the outside
- Gradual increase of the complexity of the tape out designs



Space Shuttle

- Characterise the radiation tolerance and reliability of SkyWater 130nm
- Project taped-out in the Open MPW2 Shuttle Program
- Open-source 32 bit, 32 register file with hardware protection
- 4 types of memory protections implemented in the test chip:
  - ECC, 1 bit correction 2 bit detection
  - Triple redundancy
  - Shadow registers
  - ECC Shadow registers
- Redundant performance monitoring unit (PMU) for to enable observability of errors and corrections

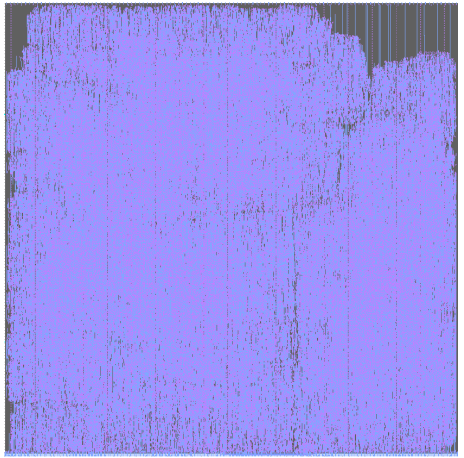


https://github.com/jaquerinte/caravel_radiation_harden

GPU4S esa

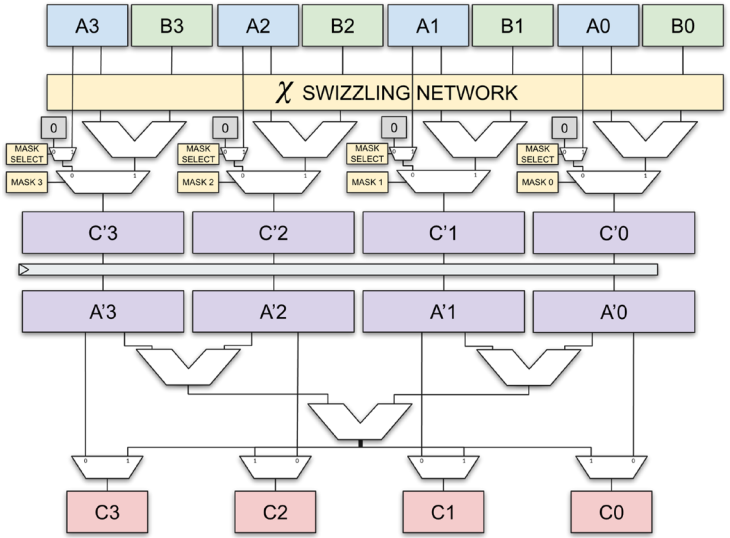
Space Shuttle Results and Evaluation

- Physical Implementation
  - Area: 2.22mm^2 (Out of the available 10mm^2)
  - Total of 75841 SkyWater cells
  - Target Frequency: 100 MHz
  - Verified in RTL and GL simulations
- Sent for tape-out in June 2021
  - Chips expected in December ~~2021~~ 2022
  - Chips will be tested under normal conditions to verify correct functionality
  - Correctly working chips will be evaluated under a series of Radiation Test campaigns (protons, neutrons, heavy-ions) in a co-funded PhD by ESA

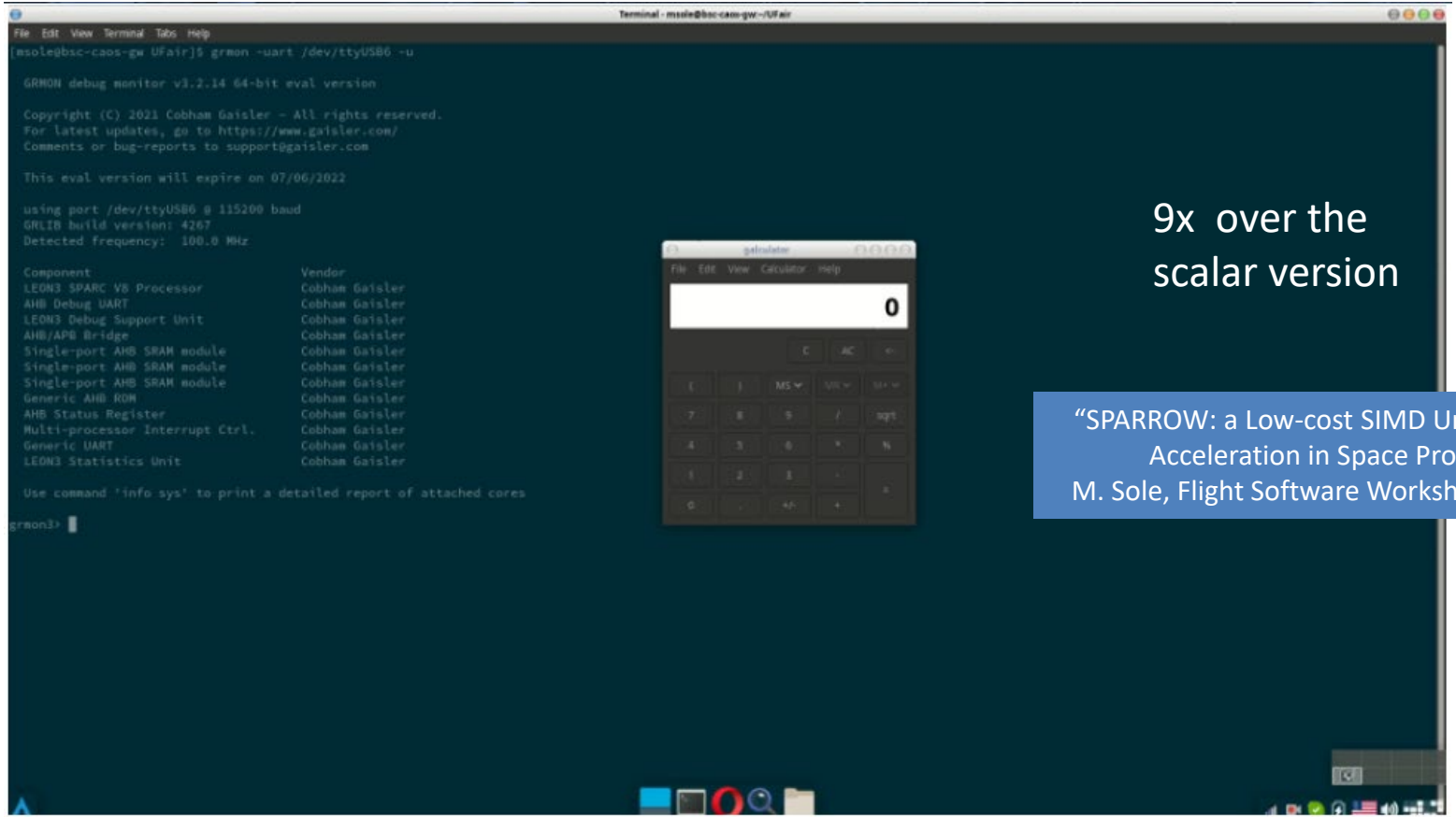


SPARROW: Hw/Sw Co-designed SIMD Unit for AI acceleration

- Increase the machine learning processing capabilities of space processors
- Portable, open source design, integrated with CAES processors NOEL-V (RISC-V) and LEON 3 (SPARC)
- High-performance, Low-cost targeting both ASIC and FPGA implementations, at least 30% smaller than conventional vector processors with similar performance
- Minimal core modifications → incremental qualification
- Key features: reuse of integer register file, short SIMD unit (8-bit), swizzling, reductions
- Collaboration with CAES for commercialisation



Matrix Multiplication Demo on a Xilinx Zynq Ultrascale+ FPGA



9x over the scalar version

"SPARROW: a Low-cost SIMD Unit for AI Acceleration in Space Processors"
M. Sole, Flight Software Workshop 2021

SPARROW Resources and Distinctions

- The hw design and compiler support for gcc and llvm for SPARROW are open source
  - https://gitlab.bsc.es/msolebon/sparrow

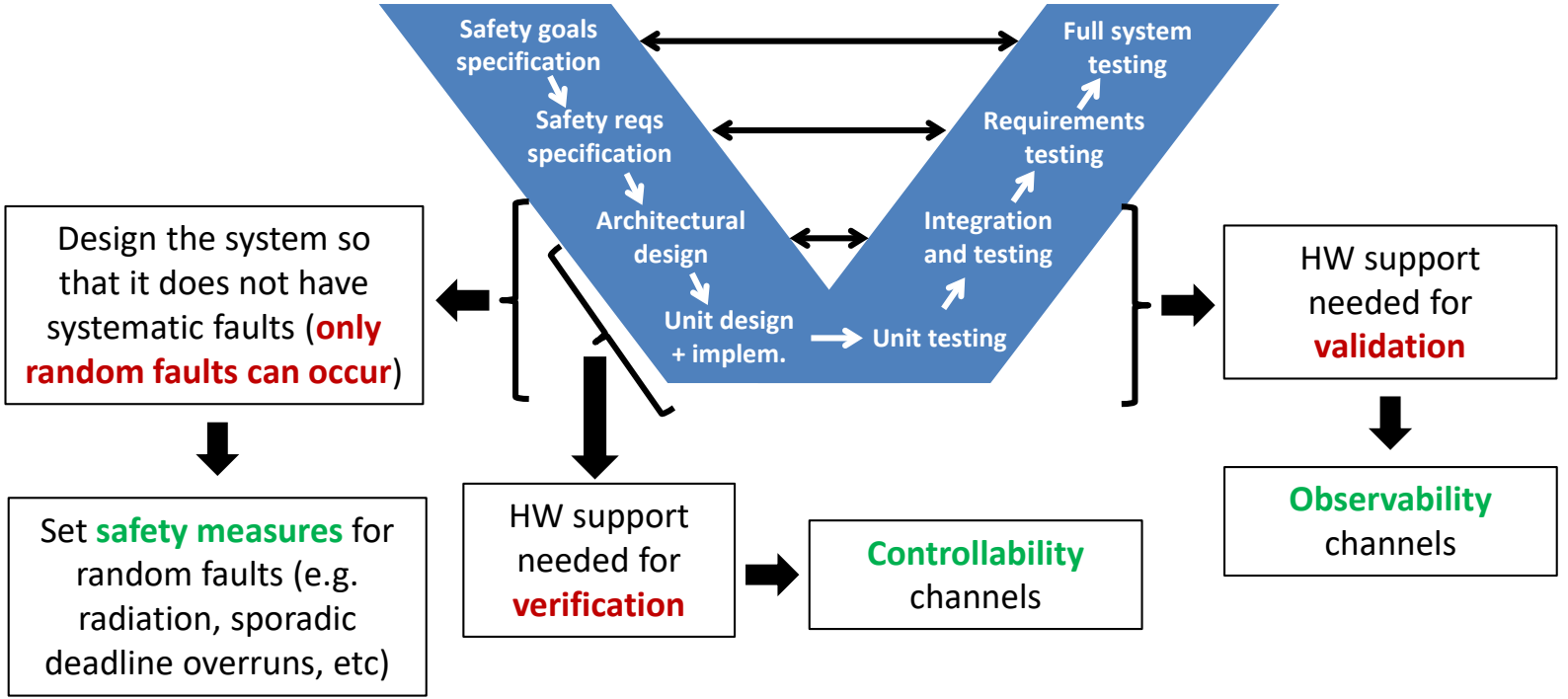
- Winner of the Xilinx Open Hardware 2021 Competition in the student category
  - http://www.openhw.eu/2021

XILINX
UNIVERSITY PROGRAM

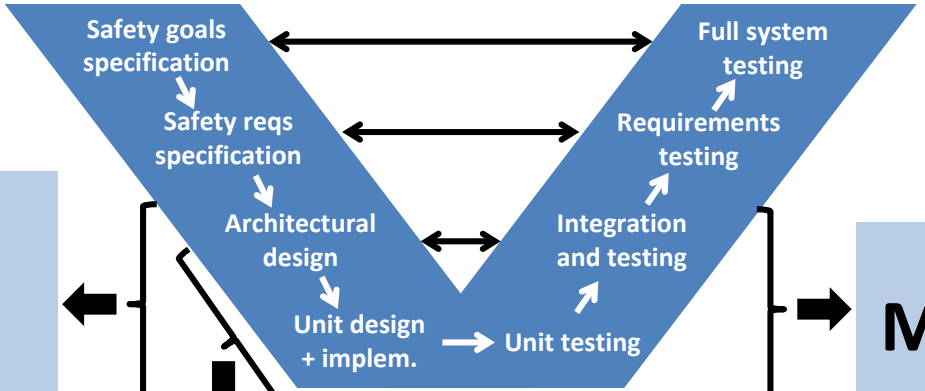
- Best Master's Thesis Project Award 2021, Spanish Chapter of IEEE AESS

- Best Industrial Impact Award in the ACM Student Research Competition of the ESWEEK Conference 2022

Development process of safety critical systems



Development process of safety critical systems



MEANS TO PRESERVE SAFETY DURING OPERATION

MEANS FOR ESTIMATION

MEANS TO EASE TESTING

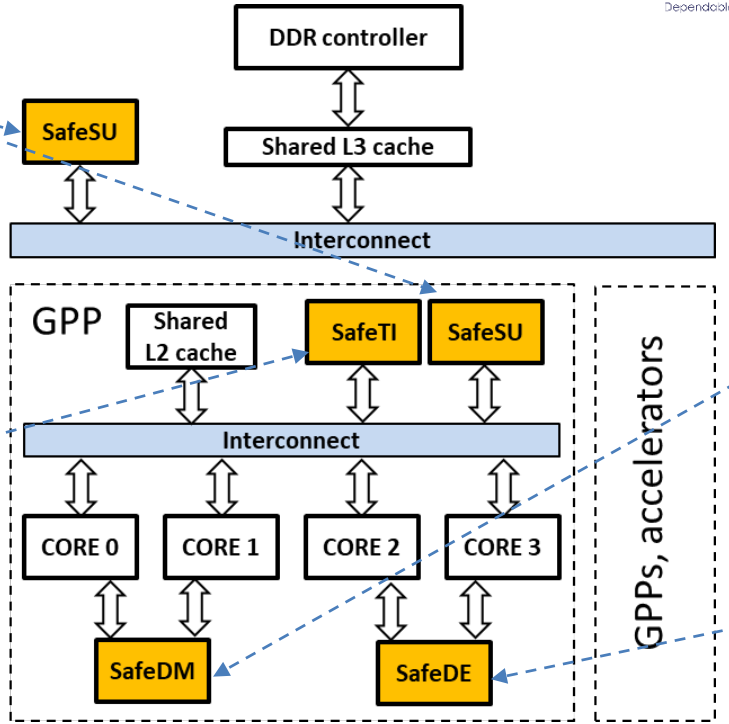
Designs for safety critical systems

De-RISC Dependable Real time Infrastructure for Safety critical Computer

SELENE

SafeSU
Statistics Unit to monitor and control multicore timing interference

SafeTI
Flexible and programmable **traffic injector** to test multicore interference



SafeDM
Module to **measure diversity** across non-native lockstepped cores

SafeDE
Module to **enforce light lockstepping** on non-native lockstepped cores

Current status

SafeSU

- Part of a commercial SoC for the space domain by Cobham Gaisler reaching TRL8 (on FPGA) by Q4-2022

SafeSU, SafeTI, SafeDE, SafeDM

- Part of a multi-domain prototype SoC by Cobham Gaisler reaching TRL5 by Q4-2022

Other targets

- Use of our components in applications with lower criticality (or no critical at all). E.g., some edge applications
- Tailor them for security purposes
- Available at: https://bsccaos.github.io/
- Actively participate in the **RISC-V SIG-Safety group**

Other less mature/work in progress developments

- Several Time-Randomised RISC-V processors for WCET using Measurement Based Probabilistic Timing Analysis (MBPTA)
  - Random placement caches
  - Upper bounding of resources with low jitter
  - Front-end performance improvements
- Binary Neural Network accelerator for space processors using TASTE for the software stack
- Various Dual and Triple lockstep RISC-V processors
- Time predictable multithreading RISC-V processors
- Open Source RISC-V Based GPU with ECC protection and MBPTA support
- Microcontrollers with vector processing (within the core and vector accelerator)

UPC
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"Educating the computer architects of tomorrow's critical systems with RISC-V "
L. Kosmidis, RISC-V Summit 2020

RISC-V®

RISC-V Educator of the Year Award 2019

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Lagarto

- First open-source core developed in Spain
- Academic, RISC-V 64IMA, Single issue, FPGA and ASIC, AXI bus
- Linux capable
- Designed by BSC, IPN, UPC, CNM
- To be open sourced soon

DRAC

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Instituto Politécnico Nacional

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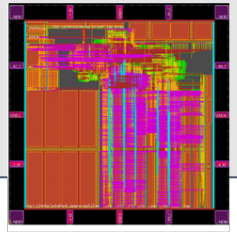
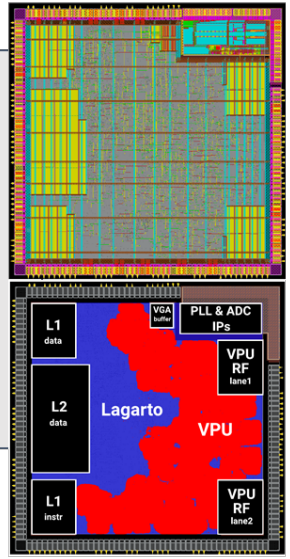
Lagarto RISC-V Planned Tapeouts

2019 2020 2021 2022 2023

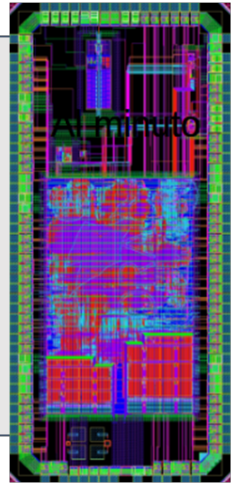
Lagarto (May'19)
- Lagarto Hun 5-stage in-order
- 150MHz (external)
- TSMC 65nm
- 2.5mm2



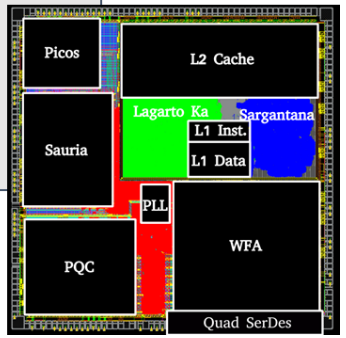
DVINO (Apr'21)
- Lagarto Hun in-order
- VPU
- PLL 600 MHz
- SDRAM mem cont
- HyperRAM
- VGA
- ADC
- TSMC 65nm
- 8mm2



Sargantana (Feb'22)
- Sargantana 7-stage in-order
- PLL 1.2 GHz
- Custom extensions
- SDRAM
- Prototype analog IPs: SerDes 8GHz
- GF 22nm
- Area: 2.9mm2

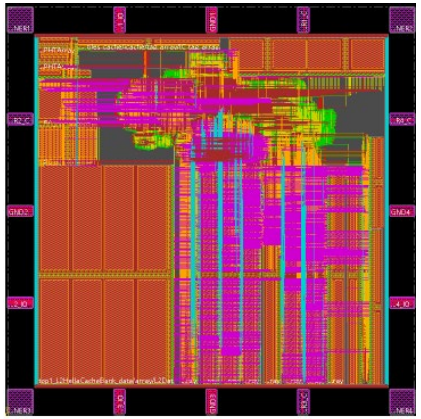


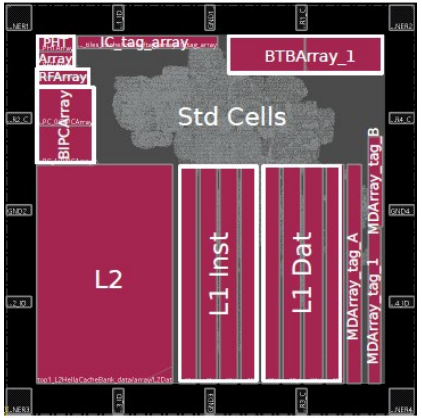
Kameleon (Dec'22)
- Lagarto Ka ooo
- PLL 1.2 GHz
- Automotive Accel
- Crypto Accel
- Genomic Accel
- PICOS Accel
- SerDes 8GHz
- GF 22nm
- Area: 9mm2



Lagarto: First RISCV Tapeout (2019)

- Target design:
  - Lagarto Hun in-order scalar core, 5 stages, single issue, RV64IMA
  - 16KB L1 caches, 64KB L2 cache, TLB
  - Memory controller on the FPGA side via packetizer
  - Debug ring via JTAG
  - Target technology: TSMC 65nm, area fits in 2.5mm2
- Fabrication and bringup
  - Submitted in May 2019
  - Samples received in Sep 2019
  - Bringup with custom PCB in Oct 2019
  - Linux boot in Dec 2019





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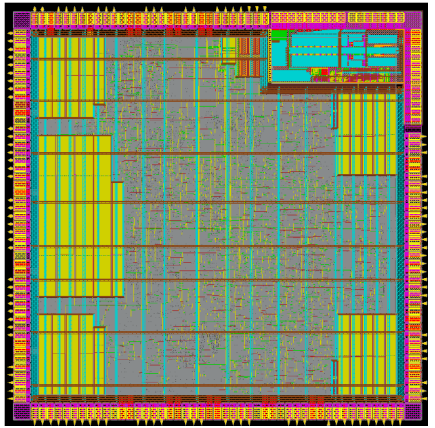
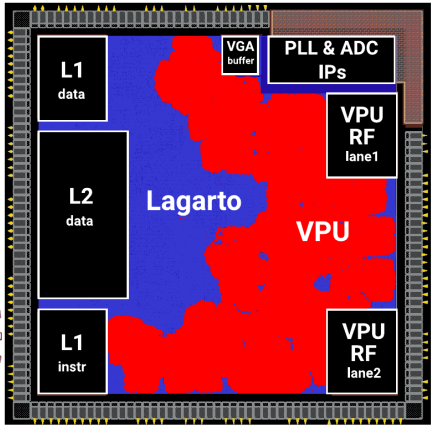
Centro Nacional de Microelectrónica
IMB

IPN

DVINO: 2nd Lagarto Tapeout (2021)

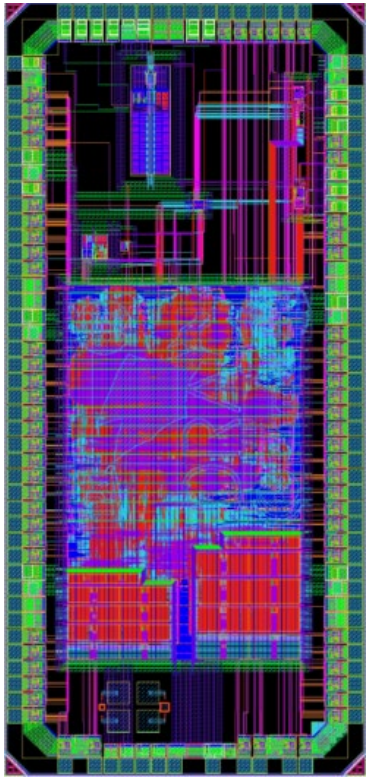
- DRAC Vector IN-Order (DVINO) processor details:
  - Lagarto Hun scalar pipeline, 5-stage, in-order, RV64IMA
  - Hydra 2-lane (VPU-DRAC-1.0), 4096-bit vector length
  - Internal PLL. DVINO can run at 600, 400, 300 and 200MHz
  - In-house L1 instruction cache and PMU
  - L1 data and L2 caches from lowRISC 0.2
  - Multiple contr: JTAG, UART, SPI, VGA, SDRAM and Hyperram.
  - In-house JTAG-based debug-ring
  - Technology node: TSMC 65nm (Europractice)
  - Area: 8.6mm2



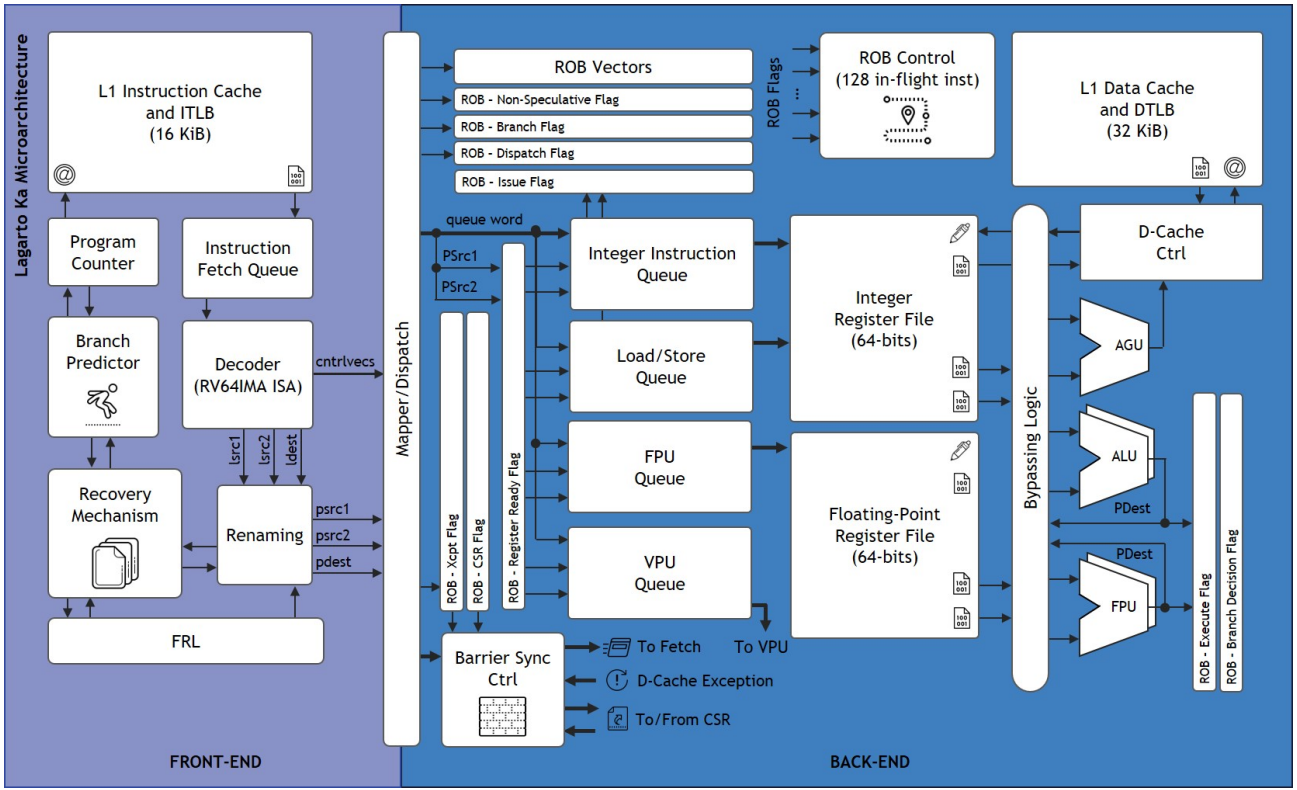


Sargantana Tapeout (Feb 2022)

- Sargantana in-order processor details:
  - Lagarto Hun pipeline, 7-stage, in-order, RV64IMAFD (RV64G)
  - Support for floating point operations (single and double precision)
  - Integer SIMD VPU, 128-bit vector length, custom instructions
  - Internal PLL. Sargantana can run above 1.1GHz
  - In-house L1 instruction cache and PMU
  - L1 data and L2 caches from lowRISC 0.2
  - Multiple controllers: JTAG, UART, SPI, SerDes, and Hyperram
  - In-house JTAG-based debug-ring
  - Technology node: GF 22nm (Europractice)
  - Area: 2.9mm2



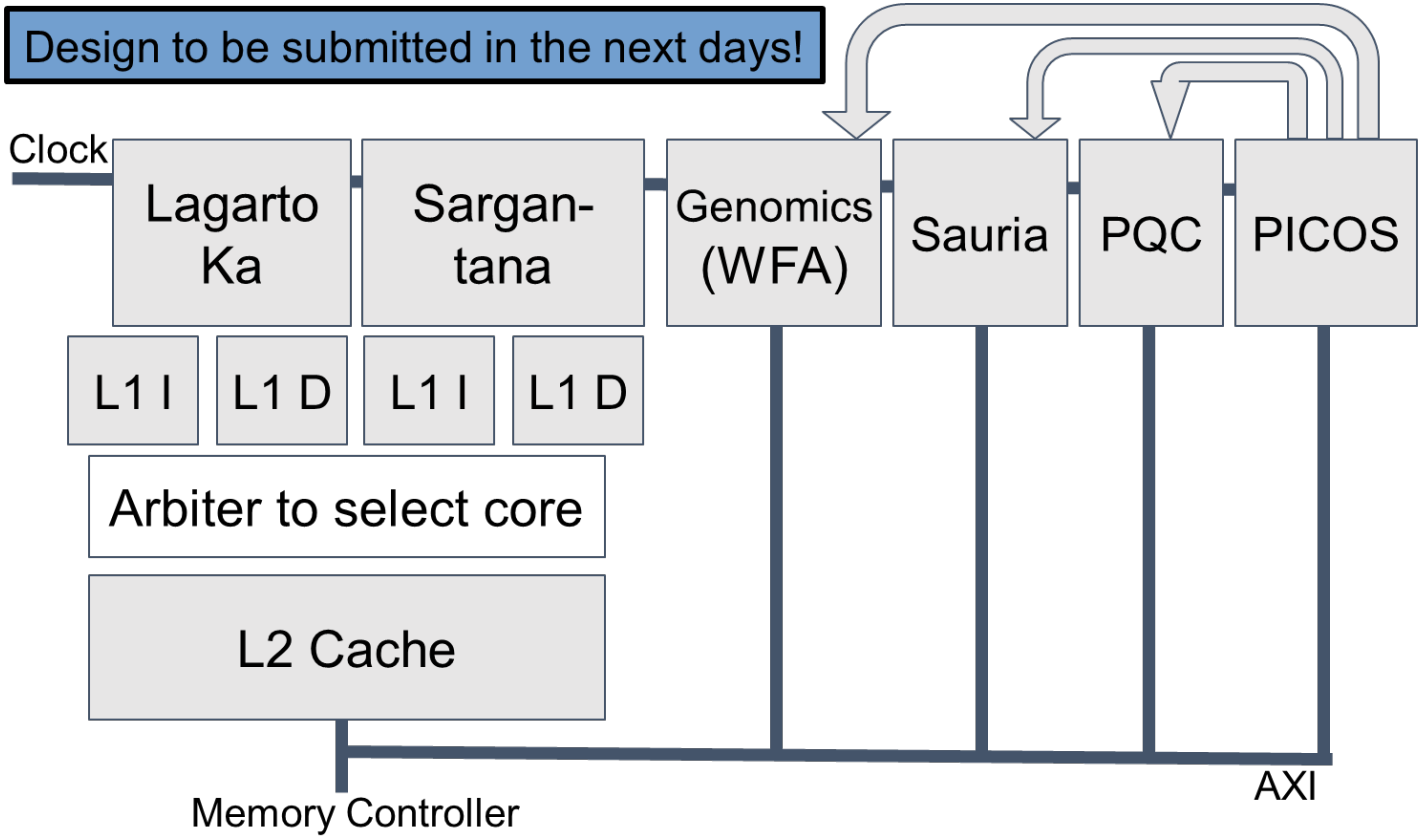
Lagarto Ka out-of-order core

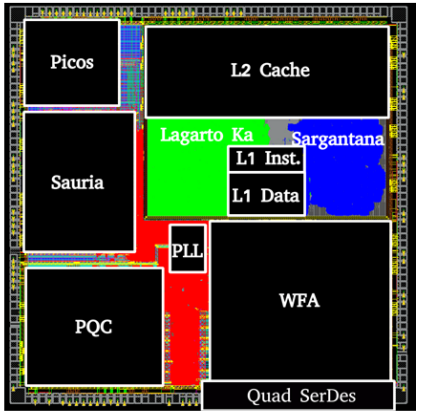


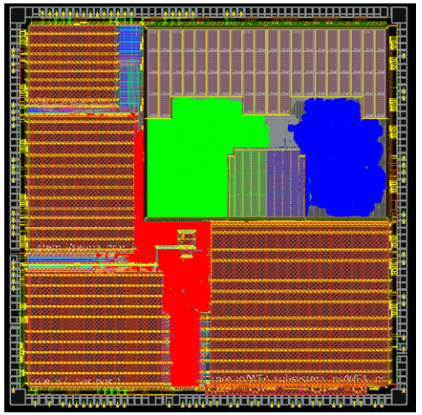
- 2-way 64-bit out-of-order architecture
- RV64IMA ISA
- 11-stage pipeline implementation
- Parameterized branch predictor:
  - BTB 16-128 entries
  - BHT 16-128 entries
  - RAS 2-8 entries
- ROB 128-entries
- Low-power Integer queue (out-of-order issue)
- In-order Load/Store Queue
- Hit-under-miss support
- Configurable, L1 caches
  - 16 KiB L1 I-cache (Typical)
  - 32 KiB L1 D-cache (Typical)

Kameleon Tapeout (Dec 2022)

Design to be submitted in the next days!







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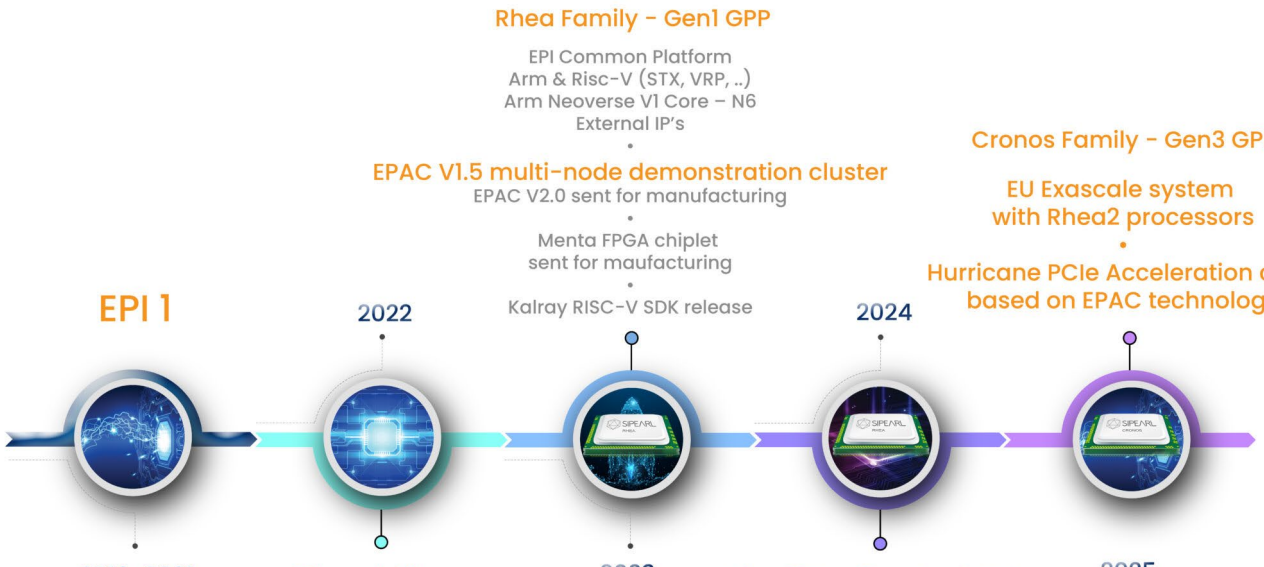
European Processor Initiative

- Development of European Supercomputing Technologies which can be used later in other strategic EU industries such as automotive

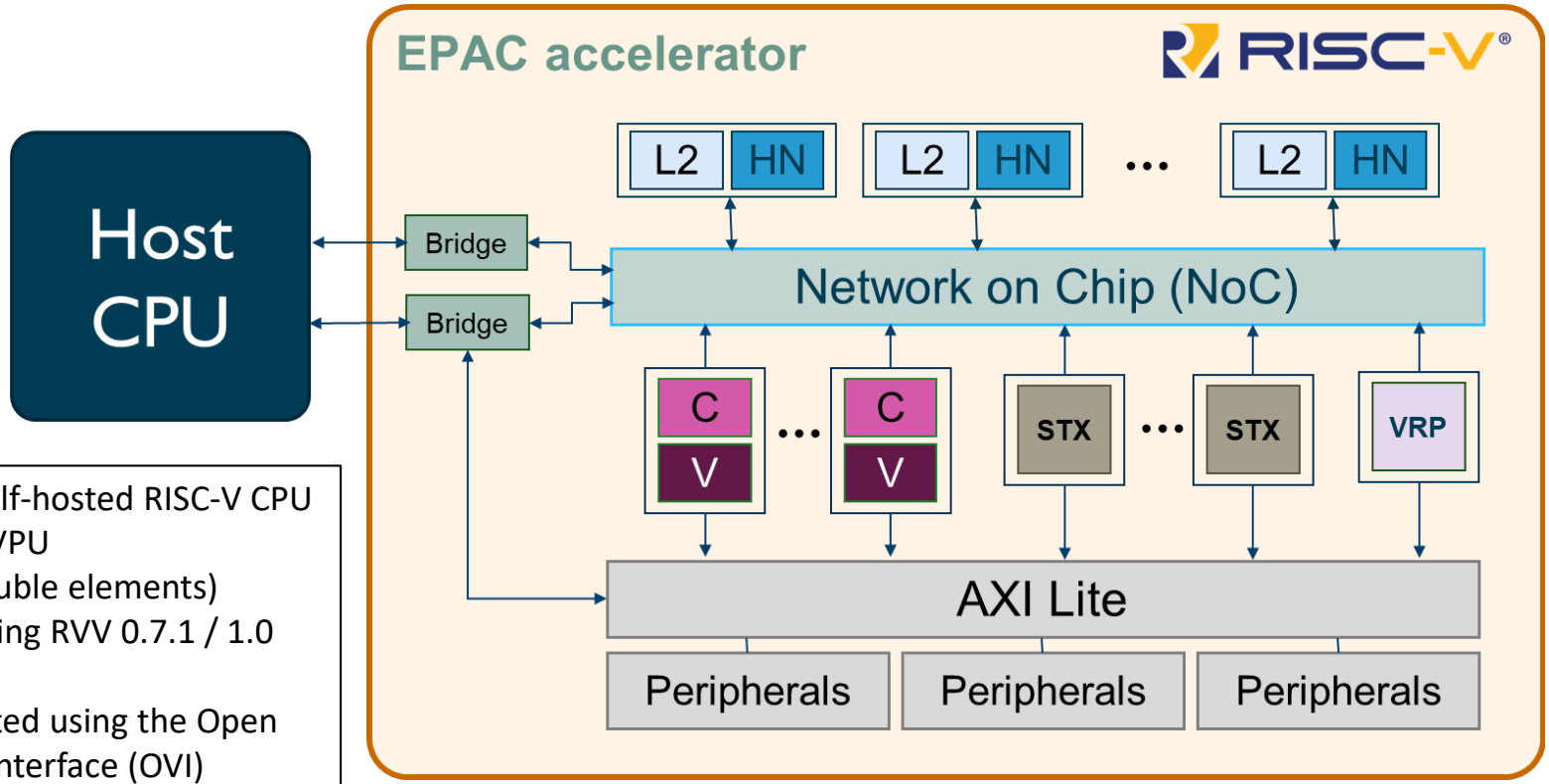
- Organised in 3 streams
- Stream 1 Software and Benchmarking
- Stream 2 General Purpose Processor
- Stream 3 - EPI Accelerator (EPAC)
  - RISC-V based
  - EU design: BSC. Semidynamics, EXTOLL, FORTH, ETHZ, UniBo, Chalmers, …

European Processor Initiative (EPI) - Timeline

European Processor Initiative



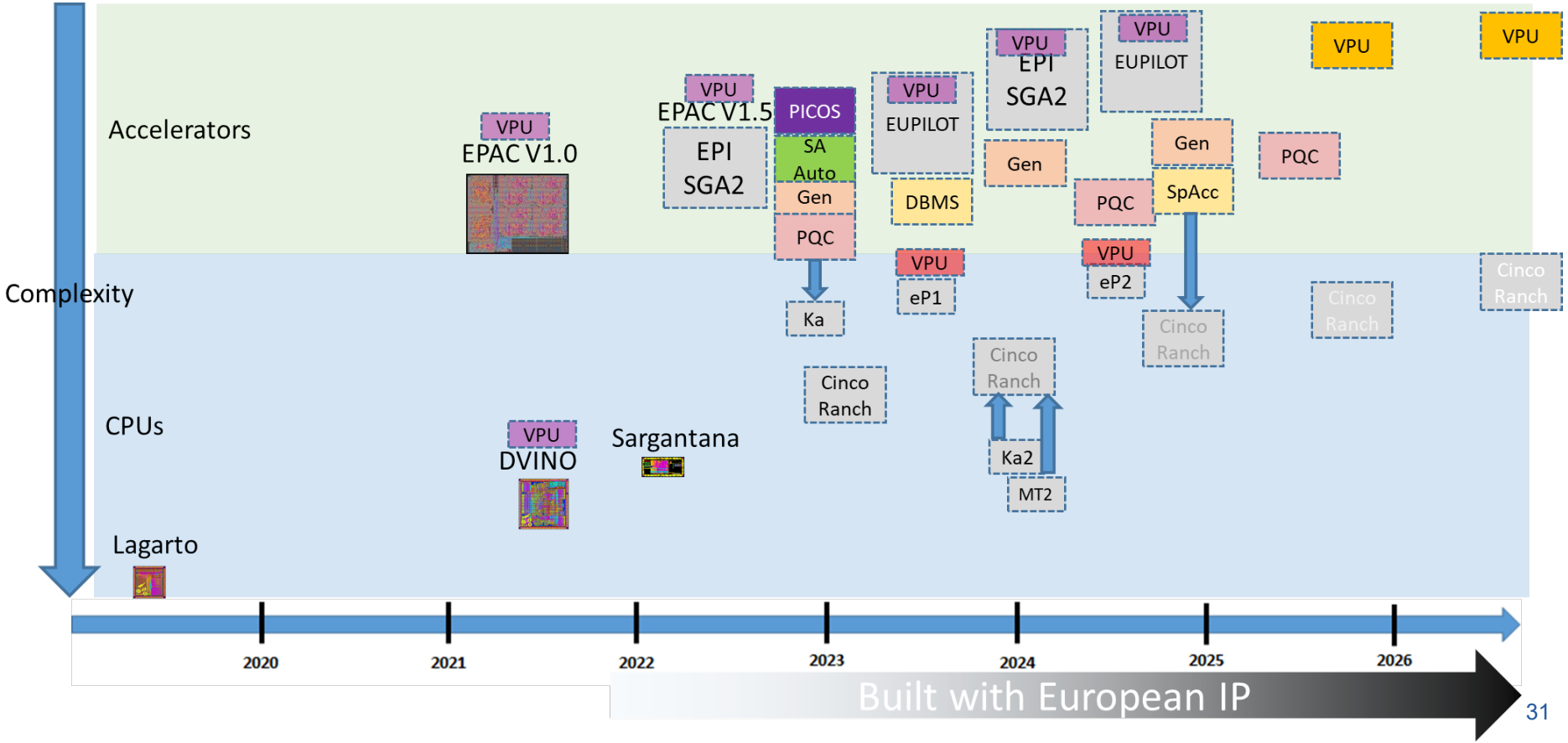
EPAC: a RISC-V accelerator



VEC - Self-hosted RISC-V CPU + wide VPU (256 double elements) supporting RVV 0.7.1 / 1.0

Connected using the Open Vector Interface (OVI)

Extended BSC Chip Roadmap



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Conclusion

- RISC-V and open hardware initiatives allow to design and experiment with many different types of design
- Several RISC-V developments are on going at BSC
  - Particular focus on Space and safety critical domains
  - Open source RISC-V core and tape-outs
  - HPC developments which can be applied to safety critical systems in the future
- Several developments are already open source or are going to be released soon

Acknowledgements

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- All funding agencies which supported these developments


Thank you!
Questions?
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