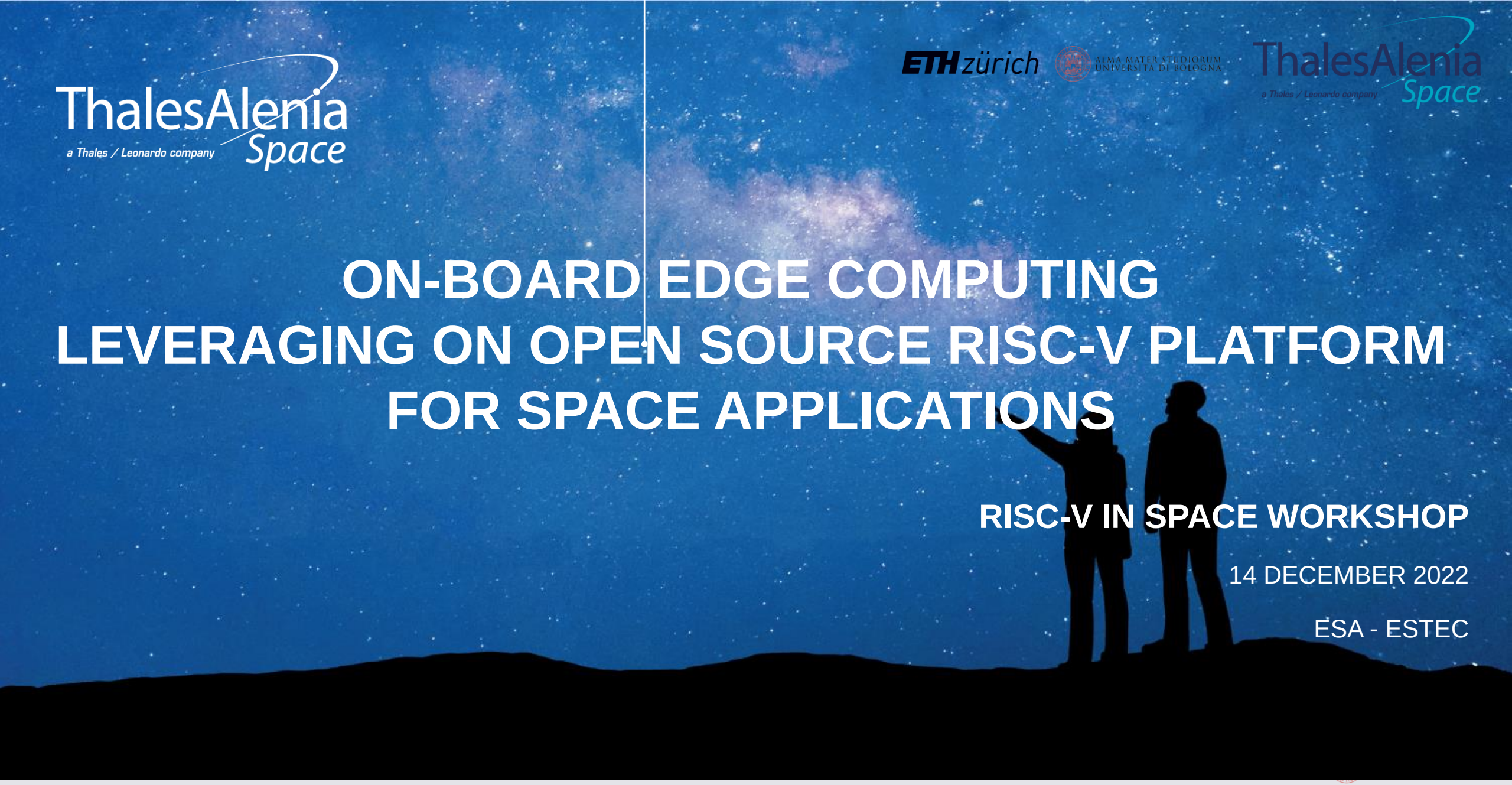

# ON-BOARD EDGE COMPUTING LEVERAGING ON OPEN SOURCE RISC-V PLATFORM FOR SPACE APPLICATIONS

## RISC-V IN SPACE WORKSHOP

14 DECEMBER 2022

ESA - ESTEC



**Date:** 25/07/2022
**Ref:** TAS/EU/PRP/021-2021
**Template:** 83230347-DOC-TAS-EN-008

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# SUMMARY

- RISC-V introduction in Space ecosystem
- Examples of targeted high performance and edge computing applications:
- TAS RISC-V foreseen and ongoing activities
- RISC-V configuration under study, description and scalability



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**Ref:** 0005-0008238691
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# RISC-V IN SPACE : CONTEXT

- European space community has a strong heritage in using “Open ISA” processors
  - SPARC processors have been successfully used for on-board applications in the last twenty years
  - But the development of the SPARC processors is now losing momentum in industry…
- Looking for SPARC processor replacement, the upstream question is whether is it convenient and possible to remain “Open ISA” or is it rather convenient to embrace some commercial solution (e.g. ARM)?
  - RISC-V is currently perceived like the most credible “Open ISA” solution for the next years
- Perceived advantages of the “Open ISA” approach (and RISC-V architecture in particular) include:
  - No license fees
  - Complete access to design internals, e.g. for tailoring and qualification purposes
  - Synergy with the Open community (not only industry but also research centres, academia…)
  - Suitable for high performance computing capabilities (e.g. massive signal processing or deep neural networks) to support edge computing applications
- Perceived challenges:
  - Match the performance of state of the art solutions, often based on commercial solutions


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# RISC-V IN SPACE : EDGE COMPUTING

- One axis of improvement of the space systems capabilities is the ”edge computing” paradigm, which is to move the processing close to the source of the data. This introduces many advantages:
  - Processing on-board reduces the amount of data to be exchanged between Ground and Board
  - Reduce the response time to changes in scenarios (avoid the board-ground loop)
  - Increases On Board autonomy and reduces workload on ground

- We report in the following a limited collection of “edge computing” use cases currently identified and under study by TAS:
  - SAR Focusing
  - Formation Flying
  - Security Aspects
  - Signal Processing for Telecommunications: Software Defined Radio
  - Machine Learning for Failure Detection


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# USE CASE: ON BOARD PROCESSING FOR SAR FOCUSING

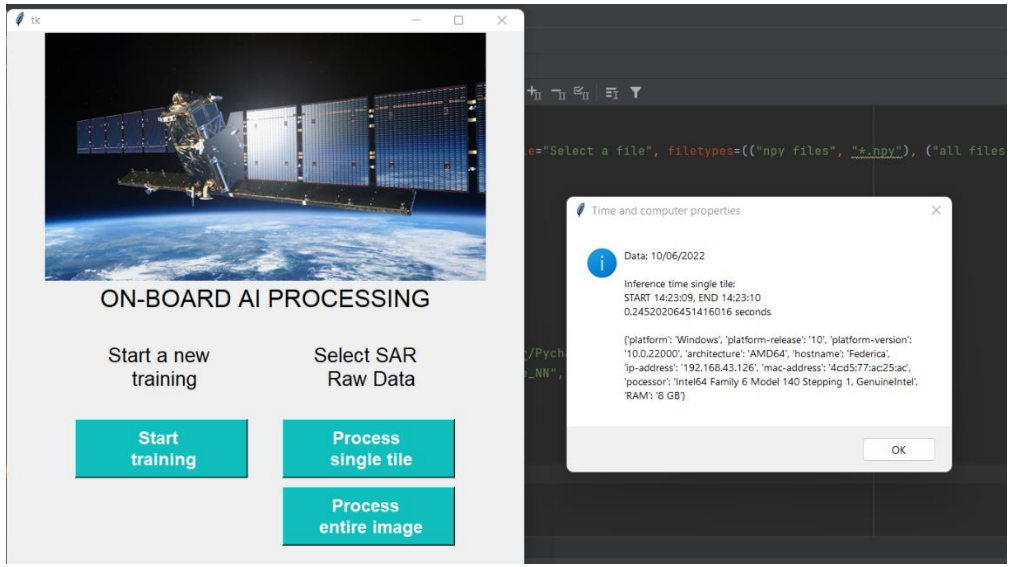
/// Processing of SAR RAW DATA on board will enable new kind of Real and Near Real time mission

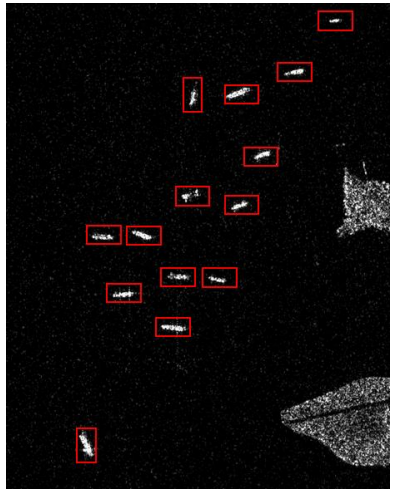
/// Possibility of using AI-based algorithms to improve the autonomy and the efficiency of the on-board management of payload data:

/// Use of AI for **detection of target**

/// Use of AI for **change detection**

/// Use of AI for **data compression**





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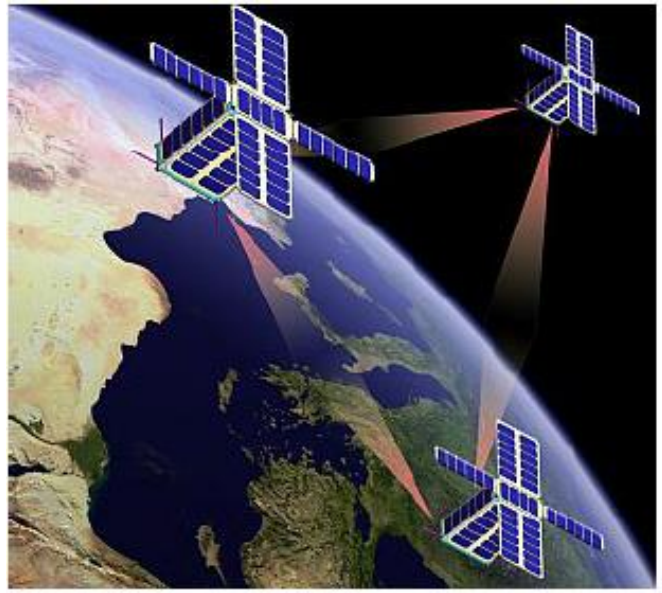
# USE CASE: ON BOARD PROCESSING FOR FORMATION FLYING

///Formations Flying systems can benefit AI in terms of:

- **Formation control**:
  - Maintenance
  - collision avoidance
  - formation change

- **Distributed processing** among the nodes



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# USE CASE: ON BOARD PROCESSING FOR SECURITY ASPECTS

///System Security can benefit from AI:

- **Anti-jamming** for satellite mission
- **Detection of threats** and countermeasures
- **Chiphering** data with AI
- **Prevention** of attacks




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# USE CASE: SOFTWARE DEFINED RADIO (SDR)

/// The main advantages offered by Software Defined Radios (SDRs) over traditional digital radio equipment are:

- The ability to alter the functionality and the architecture of the signal processing chain by uploading and running new software
- The possibility of adaptively choosing algorithm parameters and operating frequencies based on arbitrary conditions
- The reduction of required analog hardware, resulting in the simplification of radio architectures and their cost

/// In addition, the capabilities of modern computing platforms and the availability of advanced development tools allow the deployment of advanced functionalities directly on-board:

- Interference identification using machine-learning techniques
- Adaptive digital beam-forming



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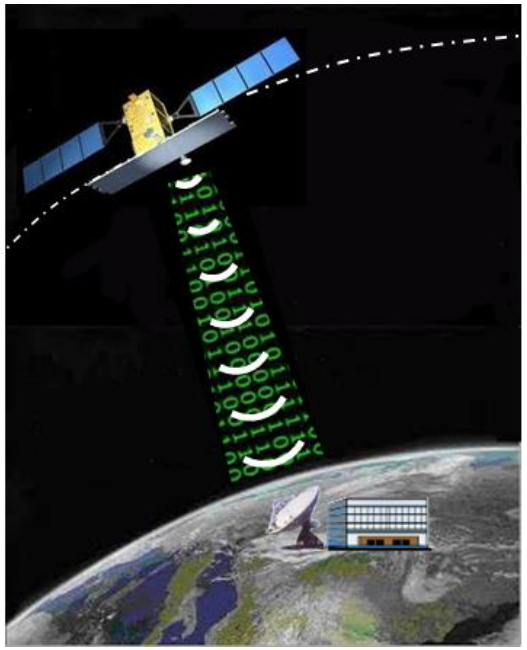
# USE CASE: SATELLITE FDIR

## ///Satellite health monitoring

- In space systems it's crucial that spacecraft operates in nominal conditions
- On board equipment generate large amount of data transferred to ground-based data centers for spacecraft health monitoring
- Major trends:
  - Use of smarter algorithms to improve the prevention and the detection of failures
  - Edge computing: move computation closer to the source of data in order to improve reaction time and (if possible) to reduce the amount of data transferred to ground
  - Adopting heterogeneous architectures to improve performances, to optimize power efficiency and to simplify the system by putting many functions in a single unit.





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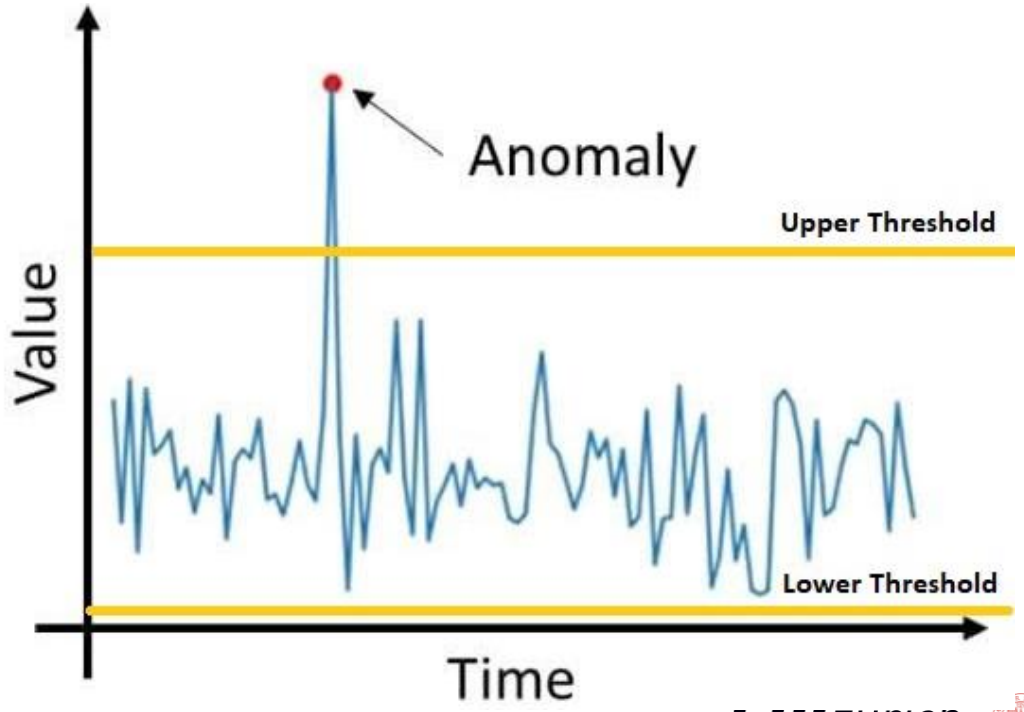
# USE CASE: SATELLITE FDIR TRADITIONAL APPROACH

## ///FDIR Traditional approach

- Traditional Out-Of-Limits (OOL) approach for Anomaly Detection uses upper and lower thresholds, if telemetry data exceeds the limits an alarm is triggered. FD(IR) is based on simples tables containing threshold values defined using expert knowledge

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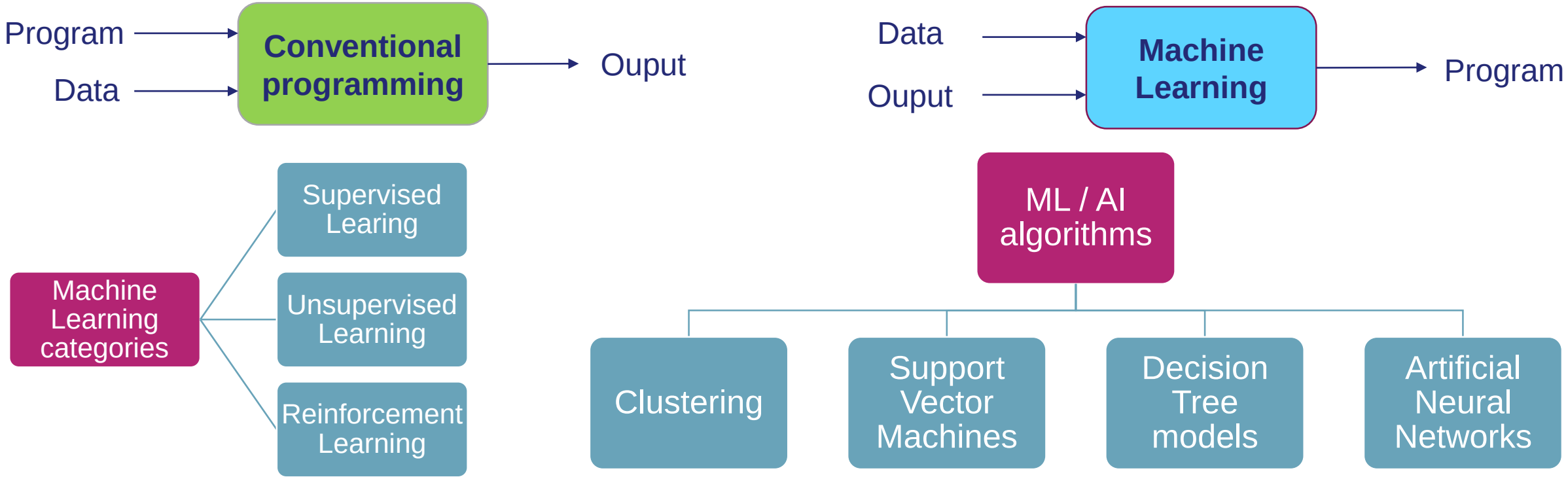
# USE CASE: SATELLITE FDIR NEW APPROACHES (ML/AI TECHNIQUES)

- machine learning algorithms build a mathematical model based on sample data, in order to make predictions or decisions without being explicitly programmed to perform the task
- Thales Alenia Space Italia S.p.A. (TAS-Italia), in collaboration with University partners (Alma Mater Studiorum - Università di Bologna, etc.) is considering ML-based solutions for **onboard development** for incoming and future space missions (ESA, ASI, etc.)



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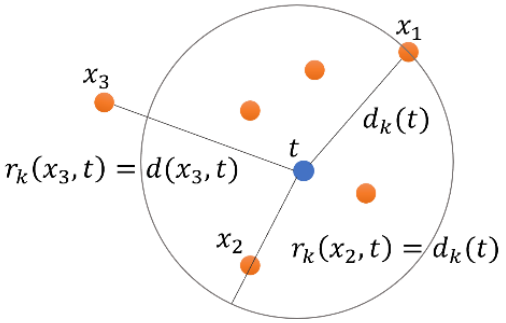
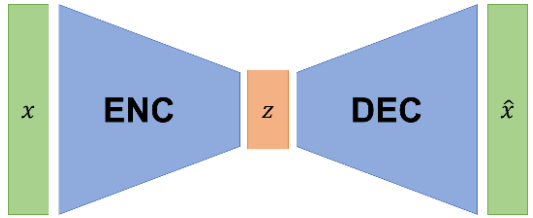
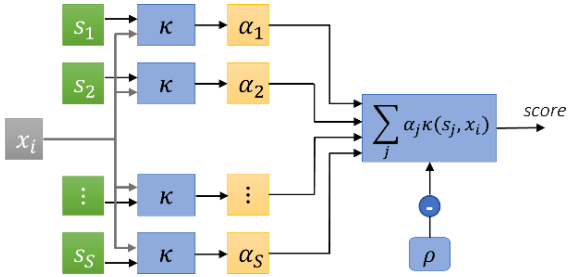
# USE CASE: TAS-I ENHANCED FDIR

We focused on four possible detectors which differ in the concept of similarity they rely on:

- **Proximity-based method**: Local Outlier Factor, LOF, combines the k-nearest neighbours learning method with some data-dependent similarity measure to address the issue of local density variation
- **Linear method**: Principal Component Analysis, PCA, which find the called principal components, which are a set of m < n vectors along which the energy of the input signals concentrates in average.
- **Non-linear method (1):** Autoencoder, AE, generalization of PCA encodes some meaningful information extracted, by non-linear projection of the input observation $x_i$, into a manifold living in a lower dimensional space $z_i$
- **Non-linear method (2):** One-class Support Vector Machine, OCSVM, allows to find a hyperplane or hypersphere separating the single-class normal data examples from the origin with maximal margin ρ.



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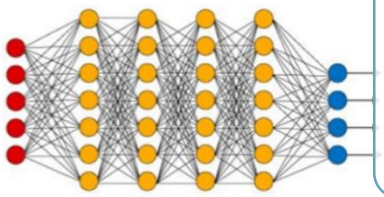
# TAS-I Enhanced FDIR  further developments

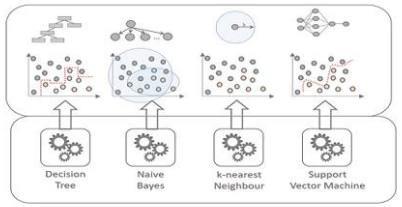
- As a rule of thumb, the performances of the algorithm increases with the number of layers, the complexity of the algorithm and the number of parameters.
- The current state of the art hardware (CAES GR740) for RAD-Hard processors is able to run algorithms with medium-low computational complexity. ML Algorithms based on DNN and Ensemble learning needs more performing solutions.
- Techniques based on the multivariate analysis are currently not feasible because their complexity is not compatible with the RAD-hard processors computational power.

**Deep Neural Networks**



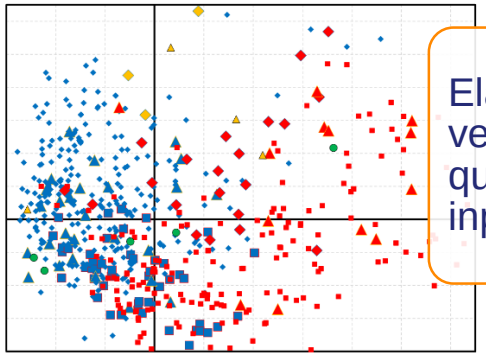
include tens or hundred of layers

**Ensemble Learning**




Combine multiple techniques

**Multivariate analysis**



Elaborate very high quantity of input data



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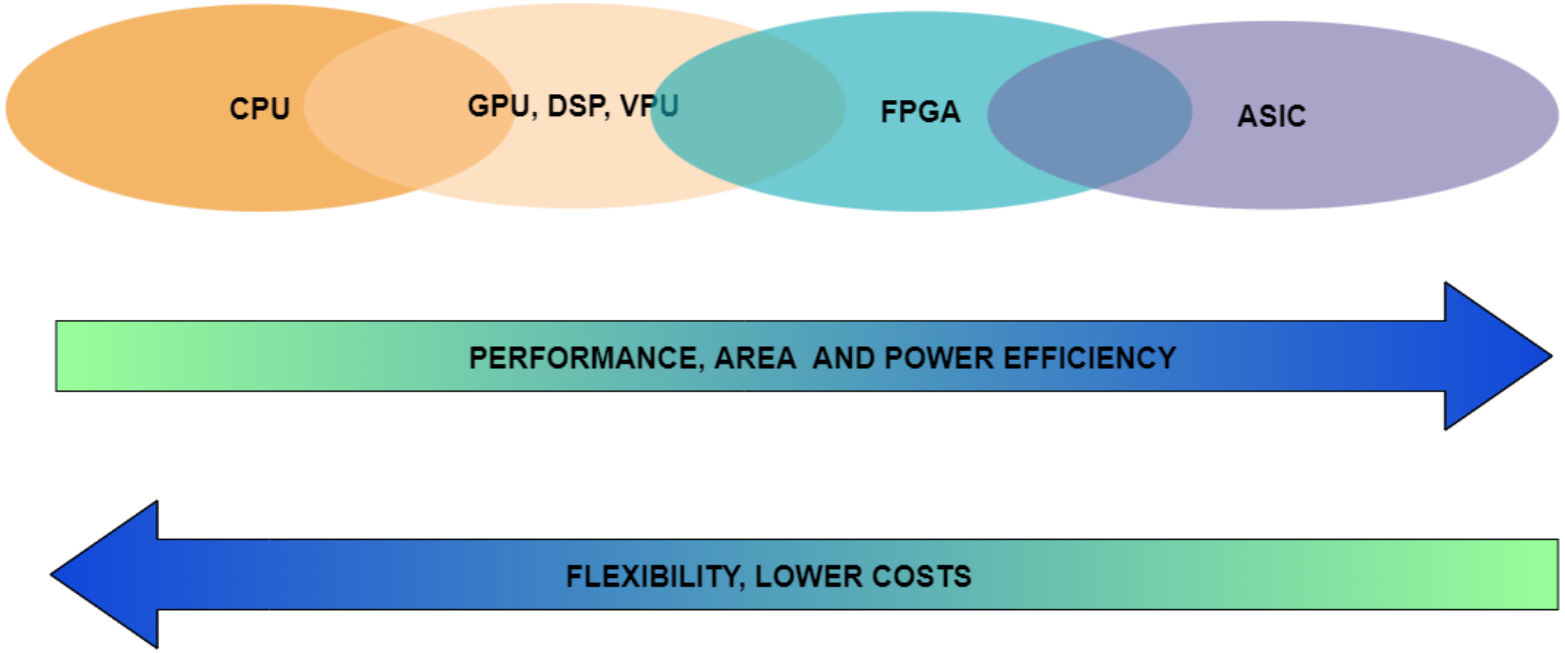
# TASI-I Hardware exploration

- The state-of-the-art CAES GR740 provides about 450 DMIPS per core that, even in the context of FDIR, may be not enough for the more complex algorithms (Enhanced FDIR) and scenarios.
- Signal processing algorithms and ML techniques for image recognition and classifications are far more demanding
- Many HW solutions are available based on different architectures and optimized for different trade-offs. The main factors taken into account are:
  - Power efficiency
  - Performances
  - Scalability




- TAS-I is exploring the development of an heterogenous SoC accelerator based on RISC-V ISA and the PULP platform combining excellent performances and power efficiency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# TAS RISC-V ONGOING AND PLANNED ACTIVITIES

- TAS and *Università di Bologna* are currently performing one PhD with the objective to assess the suitability of the PULP architecture for space applications, and its porting to space systems.
- TAS-I interest in the RISC-V development is underlined by the involvement in recently approved **ISOLDE** project, part of the Key Digital Technology Joint Undertaking (KDT JU) program
  - ISOLDE is a joint project carried out by 41 European entities (companies, universities and research centers), including TAS-I, for the "*Design of Customisable and Domain Specific Open-source RISC-V Processors*"
  - Subdivided in national clusters, Italy cluster consist in a space use case
  - The goal is to design a high performance RISC-V space processor, in order to move the processing capabilities close to the sensor
  - A demonstrator for space use case will be developed, where applications like enhanced FDIR and ML-based data classification of EO data will be used for benchmarking

KDT

ISOLDE
Space

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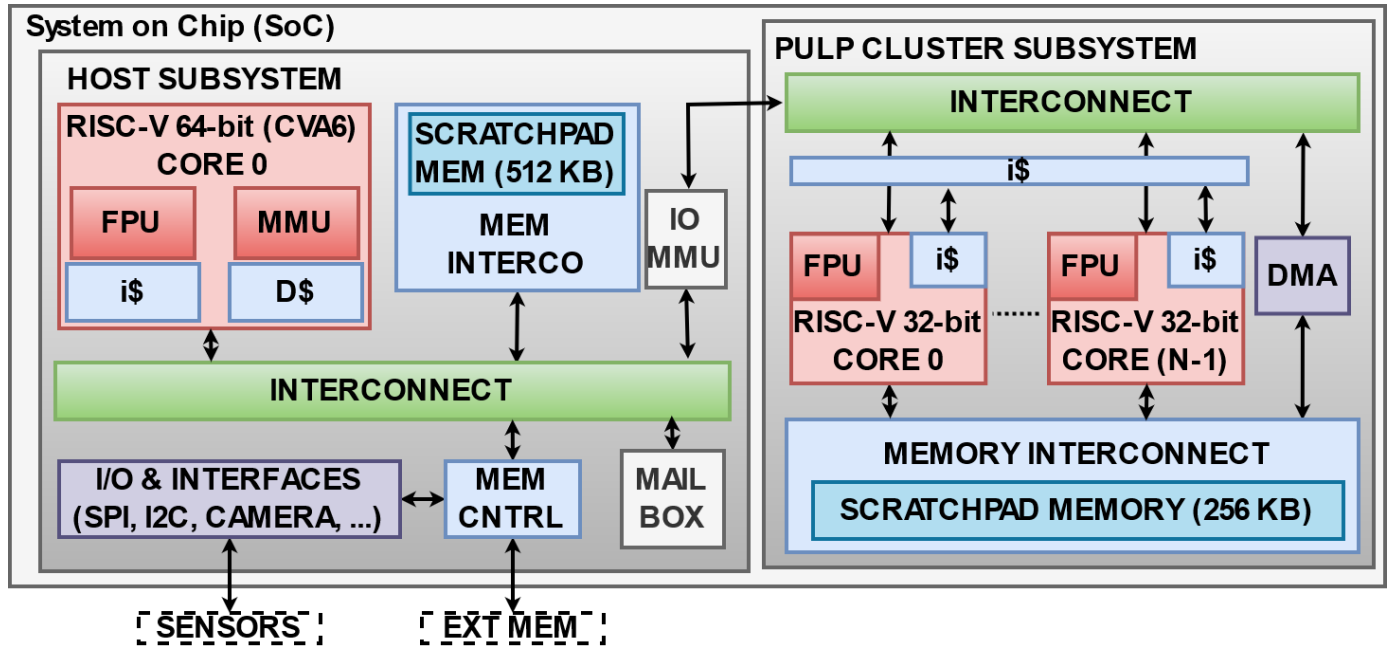
# Heterogeneous SoC for Space Applications

- Heterogeneity leaves space for scalability
- Two main scaling directions:
  - Multicore host subsystem for powerful real-time executions
  - Multicluster (parametric number of cores per cluster). Chiplet-based solution for extreme performance and energy efficiency
  - Multicore host + multicluster: real-time applications for extreme performance and energy efficiency



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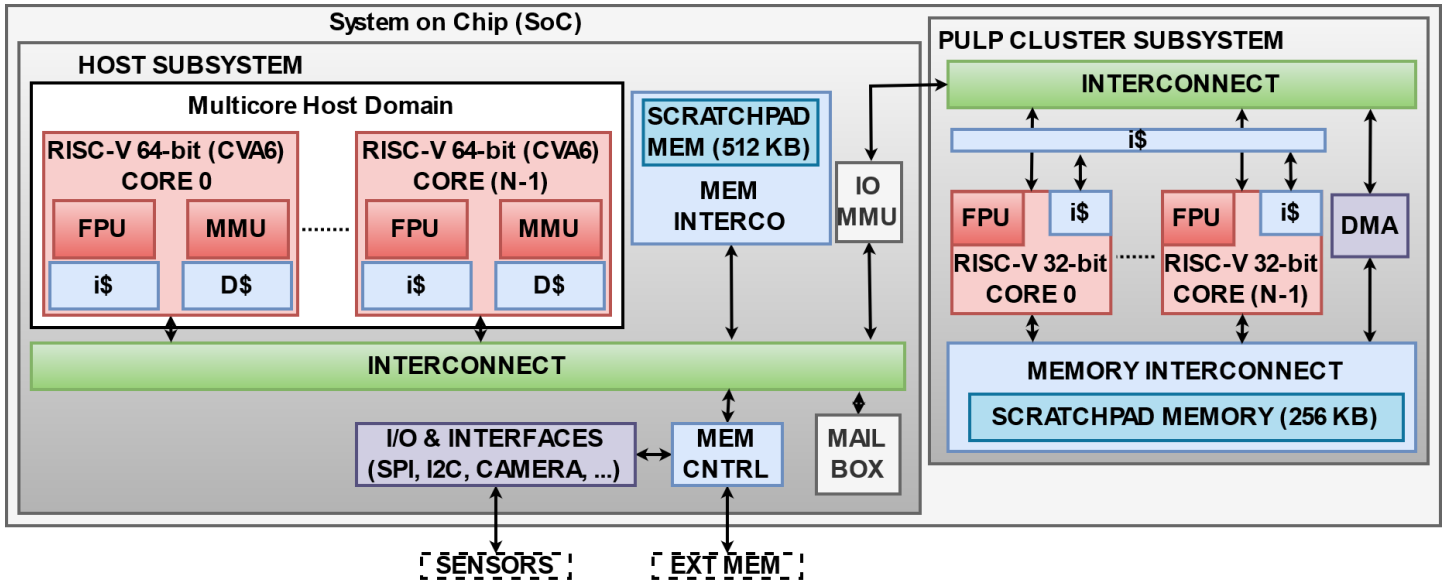




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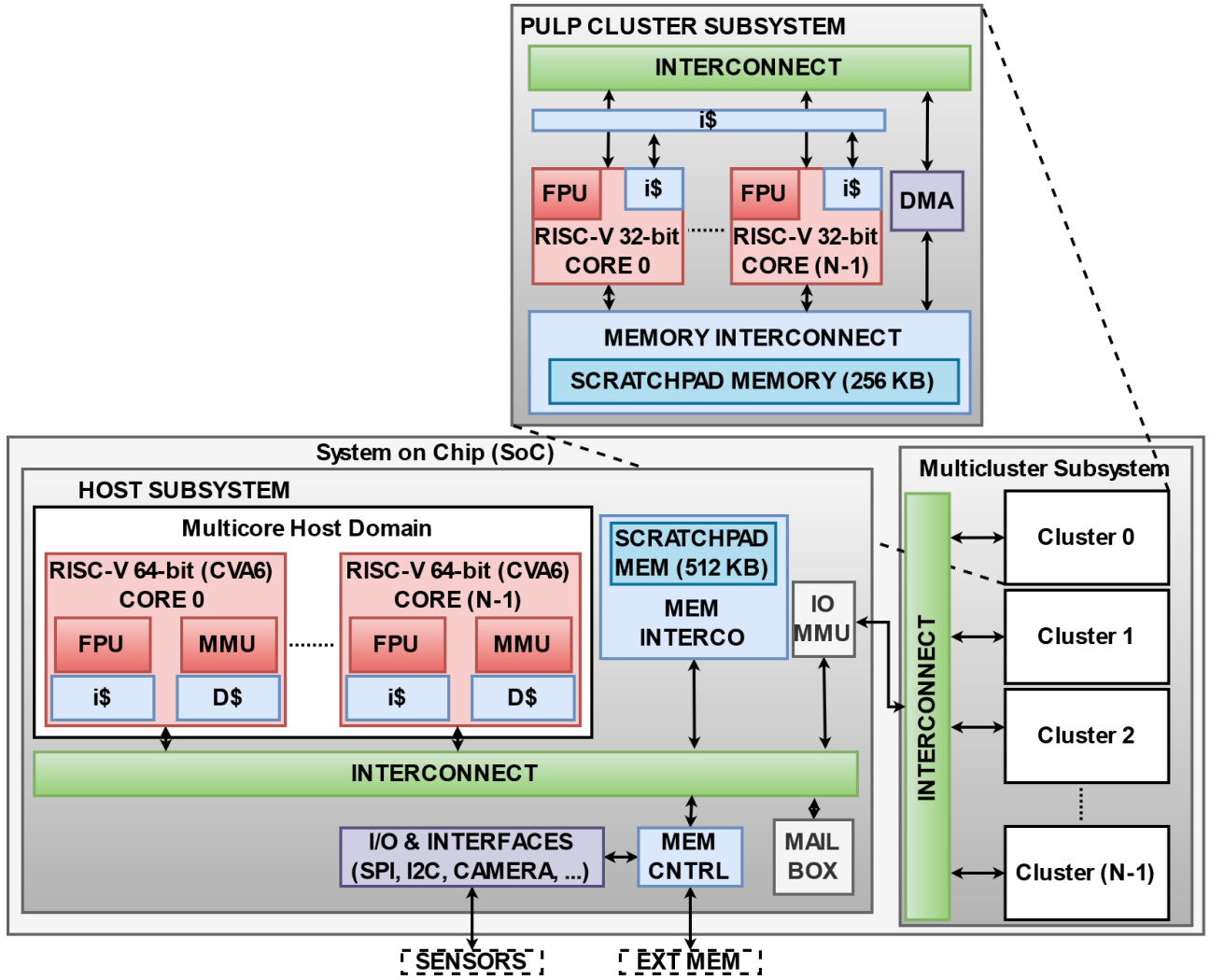




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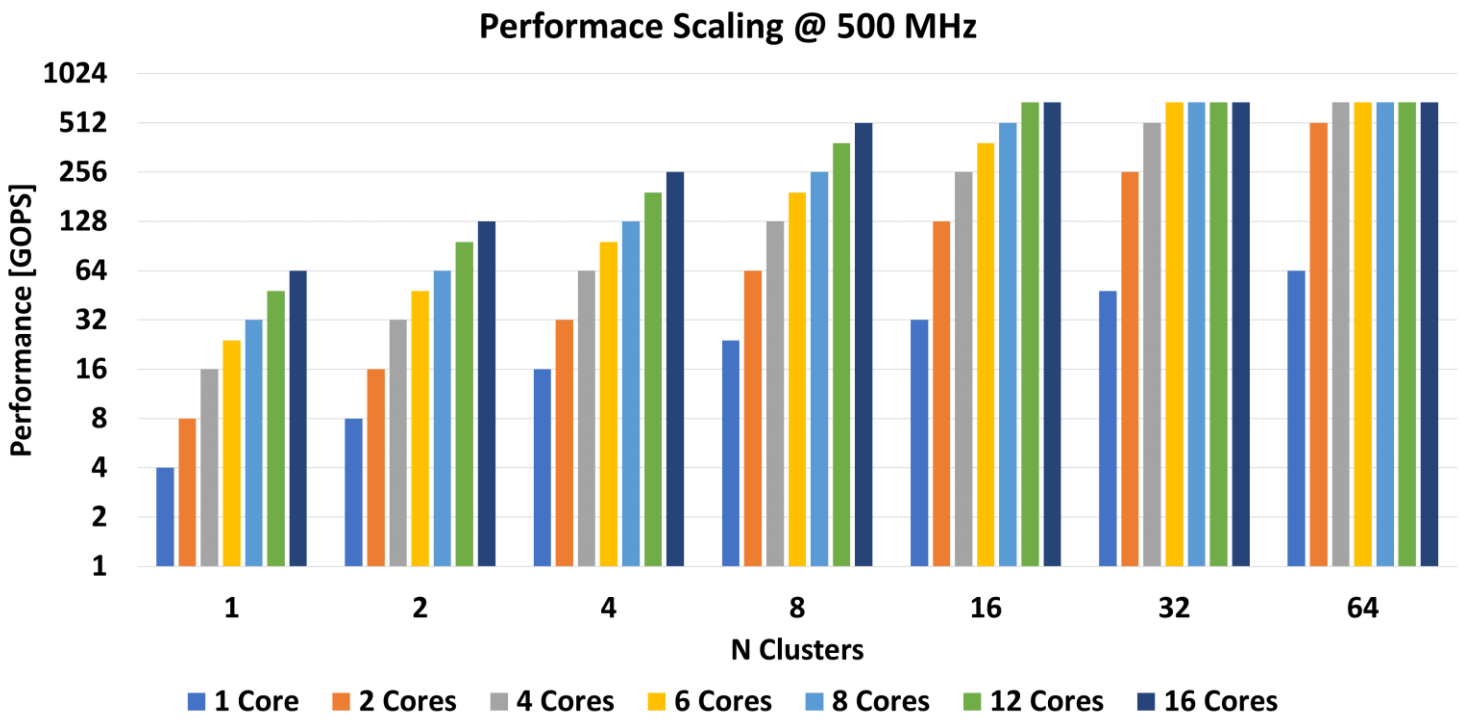
# Heterogeneous SoC for Space Applications

## Performance scales as well

- Two-axis scaling possibilities: number of clusters and number of cores per cluster
- Rooftop reached with 16 clusters, beyond the bandwith limitation blocks the performance (64 Byte/s)



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