De-RISC: the first European space-grade RISC-V platform

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THALES

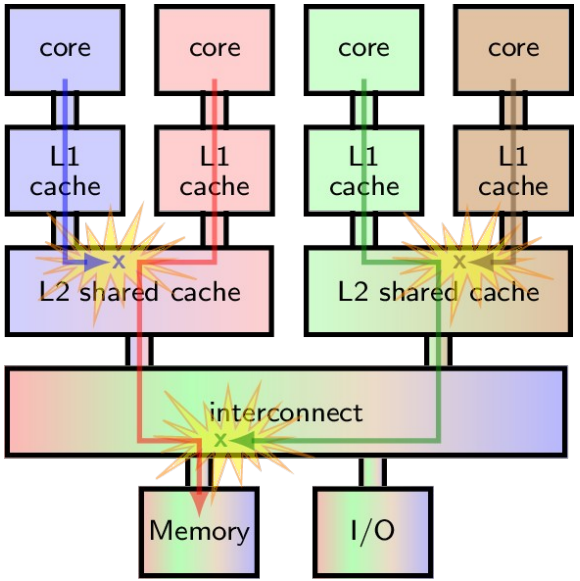

Context and Challenges

Context of safety-critical systems

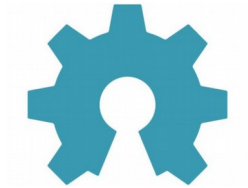
- Strict requirements for dependability
  - Robustness in harsh environments
  - Fault tolerance, fail-operational
  - Deterministic real-time behaviour
- Increasing need for performance
  - Algorithms get more complex, with larger datasets
  - Adaptive or multi-mode applications, multiple applications
  - Autonomous systems
- New requirements
  - Increased connectivity
  - Cybersecurity
  - Free from export control restrictions

Context of COTS multicore processors

- To address performance needs, increase the number of processor cores
- Other resources are not duplicated accordingly
  - Memory hierarchy, peripherals, datapaths
- Timing interference
  - Delay due to concurrent access to shared resource
  - Need for interference channels identification and mitigation
    - Required by safety standards (e.g. CAST32A)
  - Often non-documented hardware arbitration policies
- Mitigation of contentions
  - Allocate resource to a single initiator
  - Global scheduling of transactions on shared resources, not just tasks on cores



Open-source opportunities



- Safety-critical systems is a small market
  - Previously not cost-effective to design dedicated hardware
    - Except for radiation-tolerance constraints in space
    - But New Space constellations need cheaper solutions
  - It's also increasingly costly to use multicore COTS
- Open-source advantages
  - Openness: observability, ability to document, cybersecurity audit
  - Respect of standards, interoperability
  - Better test coverage by a broader userbase
- Open-source Hardware
  - LEON Sparc is a European success story in Space
  - Recent rise in popularity with RISC-V
  - Opportunity to introduce safety constraints in the community

RISC-V is a game-changer

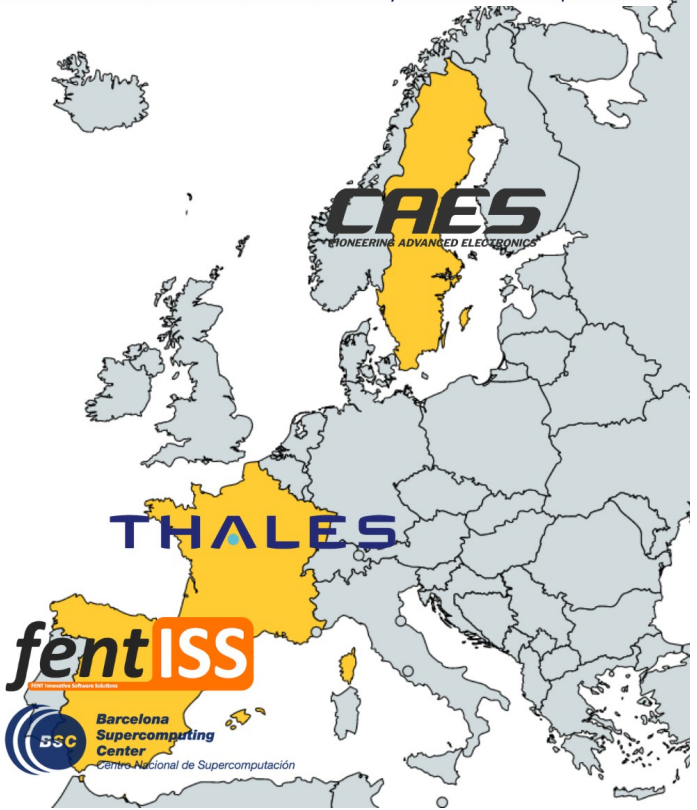
- RISC-V instruction set
  - Standard maintained by RISC-V International
  - Permissive open-source licence ensures wide adoption
  - Efficient and modular ISA, with optional extensions
  - Some peripherals : interrupt controller, MMU, etc.
- Technical Groups and Special Interest Groups
  - Security Standing Commitee
  - Cache Management Operation Task Group
  - Functional safety SIG
- Open source implementations by industrial associations
  - OpenHW Group
  - CHIPS Alliance

De-RISC approach

De-RISC project overview

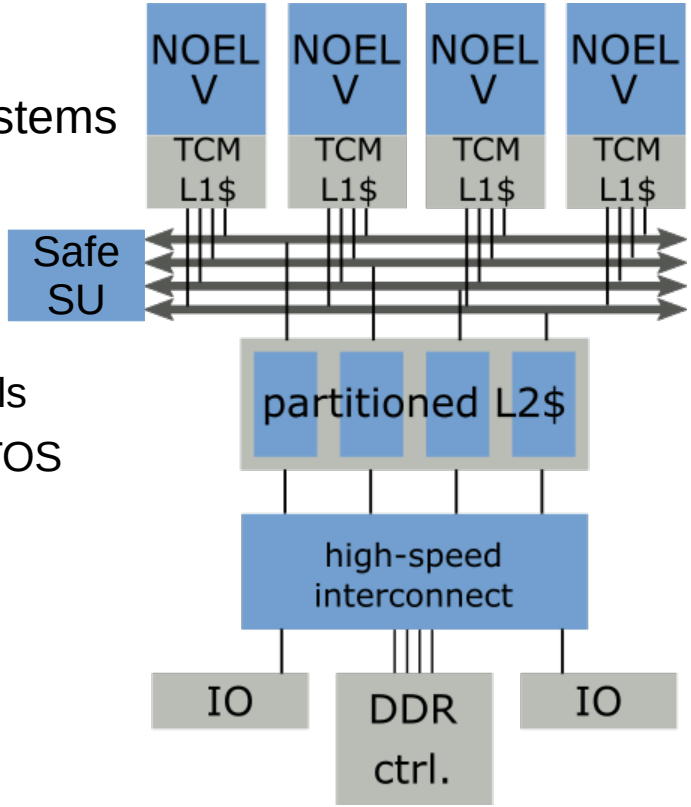
De-RISC
Dependable Real-time Infrastructure for Safety-critical Computer

- Dependable realtime infrastructure for Safety-critical Computers
  - H2020 Fast Track to Innovation project
  - 4 partners: fentISS, Barcelona Supercomputing Center, CAES Gaisler, Thales Research & Technology
  - Started in October 2019 for 36 months
- Goal: to develop a full computing platform for space
  - Fault-tolerant multicore NOEL-V architecture on FPGA
  - XtratuM NG space-qualified hypervisor
  - Advanced monitoring and interference mitigation
  - Validation with space applications
- Made in Europe



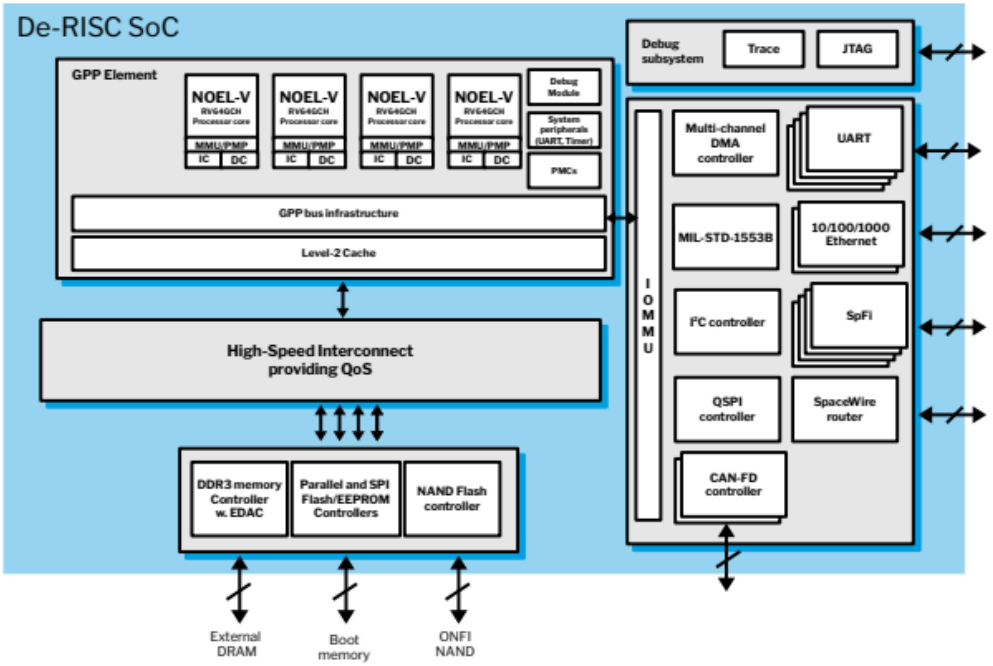
De-RISC solution

- Leveraging the RISC-V architecture for critical systems
  - High-performance NOEL-V core
  - Designed with fault-tolerance capabilities
- Building a full platform
  - A complete MPSoC with a wide selection of peripherals
  - A full software stack with certifiable hypervisor and RTOS
  - Advanced monitoring capabilities with SafeSU
- Minimized interference channels
  - Private scratchpad memories
  - Low-interference interconnect
  - Multichannel DDR controller



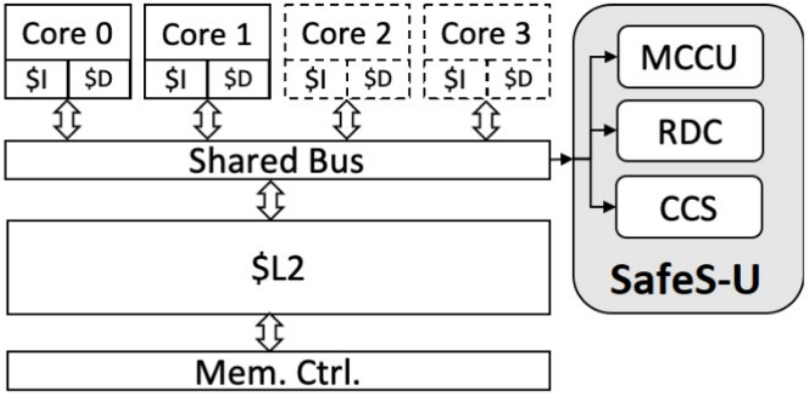
De-RISC hardware overview

- Quad-core SoC
  - Extensible to multiple clusters
  - Provision for Accelerators
- Implemented on FPGA
  - Xilinx KCU105 prototype board
  - DeRISC embedded board
  - Plans of future ASIC version
- Space-grade IO
  - SpaceWire, SpaceFibre, CANbus
  - MIL-STD-1553 provision



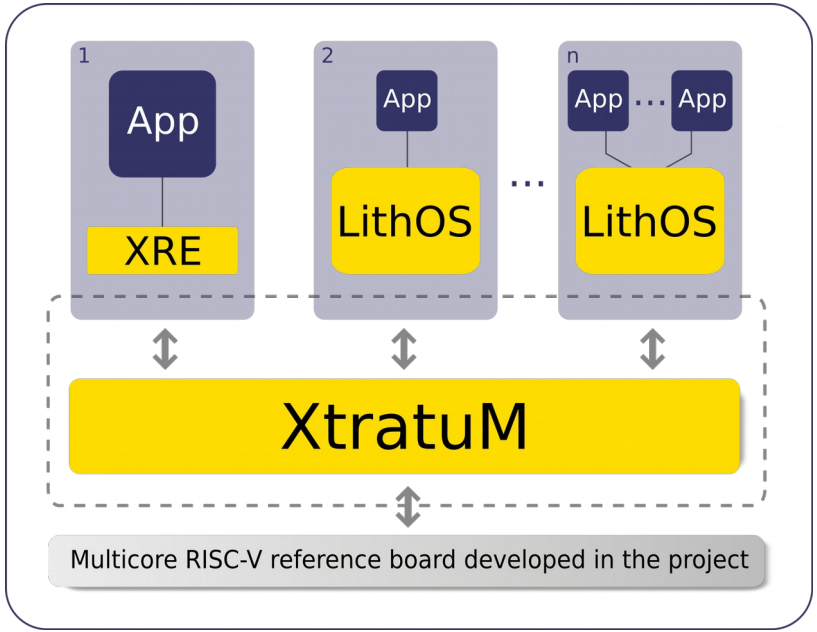
Hardware focus: SafeSU Statistics Unit

- Connected to the cluster local AMBA bus
- **Timing verification → RDC**
  - Collects maximum latency values for WCET estimation
- **Timing validation/diagnosis → CCS**
  - Statistics on how much contention (interference) each core causes on every other core
- **Implementation of safety measures related to timing → MCCU**
  - Allows setting interference quotas and raise interrupts when user-defined interference quotas are exceeded



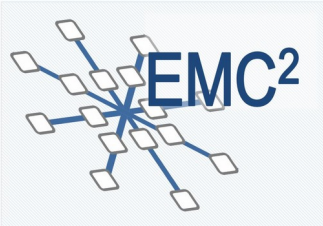
De-RISC software overview

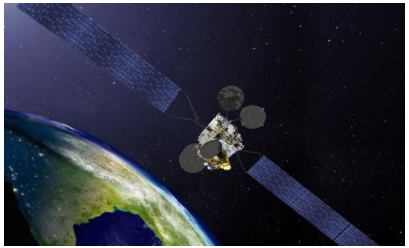
- XNG - XtratuM Next Generation
  - Lightweight hypervisor
  - Simple XRE execution environment
  - Support of LithOS and RTEMS as guest-OS, support of Linux in development
  - Used in OneWeb constellation
- LithOS
  - ARINC-653 RTOS running in a XNG partition
  - Planned qualification ECSS level B (expected after end of project)



De-RISC validation use cases

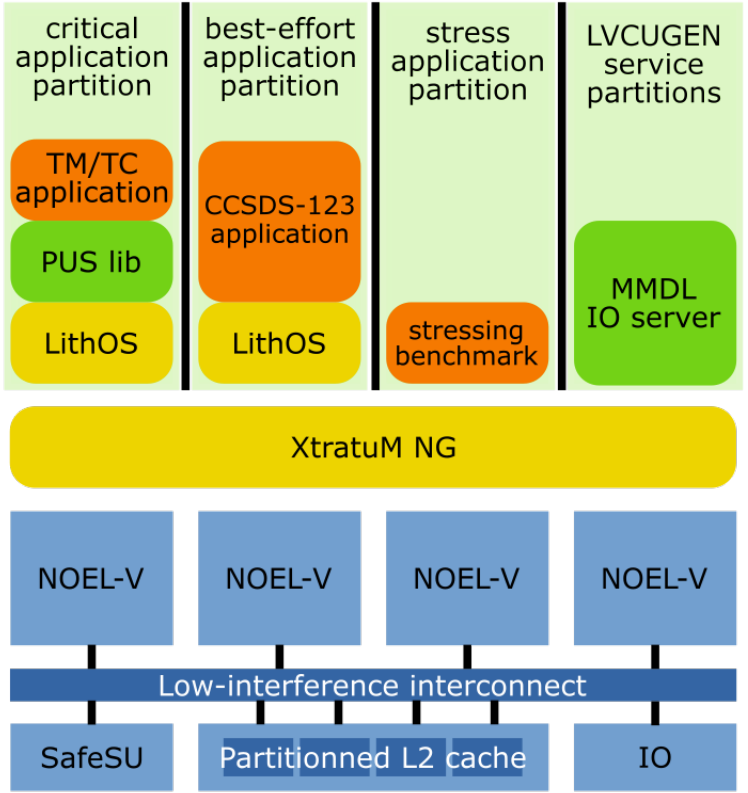
- Basic benchmarks
  - Standards for performance estimation such as Dhrystone, Coremark
  - Usual compute kernels with larger datasets
  - Stressing benchmarks to characterize interference channels
- Space use case for comparison with previous platforms
  - Control & Data Handling application from Thales Alenia Space Italy
  - Previously used in EMC² project on LEON-4 platform
- Representative space payload software
  - Based on LVCUGEN from CNES
  - Hyperspectral image compression as data-intensive application
  - Realtime services as critical application





Flight software use-case

- Critical partition based on LVCUGEN services
  - TM/TC messaging
  - IO server
- Memory-intensive partition
  - CCSDS-123 lossless image compression
    - Hyperspectral data cube
    - Predictor and propagation
- Validation of time and space isolation
  - Using hardware counters to monitor timing interference



Results

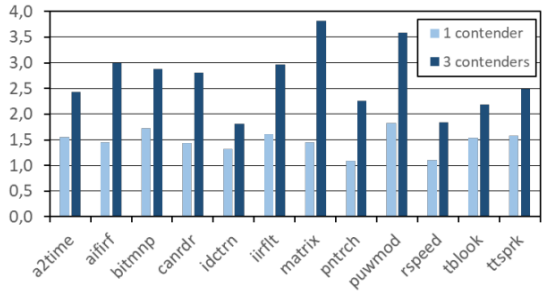
Results

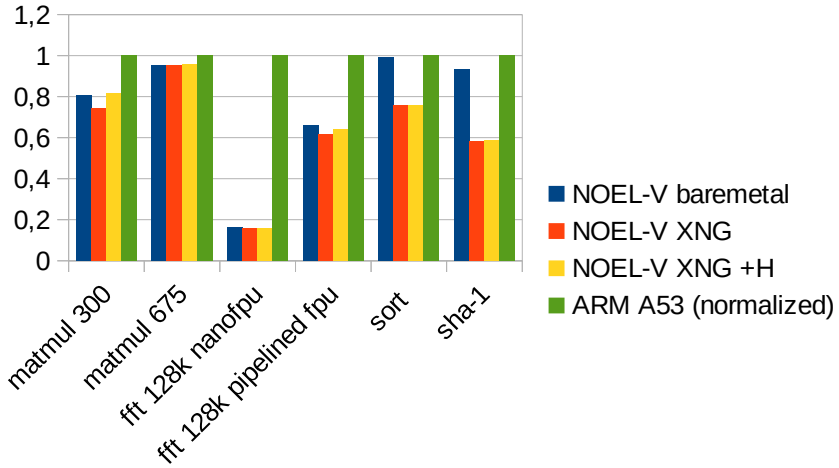
- De-RISC SoC is functional on FPGA
  - Integration of new features (incl. H extension, new FPU)
  - Integration of SafeSU monitoring unit
  - Development of GR-CPCIS-XCKU 6U cPCI Space Serial board
  - Radiation tests – published in RADECS 2022
- Successful porting and integration of hypervisor and RTOS
  - XtratuM Next Generation with SMP support, LithOS guest OS
  - RTEMS ported as guest OS
  - Development tools incl. Xoncrete schedulabilty analyser
- Validation phase
  - Performance and stressing benchmarks ported
  - LVCUGEN ported to RISC-V and 64-bits
  - Integration of space use-cases

Results

- Benchmarks

(higher is better)	NOEL-V	ARM A53
DMIPS/MHz	2.82	2.31
Coremark/MHz	4.41	3.27





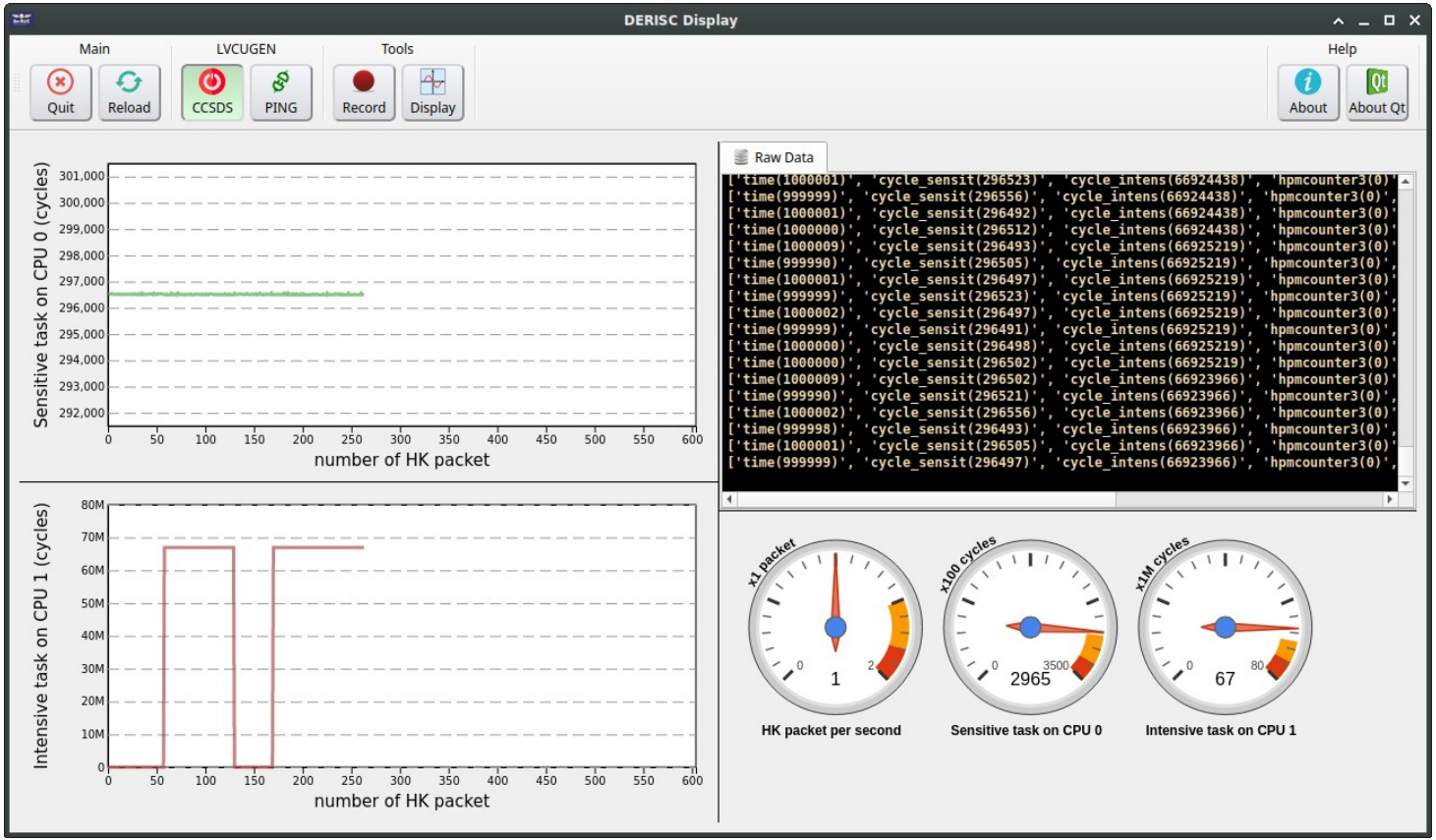
- Command & Data Handling platform
  - Inter-partition communications
  - Floating-point quaternion computation

Time in µs (lower is better)	NOEL-V XNG	LEON-4 XtratuM
Enqueue TC	55	95
Dequeue TC	56	57
Dequeue TM	29	36
Work (float)	60	316

Flight software use-case

- Based on LVCUGEN
  - Data-intensive application on one core : CCSDS123 hyperspectral image compression
  - Time-sensitive application + LVCUGEN service partitions on another core : TM/TC process, reporting execution time and activating the data-intensive app
- Simple ground station simulator
  - Visualisation interface, showing execution time variation
  - Activation of data-intensive app has very little effect on critical task
- Live demo shown at DeRISC workwhop, HiPEAC 2022, Budapest

Result : Flight software use-case



Conclusion

- De-RISC solution
  - Open-source, safety- and determinism-oriented multicore SoC
  - Complete and certifiable software stack
  - Advanced interference measurement and mitigation techniques
  - Validation with representative use-cases
- The De-RISC platform is available now
  - NOEL-V open-source design and evaluation bitstreams
  - XNG, LithOS and their toolchain
  - SafeSU under permissive open-source licence
- Follow-up projects
  - ESA ITT Fifth-gen Space Multicore Processor Prototype
    - ASIC implementation
  - KDT Isolde
    - RISC-V Multicore for safety and security, all De-RISC partners involved

De-RISC

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