Introduction to Microchip's RISC-V ecosystem

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

Luca Cattaneo
EMEA Aerospace & Defense Segment Technical Manager

December 14, 2022

Pioneering the RISC-V FPGA Revolution

Join RISC-V Foundation Launch Fund

Attend our first RISC-V Workshop

Microchip meets with UC Berkeley

Microchip is RISC-V Aware

2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023

RISC-V revolution benefits

- **Free and open ISA**
  - Clean Slate Design
  - Simple, Stable
  - Modular, Extendable
- **RISC-V owned by everyone**
- **RISC-V extends Moore's Law**
  - Provides a free “architectural” license enabling innovation
  - Customers can, now, influence the micro-architectural design
  - Provides lower power & higher performances
- **Chairing Marketing, Debugging, Encryption ISE**

Microchip RISC-V Solutions: Address Challenges at the Edge

4 Big Challenges For Edge Compute

- Thermal Constraints
- Minimal Power Budgets
- Safety and Security
- Flexible Compute Requirements

Clear Leadership with PolarFire® Platform

MICROCHIP PolarFire® FPGA

MICROCHIP PolarFire® SoC SoC FPGA

- Low Power
- Security
- Reliability

Freedom to Innovate With RISC-V in Embedded Systems

- Linux
- Bare Metal
- Linux + Bare Metal

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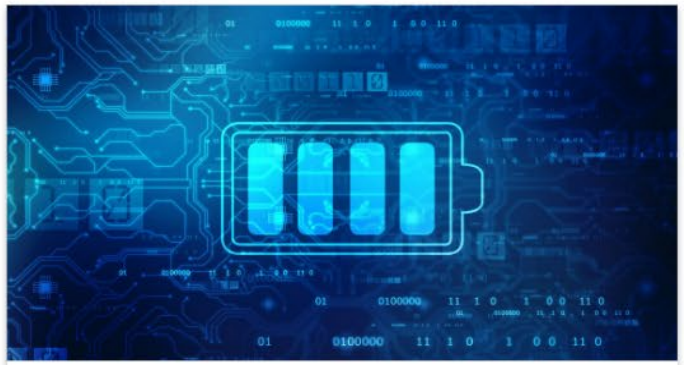
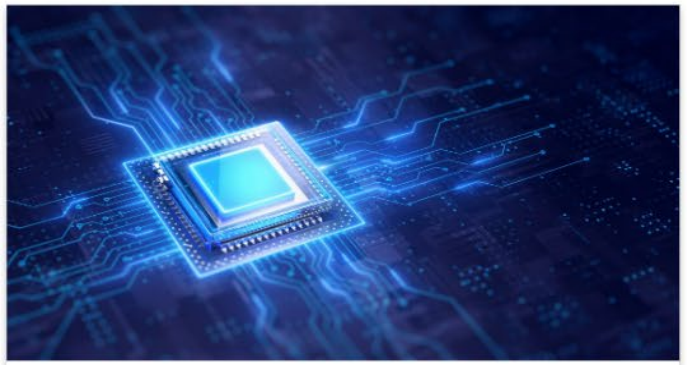
The PolarFire® and RISC-V Revolution: Solving Problems No One Else Can

Enable Innovation by Offering the Most Power-efficient Programmable Solutions



Most Power-Efficient FPGAs

Two Times More Performance Per Watt



Exceptional Reliability

Zero Configuration Upsets

Military-Grade Security

Best Cyber and Anti-Tamper Security

MICROCHIP PolarFire® FPGA — Soft RISC-V®

MICROCHIP PolarFire® SoC SoC FPGA — RISC-V®

MICROCHIP RT PolarFire® FPGA — Soft RISC-V®

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What is Mi-V?

“Mi-V” (pronounced My-Five) = Microchip’s RISC-V Ecosystem

- A continually expanding, comprehensive RISC-V Ecosystem
- Supporting client application development using Microchip’s soft-CPUs and RISC-V SoC FPGAs

Flash Technology Based SoC & FPGA Offering

Hard Processor Subsystems, Soft RISC-V CPU's

Features / RT-FPGA SoC FPGA Technology	RT-ProASIC3® SmartFusion ProASIC3®, IGLOO Flash 130nm	RTG4™ Smartfusion2® Igloo2® Flash 65nm	RT-PolarFire® PolarFire® SONOS 28nm	PolarFire® SoC SONOS 28nm
Logic Elements	100 - 30K	5K - 150K	100K - 480K	25K - 450K
Transceiver Rate	--	1-5 Gbps	250 Mbps-12.7 Gbps	250 Mbps-12.7 Gbps
I/O Speeds	400 Mbps LVDS	667 Mbps DDR3 750 Mbps LVDS	1600 Mbps DDR4 1.6 Gbps LVDS	1600 Mbps DDR4 1.6 Gbps LVDS
DSP (18x18Mult) w/o w/ pre-adder	--	240	1480	1420
Max RAM	144 Kb	5 Mb	33 Mb	32 Mb
Processor Option Soft Crypto Hard	100 MHz **ARM Cortex-M3**	**Soft RISC-V** **Secure Micro** 166 MHz **ARM Cortex-M3**	**Soft RISC-V** **SecMcu+Crypto Co-Processor**	**Soft RISC-V** **Secure Micro + Crypto Co-Processor** **5 RISC-V (1xS51 + 4xU54) Multicore System**
On-board Flash	Up to 512 KB code store	Up To 512 KB code store	56 KB secure NVM	56 KB secure NVM 128KB BootFlash
Family Type	CPLD Replacements Smallest Packages	Low Density FPGAs with more resources & Lowest Power	Mid-Range Density FPGAs Lowest Power, Cost Optimized	Open, Lowest Power, Cost Optimized, Programmable SoC

CPUs: Mi-V Soft CPUs Detailed Offering

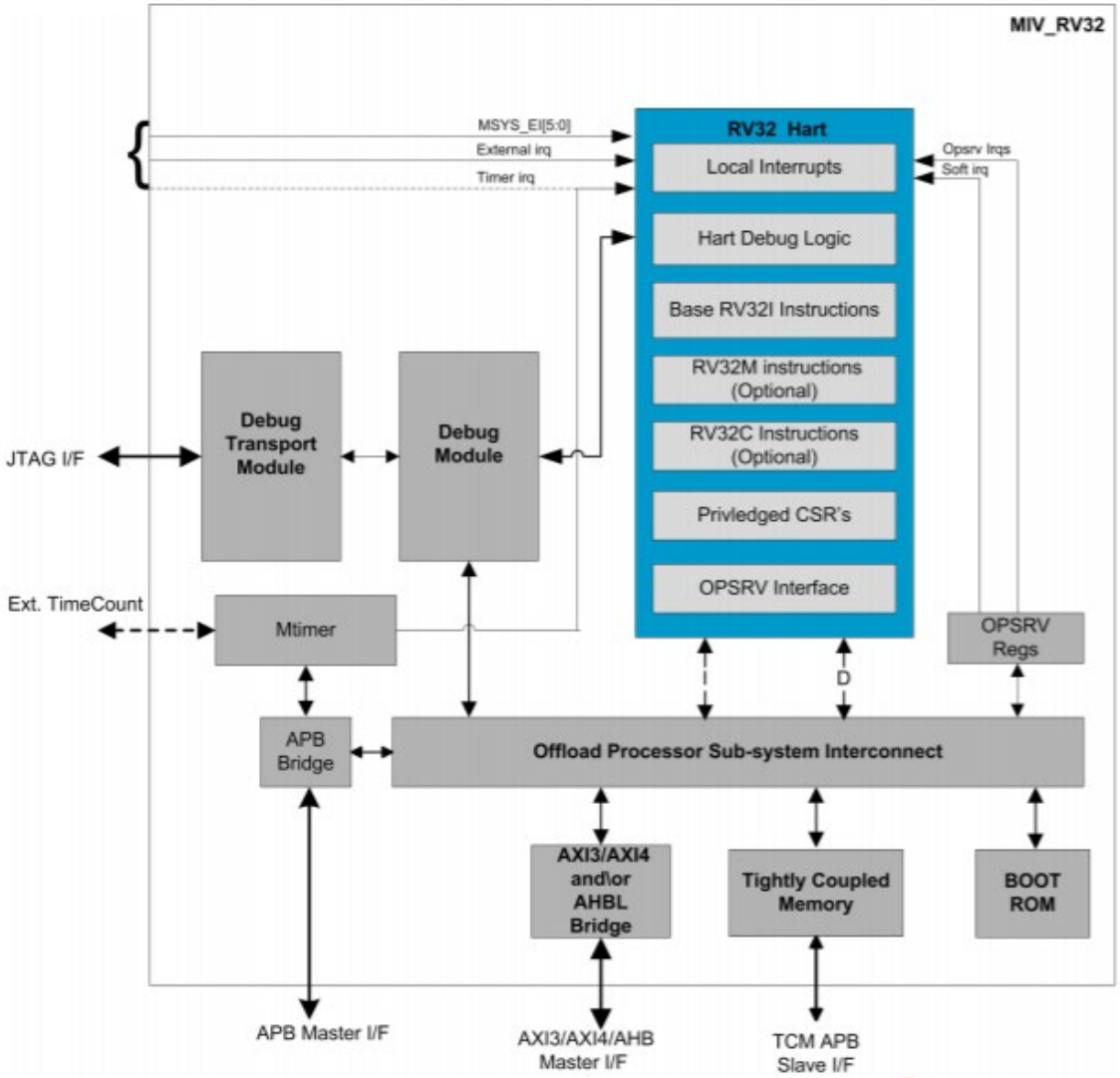
RISC-V Soft CPU	MiV_RV32	Mi-V_RV32IMAF_L1_AHB	Mi-V_RV32IMA_L1_AHB	Mi-V_RV32IMA_L1_AXI
LEs	4k-10k	26k	10k	10k
Coremark Score	0.177-2.77	2.01	2.01	2.01
Cache Size	N/A (Coming soon)	8KB I/D	8KB I/D	8KB I/D
Tightly Coupled Memory (TCM)	configurable depth upto 256Kb	N/A	N/A	N/A
Compressed	optional	N/A	N/A	N/A
Mul/Div	Optional: MACC, Pipelined-MACC, or 32 cycle fabric	Yes	Yes	Yes
Atomics	N/A	Yes	Yes	Yes
Floating Point	N/A (Coming soon)	Single Precision	N/A	N/A
Interface(s)	APB3/AHB/AXI	AHB	AHB	AXI
Debug	Optional	Yes	Yes	Yes
SECDEC	Optional	Optional	Optional	N/A
Availability	2019	2017	2017	2016

Mi-V_RV32 Configurable Soft CPU

RT-PolarFire® / RTG4™ / PolarFire® / IGLOO2®

Features

- 2.77 Coremarks / MHz
- HW breakpoint - 1
- Interrupts - 13
- Timer / Counter - 1
- 50 MHz–150 MHz (Product dependent)
- Optional / Configurable Features
  - AHB/AXI3/AXI4/APB Bus Interfaces
  - Integer mul/div
  - Tightly coupled memory
  - Debug
  - Error Correction



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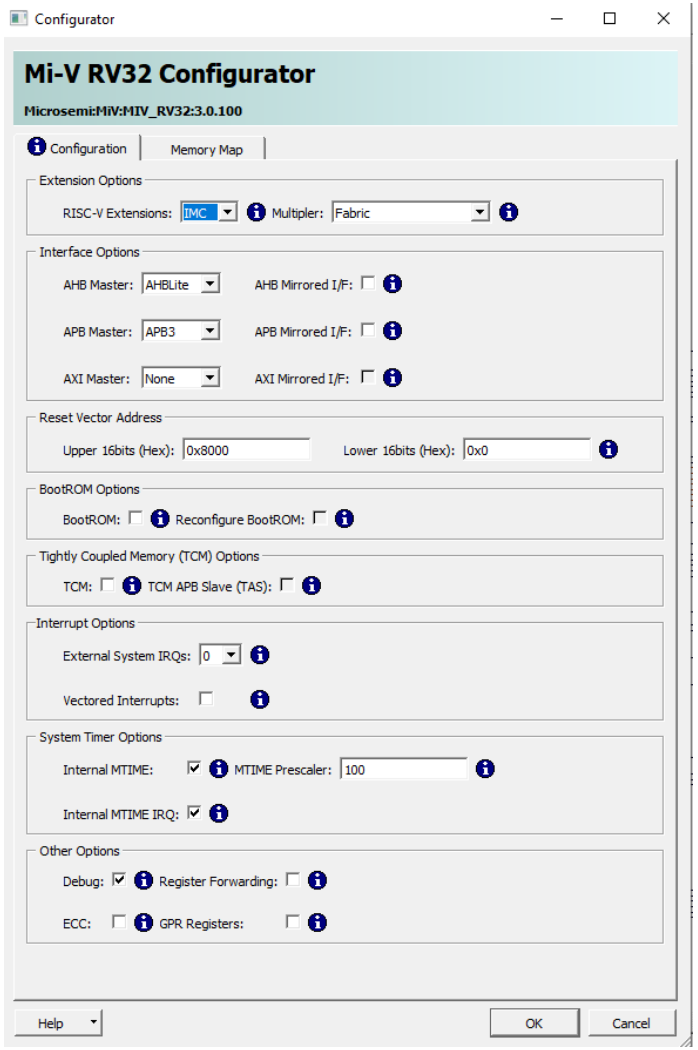
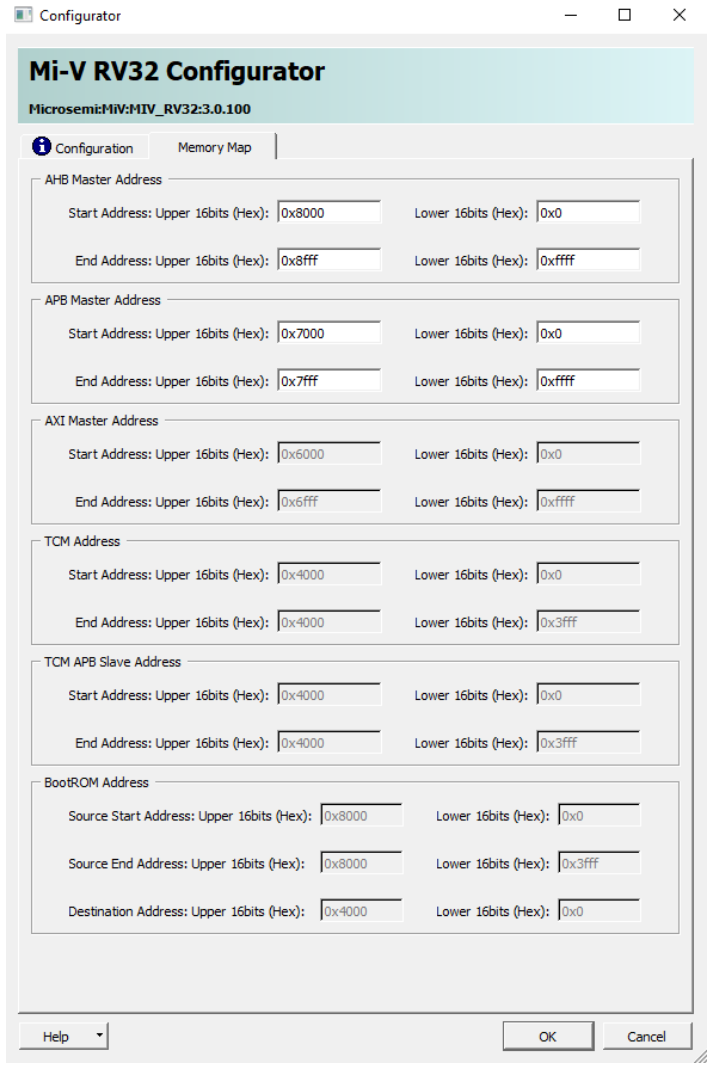
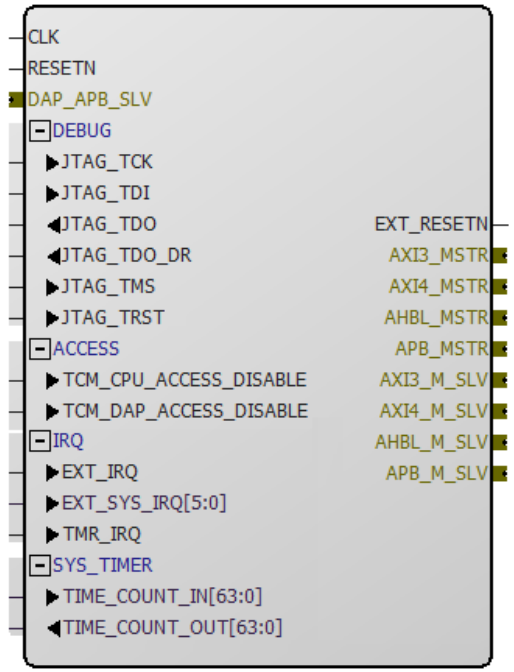
MiV_RV32 Configurator

GUI Configuration & Memory Map





MIV_RV32 Full I/O View



MIV-ESS Extended SubSystem Solution

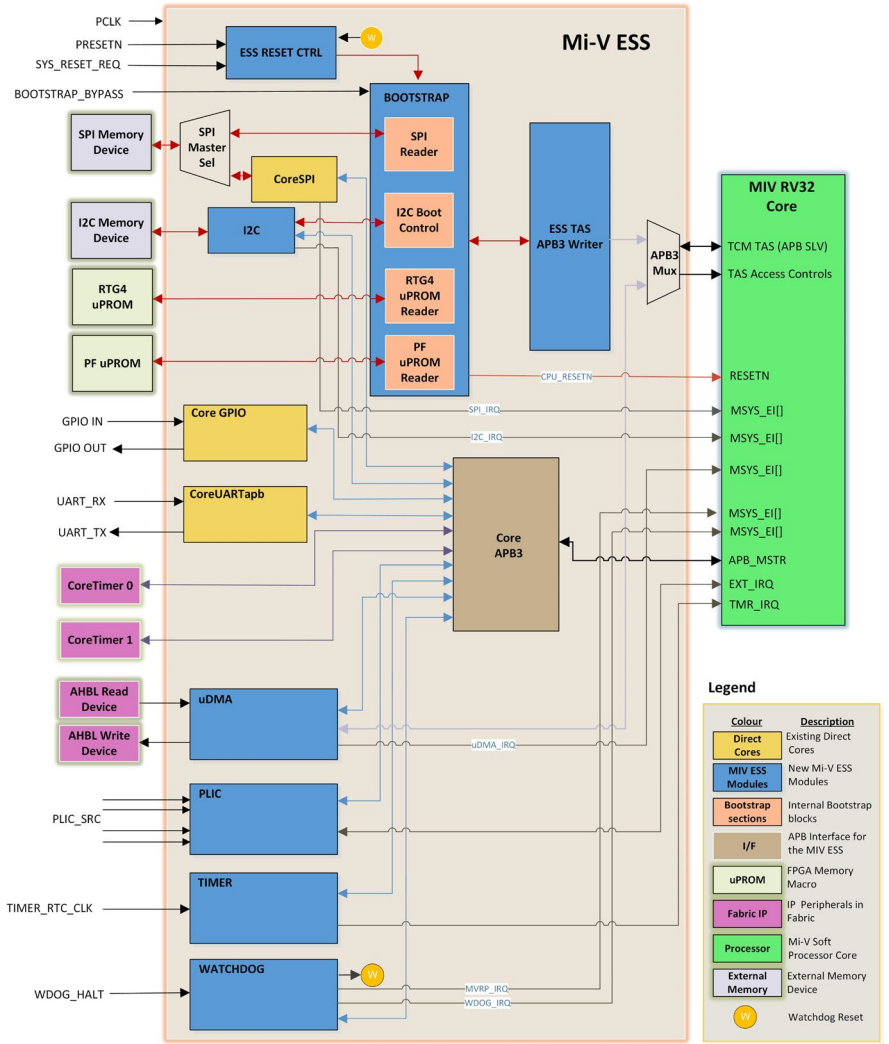
The MIV_ESS is a highly configurable, compact, extended subsystem solution

Optional bootstrap to MIV_RV32 TCM from the following non-volatile memory sources.

- – Serial peripheral interface (SPI) Flash
- – I2C EEPROM
- – On-chip µPROM (PolarFire® and RTG4™ devices)

Optional memory-mapped **peripheral** modules.

- – Timer (64-bit with pre-scaler)
- – Watchdog
- – SPI
- – I2C
- – µDMA with AHB-Lite read port and either AHB-Lite or TAS (APE
- – Platform-Level Interrupt Controller (PLIC) with up to 31 interrup
- – GPIO
- – UART
- Seven **optional** external APB interfaces to connect additional per



RISC-V Multicore on RT FPGAs

- **RISC-V Multi-Processors Subsystem**
  - Extensive list AMBA Based IP cores available

    AMBA Buses, LSRAM, UART, GPIO, SPI, I2C, Timer, WDOG, 1553B, Ethernet MAC 10/100/1000
- **RT PolarFire®, RTG4™ FPGA**
  - RISC-V Lockstep System AN4228
  - Single RISC-V System TU0775, AC490

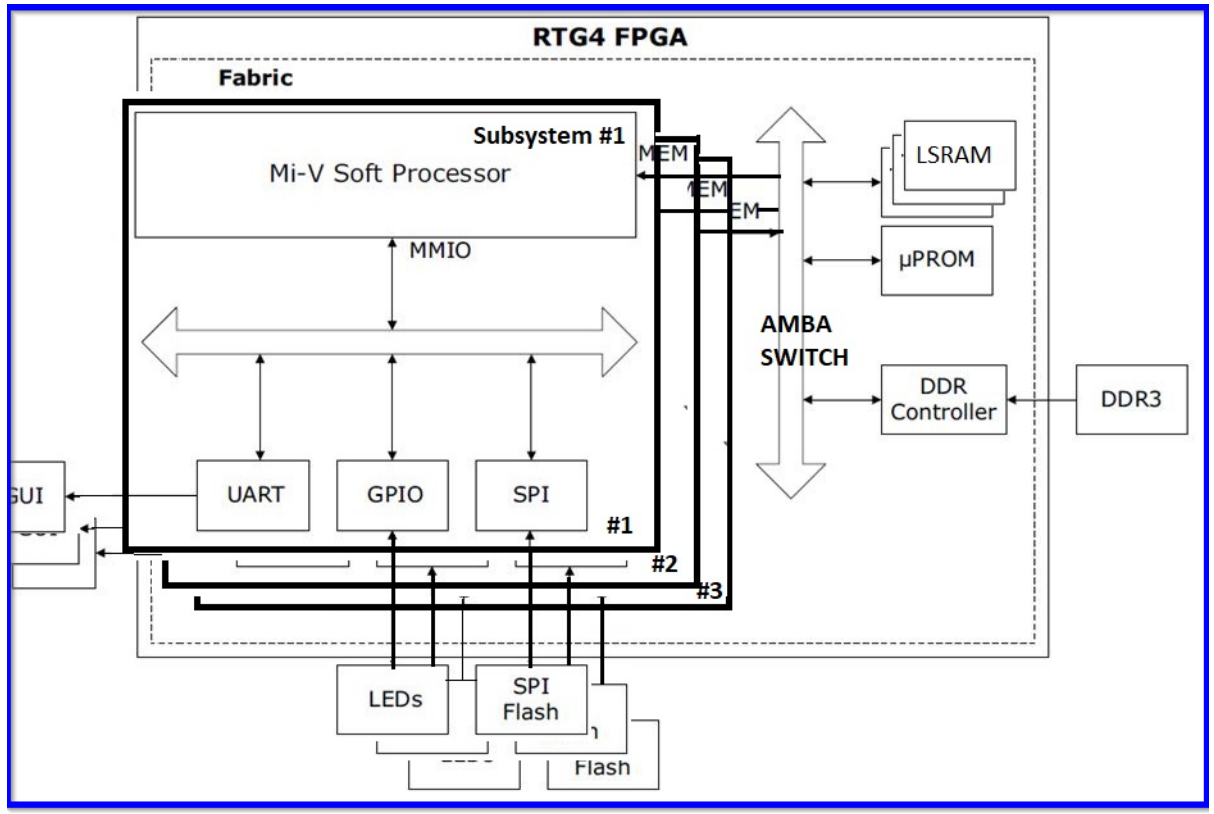
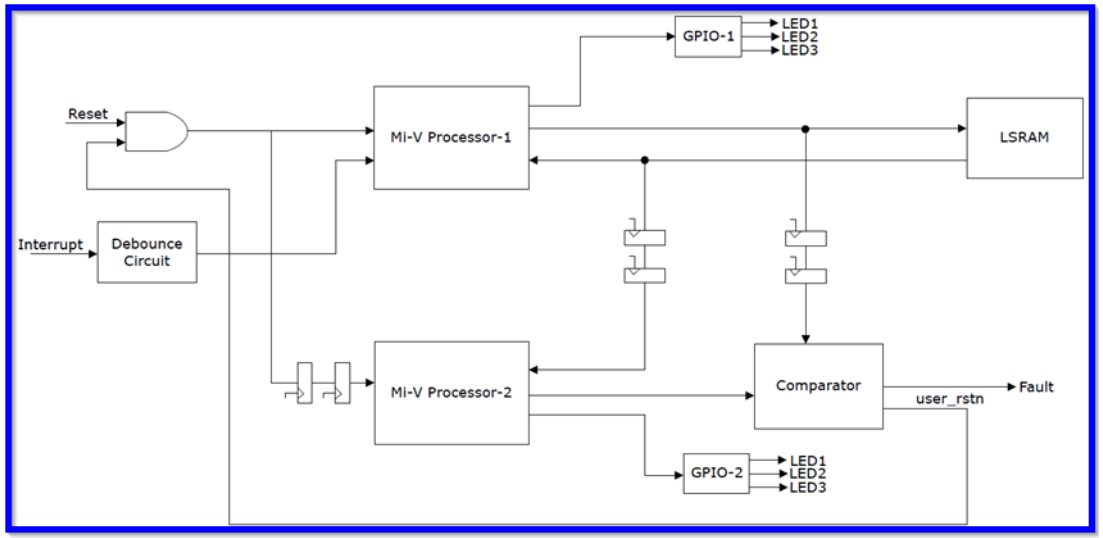


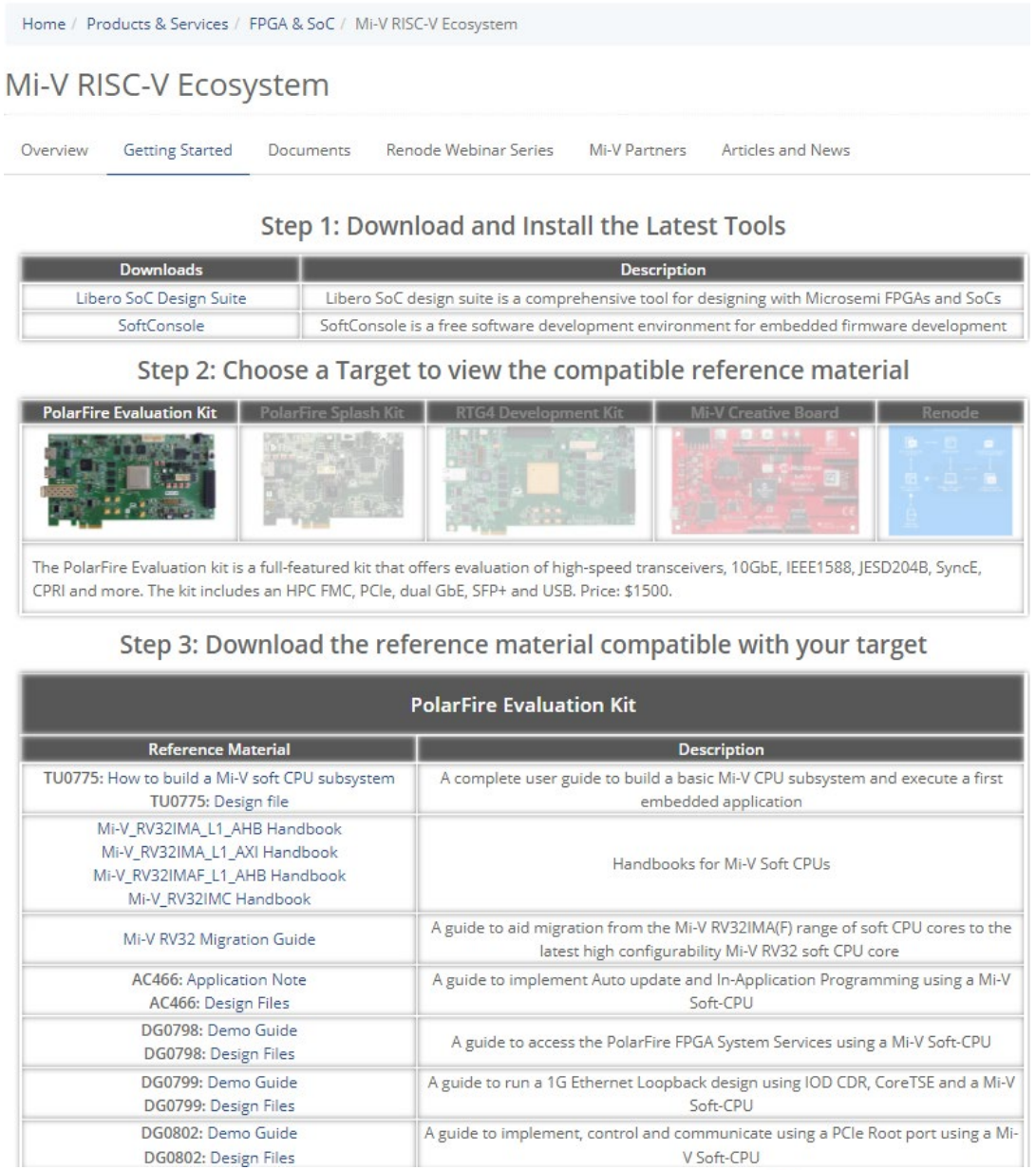
Figure 1-1. Lockstep Design High-level Block Diagram



Getting Started

- www.mi-v.org
  - Design Tools
  - Supported hardware
  - Documentation:
    - Tutorials
    - Application notes & User guides

- **GitHub page:**
  - https://github.com/RISCV-on-Microsemi-FPGA
  - Reference designs
    - Libero Projects
    - SoftConsole projects
  - RTOS Ports
  - Documentation and Sample Designs



Home / Products & Services / FPGA & SoC / Mi-V RISC-V Ecosystem

Mi-V RISC-V Ecosystem

Overview | Getting Started | Documents | Renode Webinar Series | Mi-V Partners | Articles and News

Step 1: Download and Install the Latest Tools

Downloads	Description
Libero SoC Design Suite	Libero SoC design suite is a comprehensive tool for designing with Microsemi FPGAs and SoCs
SoftConsole	SoftConsole is a free software development environment for embedded firmware development

Step 2: Choose a Target to view the compatible reference material

PolarFire Evaluation Kit | PolarFire Splash Kit | RTG4 Development Kit | Mi-V Creative Board | Renode

The PolarFire Evaluation kit is a full-featured kit that offers evaluation of high-speed transceivers, 10GbE, IEEE1588, JESD204B, SyncE, CPRI and more. The kit includes an HPC FMC, PCIe, dual GbE, SFP+ and USB. Price: $1500.

Step 3: Download the reference material compatible with your target

PolarFire Evaluation Kit	
Reference Material	**Description**
TU0775: How to build a Mi-V soft CPU subsystem TU0775: Design file	A complete user guide to build a basic Mi-V CPU subsystem and execute a first embedded application
Mi-V_RV32IMA_L1_AHB Handbook Mi-V_RV32IMA_L1_AXI Handbook Mi-V_RV32IMAF_L1_AHB Handbook Mi-V_RV32IMC Handbook	Handbooks for Mi-V Soft CPUs
Mi-V RV32 Migration Guide	A guide to aid migration from the Mi-V RV32IMA(F) range of soft CPU cores to the latest high configurability Mi-V RV32 soft CPU core
AC466: Application Note AC466: Design Files	A guide to implement Auto update and In-Application Programming using a Mi-V Soft-CPU
DG0798: Demo Guide DG0798: Design Files	A guide to access the PolarFire FPGA System Services using a Mi-V Soft-CPU
DG0799: Demo Guide DG0799: Design Files	A guide to run a 1G Ethernet Loopback design using IOD CDR, CoreTSE and a Mi-V Soft-CPU
DG0802: Demo Guide DG0802: Design Files	A guide to implement, control and communicate using a PCIe Root port using a Mi-V Soft-CPU

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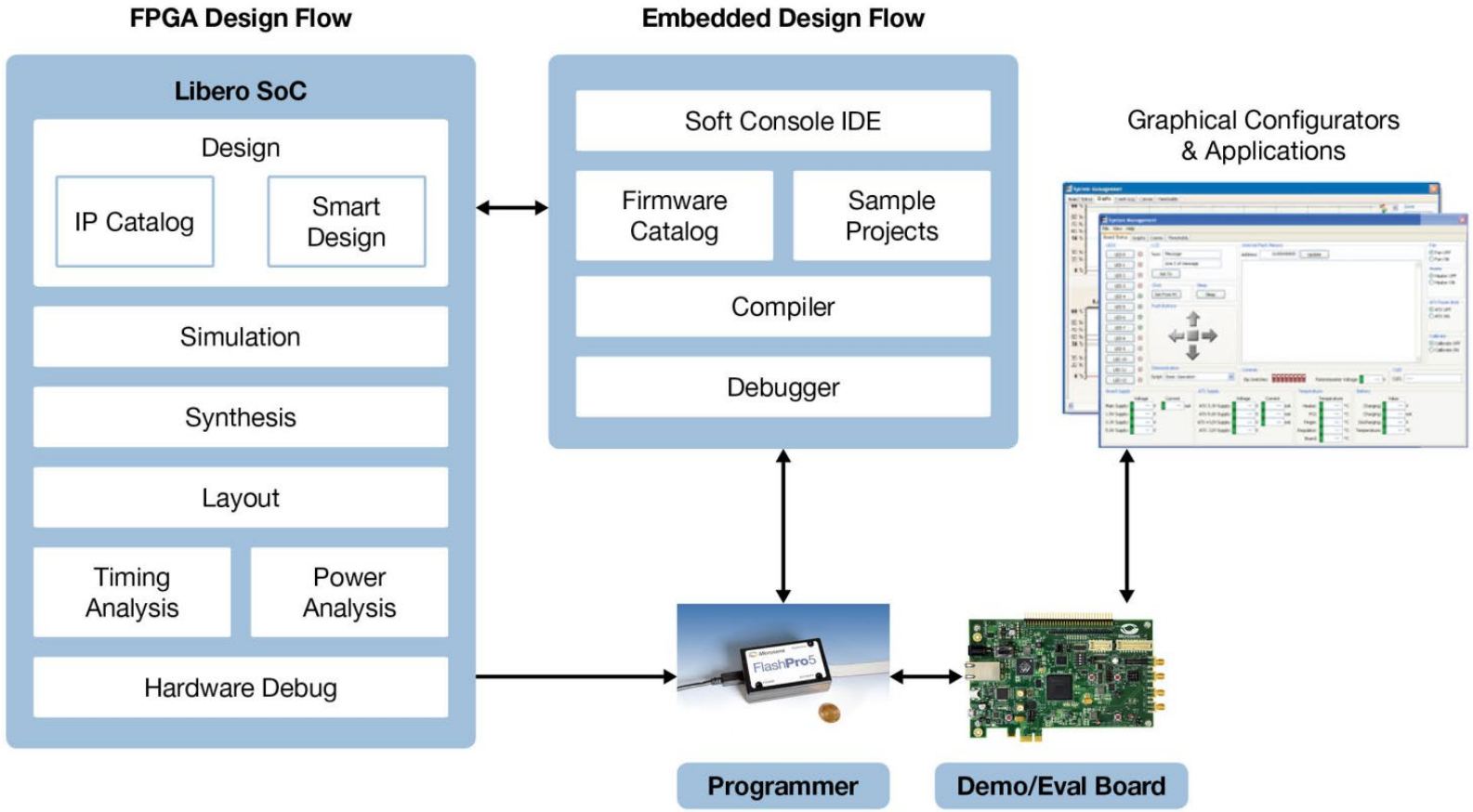
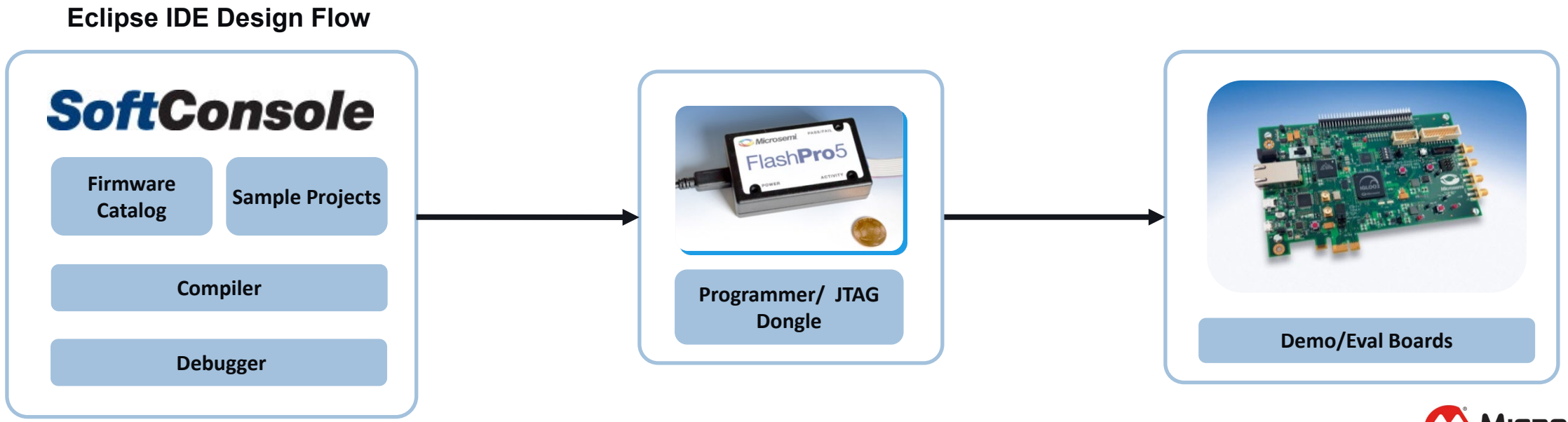
Libero® SoC Design Suite

- **Comprehensive FPGA Design Suite**
- **Easy to Learn**
  - Intuitive design flow
  - GUI wizards guiding the design process
- **Easy to Adopt**
  - Rich IP library of Microsemi and Partner Cores
  - Availability of complete reference designs and kits



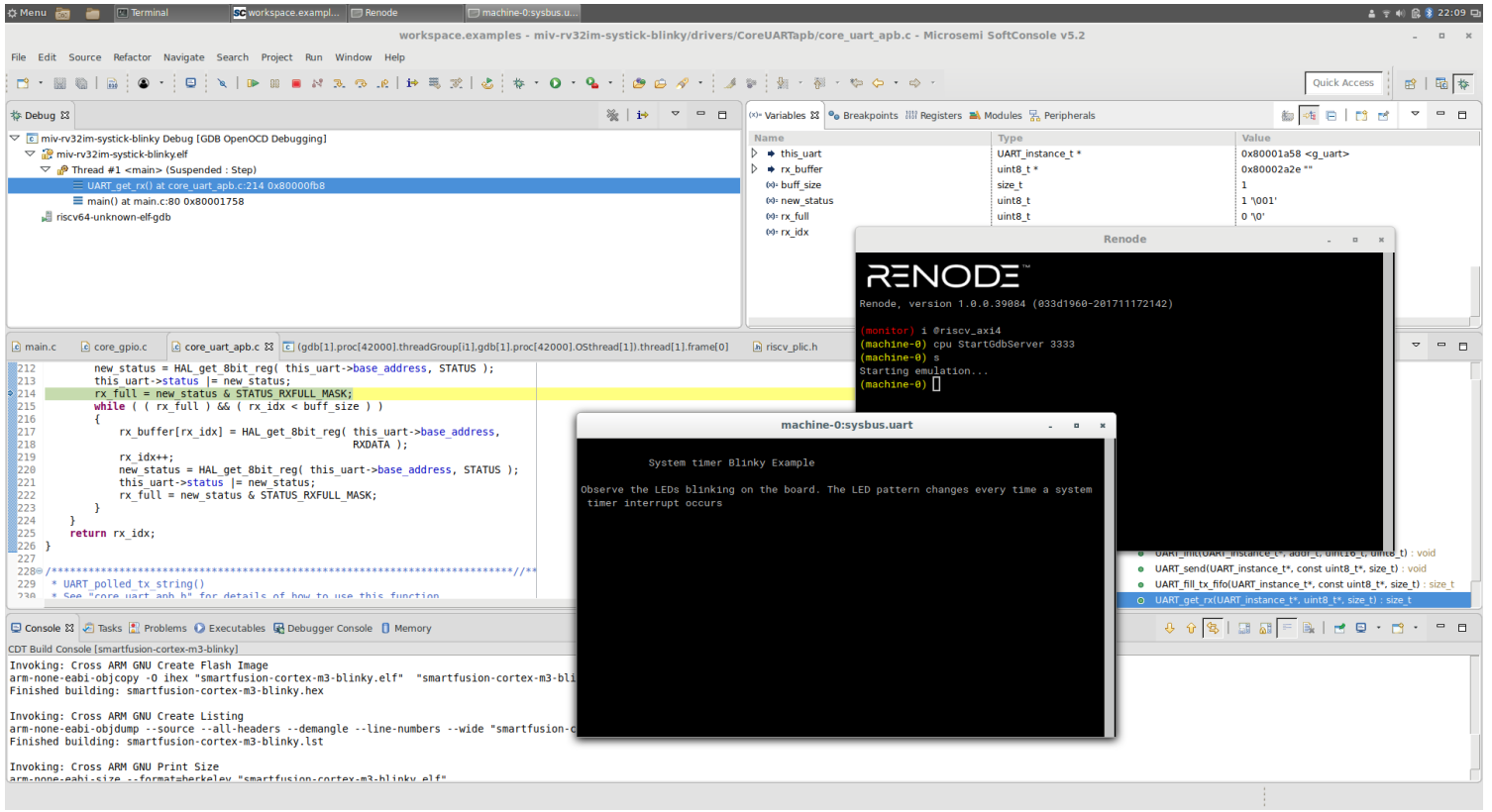
SoftConsole Eclipse IDE

- **A single tool chain supporting RISC-V MCU's**
  - Easy migration from ARM to RISC-V
- **Running on Linux or Windows Hosts**
- **Supported by a Tier 1 Supplier**
- **Bundled with example projects and RTOSs**



Instruction Set Simulator

- **Fully integrated within SoftConsole**



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Demo PolarFire® FPGA+ SiFive RISC-V ASIC

PolarFire® SoC announced: World's first FPGA with hardened multi-core MSS

PolarFire® SoC samples shipped

PolarFire® SoC Production qualified

1st MiV Summit

MiV Ecosystem @62 partners

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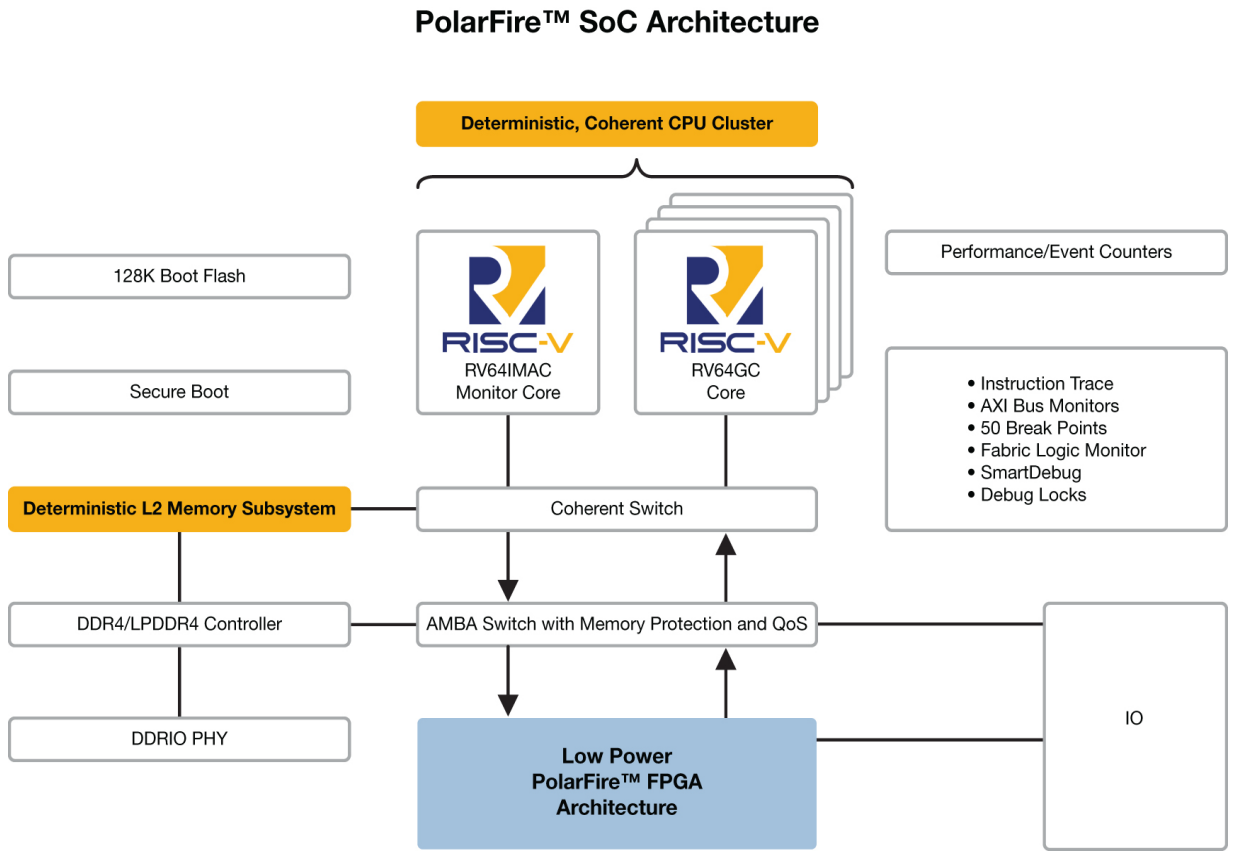
PolarFire® SoC and RISC-V: Freedom to Innovate

Freedom to Innovate in:

- ✓ Asymmetric Processing: Linux and Real-Time
- ✓ Thermal and Power Constrained Systems
- ✓ Securely Connected IoT systems
- ✓ High-Rel Safety Critical Systems

Industry's only Hardened RISC-V Processor Subsystem
Enabling SWaP-C advantages



SiFive

Mi-V ECOSYSTEM UNLEASHED

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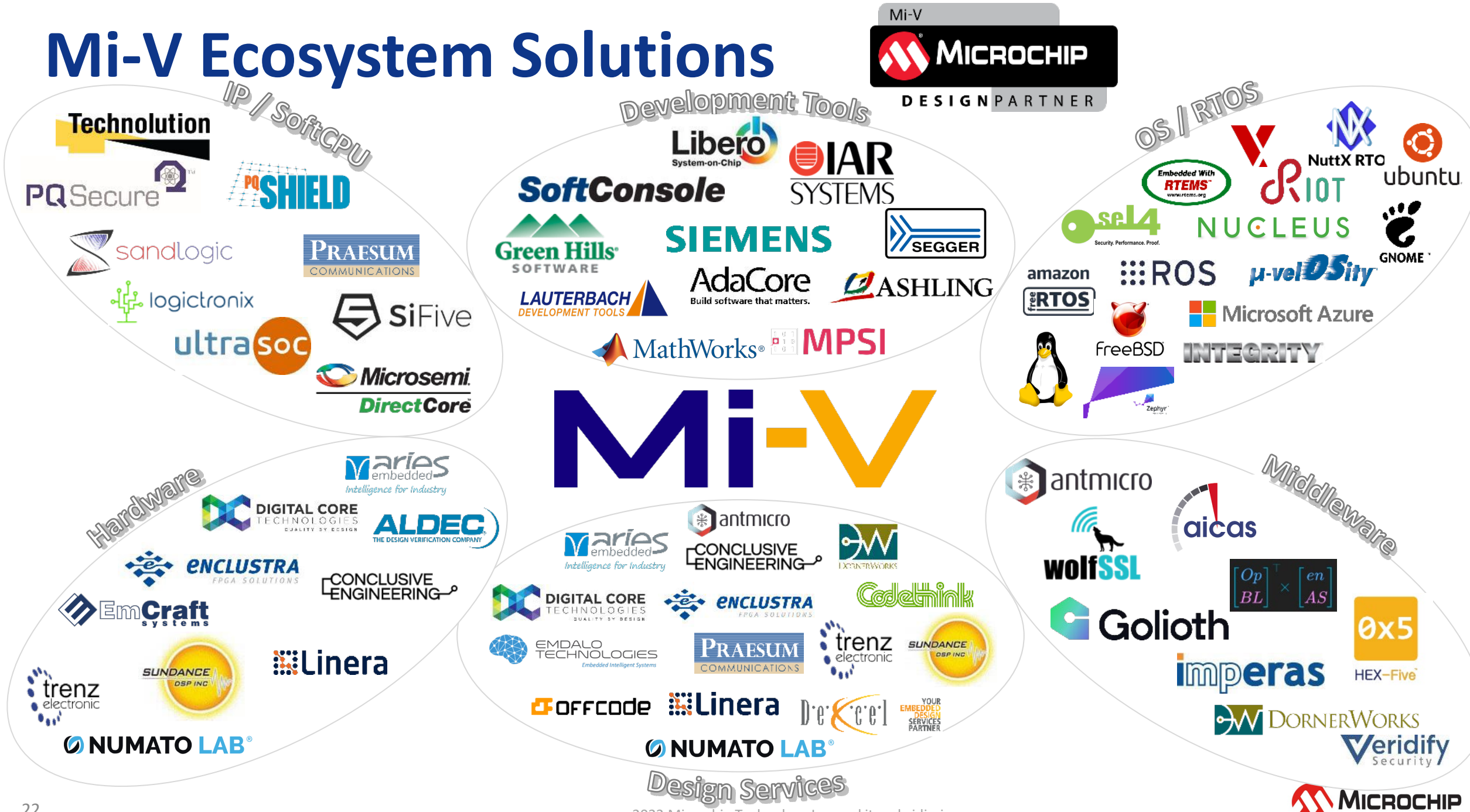
Mi-V Ecosystem Solutions

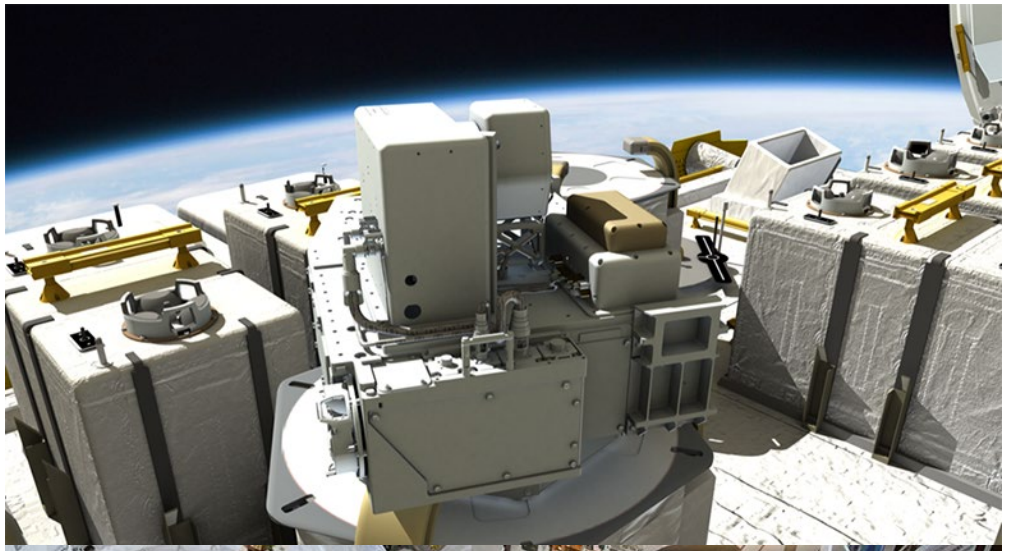


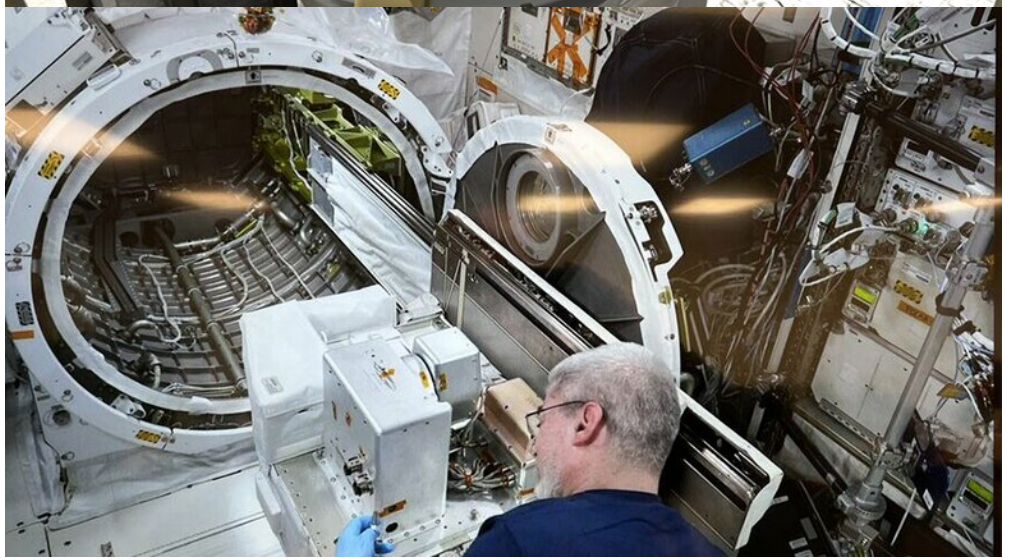
PolarFire® SoC used on Internation Space Station

- **Skycorp platform built around PolarFire® SoC FPGA device, MPFS250T**
  - a 64-bit multicore RISC-V® CPU subsystem processor using following features
    - FPGA fabric logic
    - error-correcting DRAM,
    - eMMC Flash, SD™ card,
    - Ethernet and USB systems.
  - The platform also runs the Linux Operation System (OS) in addition to FreeRTOS

- **intelligent Space System Interface Modular Coupling Kit is the "USB for Space"**
  - testing occurred on the robotic connector developed by iBoss GmbH to transmit power and data like a computer's USB cable
  - https://www.microchip.com/en-us/about/media-center/blog/2022/polarfire-international-space-station

- **system has been working successfully for over 6 months**





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The Future!

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Get Ready for More!!

HPSC: Redefining What's Possible For Space

- **NASA JPL awarded contract to Microchip to develop the next-generation High-Performance Spaceflight Computing (HPSC) processor**
- **Provides >100X compute over current solutions**
  - Based on multi-core, fault tolerant **RISC-V architecture**
- **Microchip will architect, design and deliver HPSC integrating Ethernet, AI/ML, High-Speed Standards-based Connectivity, Fault-Tolerance, Defense-in-Depth Security and Low Power capabilities**
- **Global collaboration between Microchip & Industry**
  - R&D, IP & Manufacturing in **Canada, Europe, U.S., SE Asia**
- **Target device availability in 2024**

August 15, 2022 – NASA

NASA Awards Next-Generation Spaceflight Computing Processor Contract

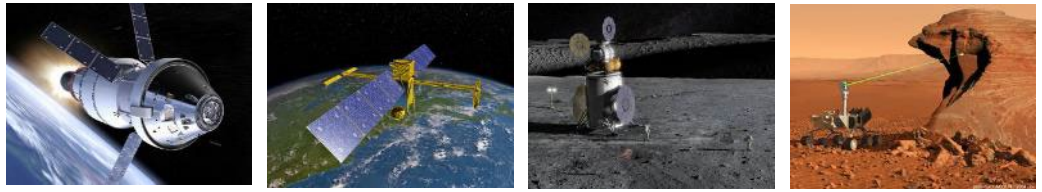

Photo courtesy: NASA

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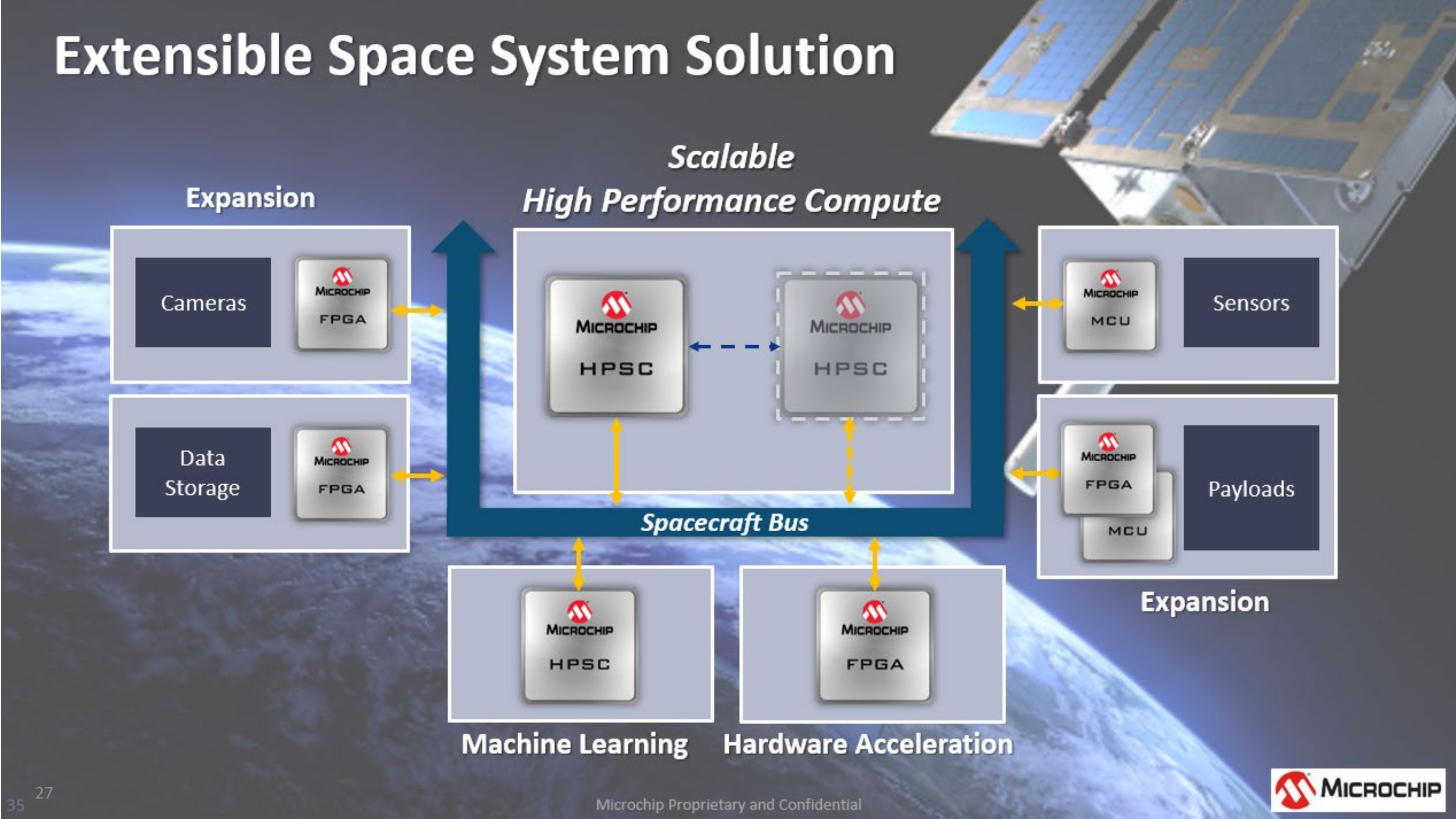
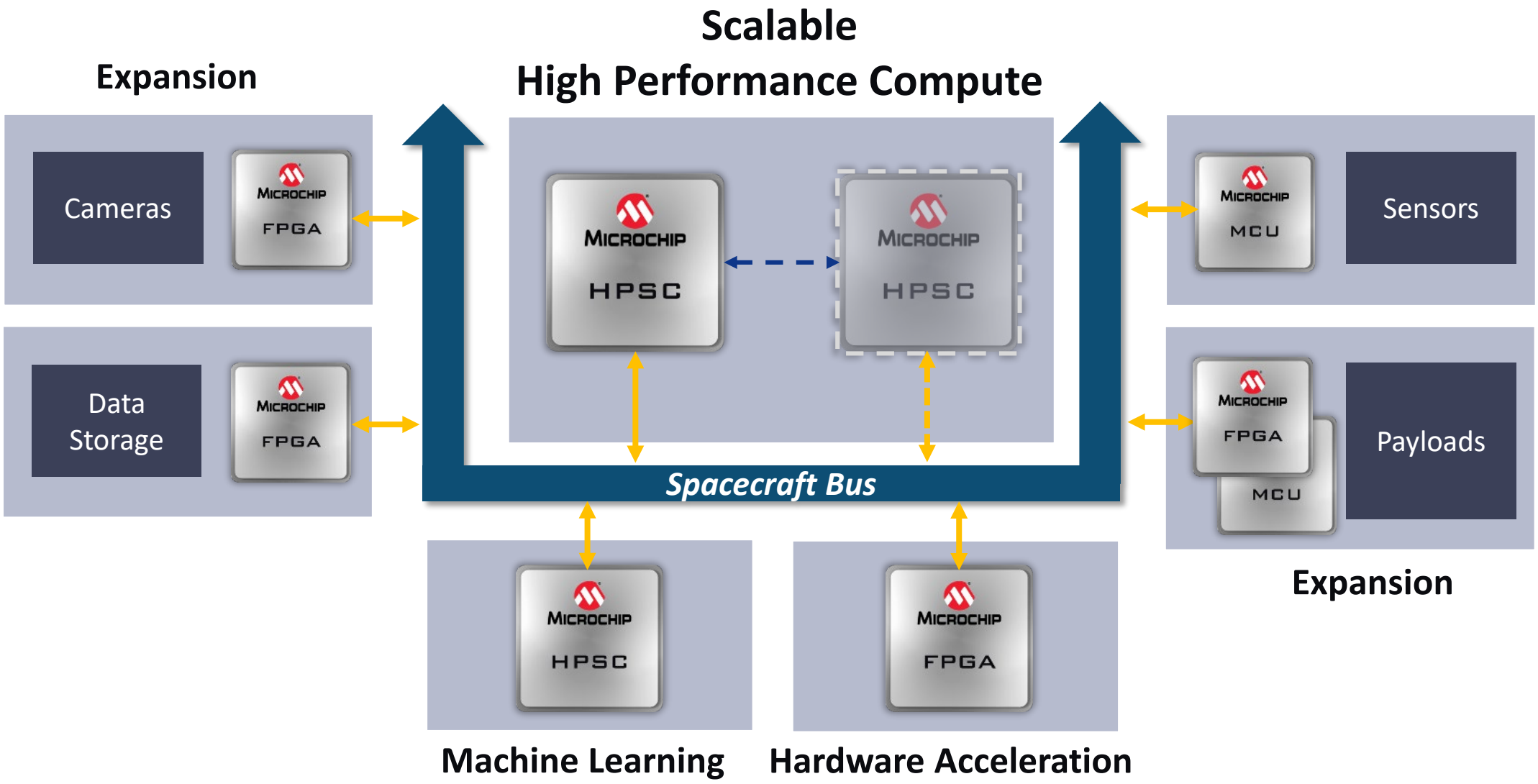
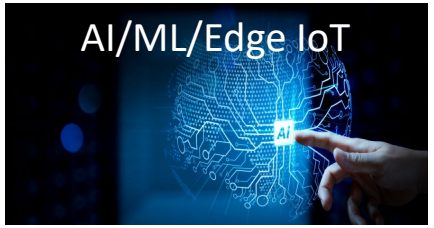
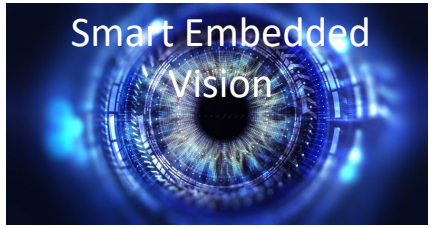
Extensible Space System Solution



Extensible Space System Solution



Needs for 100G Edge Compute with Market Leading Power Efficiency

	PolarFire® Capabilities	NEXT GENERATION	PolarFire® 2 Capabilities
	• 1-2 CNNs • Simultaneous Real Time and OS capability		• Multiple Concurrent CNNs • Multifold CoreMark® Performance Increase
	• 40G Fabric Processing • 8x8 MIMO Radio • 12G Multiprotocol Transceivers		• 100G Processing • 64x64 MIMO Radio • 32G Multiprotocol Transceivers
	• Up to 4K Video		• Up to 8K Video
	• SEU Immune • Military Grade Anti-Tamper Security		• SEU Immune • Resistant to Next Generation Threats
	• Class Leading		• Support 100G Edge Compute at SAME POWER as PolarFire®

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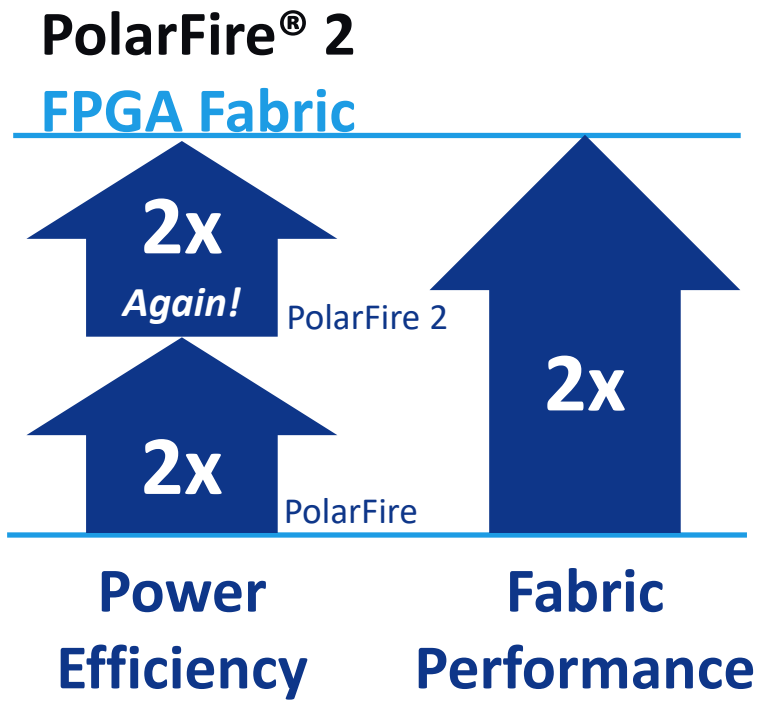
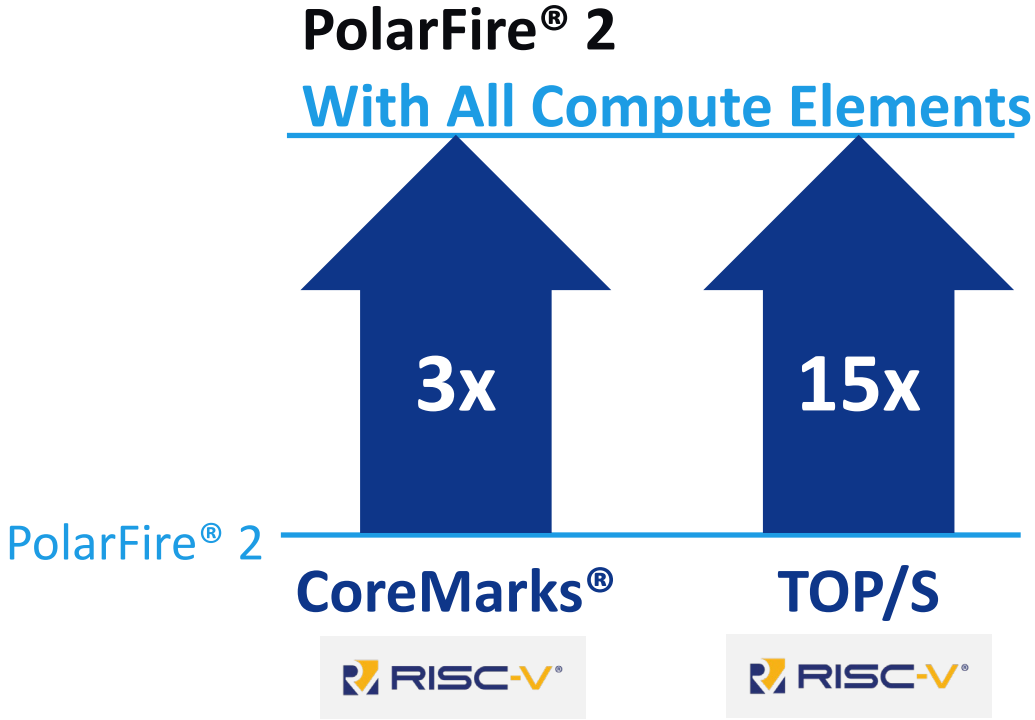
Previewing PolarFire® 2

Doubling our POWER-EFFICIENCY *Again!*



Military Grade Anti-tamper and Cybersecurity
Configuration SEU Immune



Deterministic, Asymmetric Processing
HPSC Compatible Core Complex

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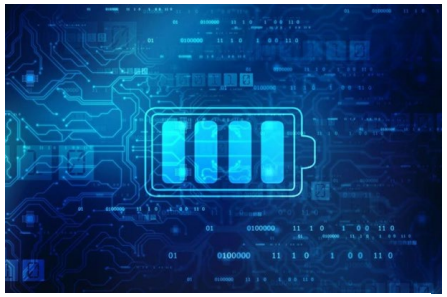
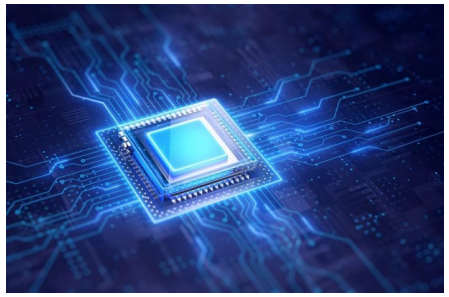
PolarFire®2 Platform Extends Mid Range FPGA Leadership

- 2x More Power Efficient Than Current Best in Class PolarFire®
  - 15X More TOP/S, 2X Fabric Performance at Same Power as PolarFire®
- Immune to SEU Upsets with Infinite Re-programmability and Partial Configuration
  - No limits to programming cycles and can re-program specific sectors
- Next Gen Military Grade Security
  - Resistant to emerging cyber and physical security threats



2x
Power Efficiency



Exceptional reliability
Zero configuration upsets

Military-grade security
Best cyber- and anti-tamper security

Provides Extensibility For
High Performance Spaceflight Computing

Summary

- **rich RISC-V offering to target FPGA**
  - Inspectable RTL
  - suitable for system critical platforms
- **Polarfire®SoC - Multiprocessing**
  - Linux and real time in a deterministic, coherent CPU cluster
- **Low Power**
  - 30-50% less than competition
- **Defense grade security/secure boot**
  - Spectre/Meltdown immune
- **Exceptional reliability**
  - All memories are protected
- **Longevity**
- **Microchip Total System Solutions**
  - Full compatibility across all platforms

Thank You!!