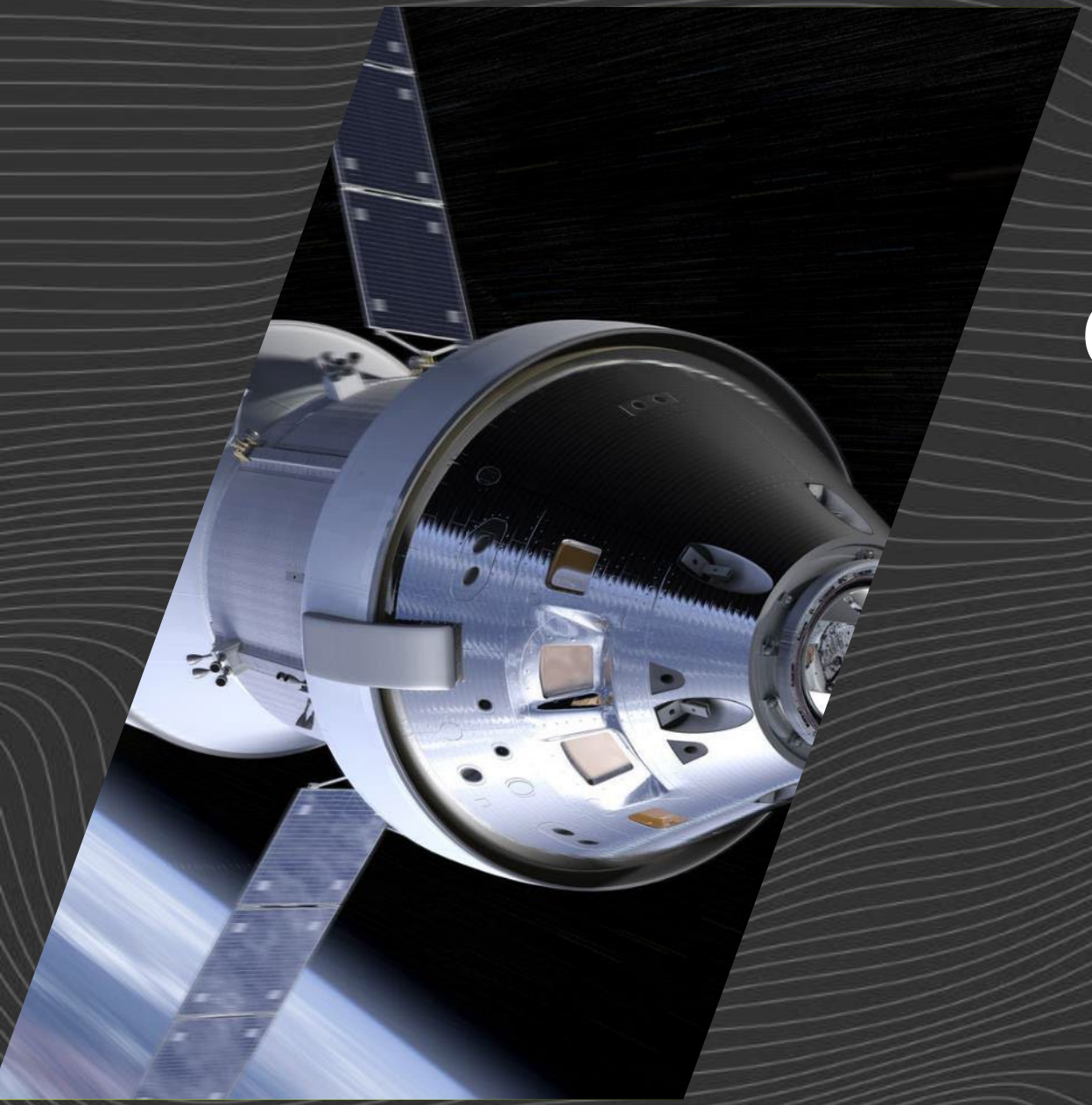

CAES PIONEERING ADVANCED ELECTRONICS

Gaisler NOEL-V SoC Applications and Ecosystem

RISC-V in Space 2022

NOEL-V Processor Core

RISC-V RV64 and RV32 Processor Model

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Characteristics:

- RISC-V 32- and 64-bit compliant processor core
- Superscalar – dual issue
- Fault Tolerance - Error Correction Codes (ECC)
- Leverage foreseen uptake of RISC-V software and tool support in the commercial domain
- Compatible with GRLIB IP Core library
- Highly configurable

Primary feature set:

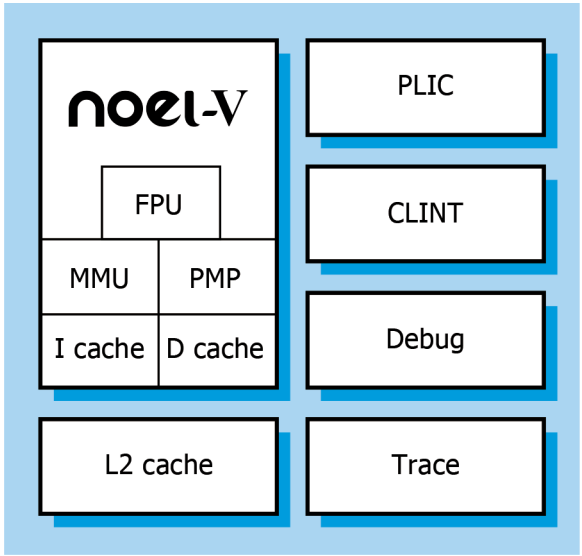
- **RISC-V RV64GCH or RV32GCH**
- AHB and AXI4 bus support

Performance

- Comparable to ARM cortex A53
- CoreMark*/MHz
  - dual-issue 4.41**
  - single-issue 3.05**

https://www.gaisler.com/NOEL-V

noel-V



* GCC9.3.0 20200312 (RTEMS 5, RSB 5 (c53866c98fb2), Newlib 7947581
-g -march=rv64ima -mabi=lp64 -B /gsl/data/products/noelv/rtems-noel-1.0.3//kernel/riscv-rtems5/noel64ima/lib --specs bsp_specs -qrtems -lrtemsdefaultconfig -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series -finline-functions -fipa-cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20

** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.

NOEL-V Processor Architecture

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RISC-V RV64(32)GCH (IMAFDCH):

- 64/32-bit Base integer instructions (**I**)
- MUL/DIV (**M**)
- Atomics (**A**)
- Single/Double Float (**FD**)
  - Slow iterative GPL FPU, or
  - Pipelined FPU
- Compressed instructions (**C**)
- Hypervisor (**H**)
- Physical Memory Protection (**PMP**)
- MMU
  - 39 bit virtual addressing
  - Separate I and D TLB, fully associative

Pipeline features:

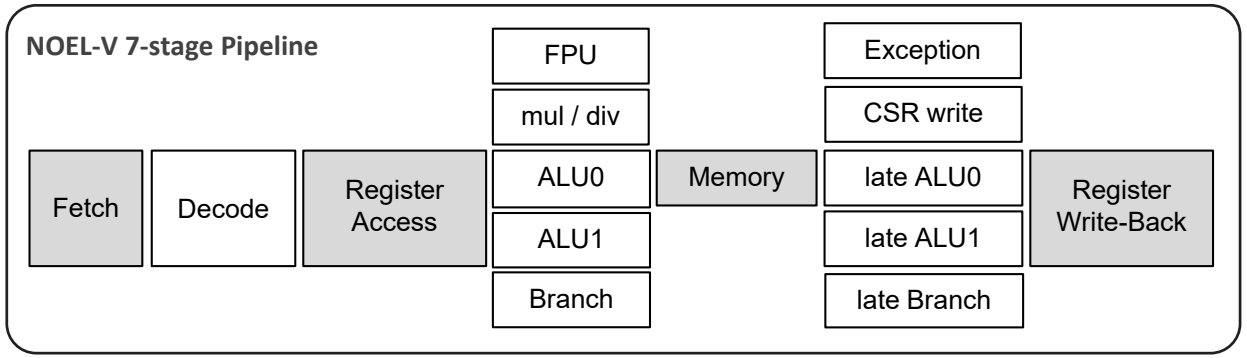
- 7-stage dual-issue in-order
- Late ALUs and branch units
- Dynamic branch prediction
  - **BTB**, **BHT**
- Return Address Stack (**RAS**)

Additional extensions:

- Bit Manipulation – standardized parts
  - **Zba**, **Zbb**, **Zbc**, **Zbs**
- Encryption – simple parts
  - **Zbkb**, **Zbkc**, **Zbkx**
- Count overflow and mode-based filtering (**Sscofpmf**)

Fault tolerance:

- SECDED on L1 caches
  - Configurable scrubbing
  - Error counting
- SECDED on register files
  - Configurable scrubbing
  - Error counting



L1 caches:

- Separate I and D caches, ASID, VIPT, LRU, write-through
- Up to 4 way, 16 kByte each
- Write buffer, snooping for coherency

RISC-V® noel-V

https://www.gaisler.com/NOEL-V

NOEL-V Configurations

The NOEL-V processor core is available as part of a subsystem that also contains system peripherals and offers some example configurations:

Configuration	Target	Architecture	Pipeline	RISC-V extensions	MMU	PMP	Privilege modes	Example SW
HP	High-performance processing	32 or 64 bits	Dual issue	IMAFDB*CH	Yes	Yes	Supervisor, User and Machine + Virtualization	Hypervisor, Linux, VxWorks
GP	General purpose processing	32 or 64 bits	Dual or single issue	IMAFDB*CH	Yes	Yes	Supervisor, User and Machine + Virtualization	Hypervisor, Linux, VxWorks
GP-lite	General purpose processing Area optimized	32 or 64 bits	Dual or single issue	IMAFDB*C	Yes	No	Supervisor, User and Machine	Linux, VxWorks
MC	Controller applications	32 or 64 bits	Single issue	IMAFDB*C	No	Yes	User and Machine	RTEMS
MC-lite	Controller applications Area Optimized	32 or 64 bits	Single issue	IMA	No	No	User and Machine	RTEMS

*only parts of the B extensions may be enabled for this configuration. See NOEL-V IP manual (grip.pdf) for more information

Notes:

- Fault-tolerance features can be enabled for all the configurations
- It is also possible to tailor additional configuration settings to create custom processor configurations by editing the VHDL generic (configuration parameter) assignments in the subsystem.

https://www.gaisler.com/NOEL-V

NOEL-V Processor Peripherals

RISC-V Debug Module (DM)

- Compatible with the RISC-V debug specification
- JTAG Debug Module Interface
- Hart Run Control
- GPR and CSR register access
- Program buffer
- Triggers (match and instruction count)

RISC-V Platform Level Interrupt Controller (PLIC)

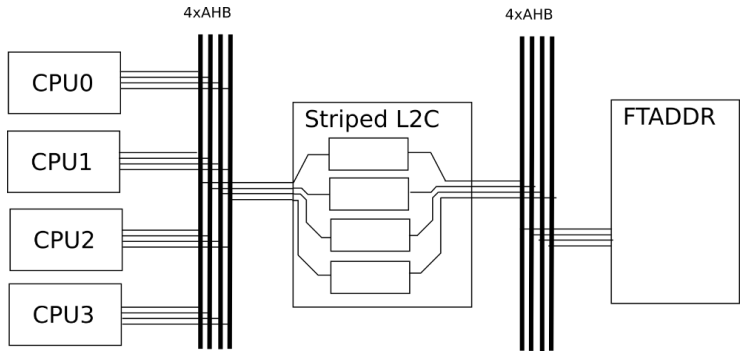
- Compatible with the Platform Level Interrupt controller specification

Also complemented by

- New DDR2 and DDR3 SDRAM controller (FTADDR23), specifically targeted for space applications
- Multi-port L2 cache extensions allowing bandwidth extensions from L1 to off-chip memory devices

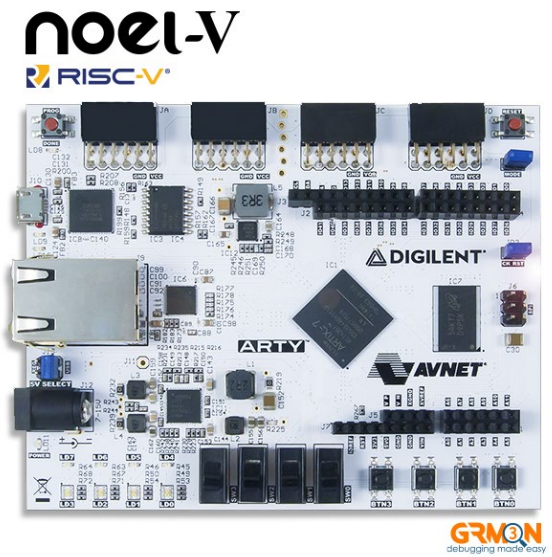
L2 cache (commercial license, -lite version as FLOSS)

- AHB or AXI4 back-end
- Up to 128 bit wide frontside and back-end
- LRU or pseudo-random
- Up to 4-way associativity and 2 Mbyte
  - Can be split between cores
- Address range configurable
  - Write-through
  - Write-back
  - Uncacheable



NOEL-V IP availability

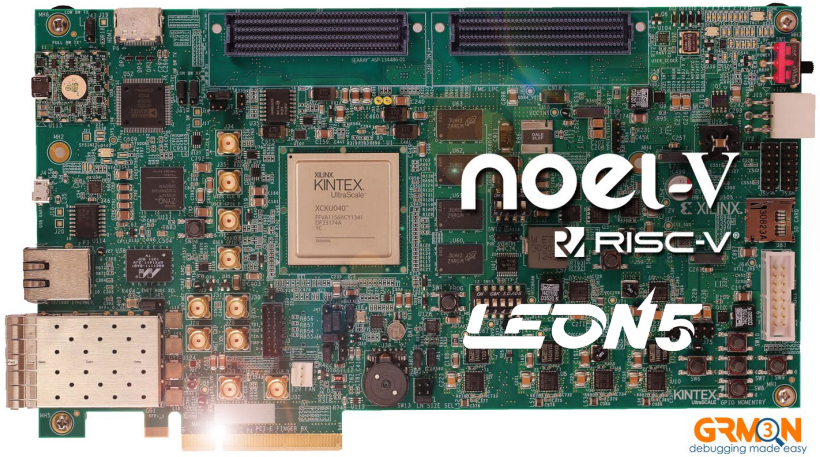
- NOEL-V is available as part of the GRLIB IP library
  - Dual licensed IP library: GPL variant available at gaisler.com/getgrlib
  - Commercial variants of the library available for different applications (COM, FT-FPGA, FT)
  - The library includes infrastructure for project file generation for most popular EDA tools and SoC template designs
- FPGA bitstreams for Xilinx and Microchip FPGA evaluation boards are available for download
- Debug monitor and software toolchains (Bare-C, RTEMS, Linux, …) are also available



NOEL-ARTYA7

LEON-PF

NOEL-PF



LEON-XCKU

NOEL-XCKU

LEON5 and NOEL-V silicon proven on STM 28nm GEO P2

Rad-hard demonstrator with LEON5FT SPARC V8 32-bit processor and NOEL-V RISC-V 64-bit processor

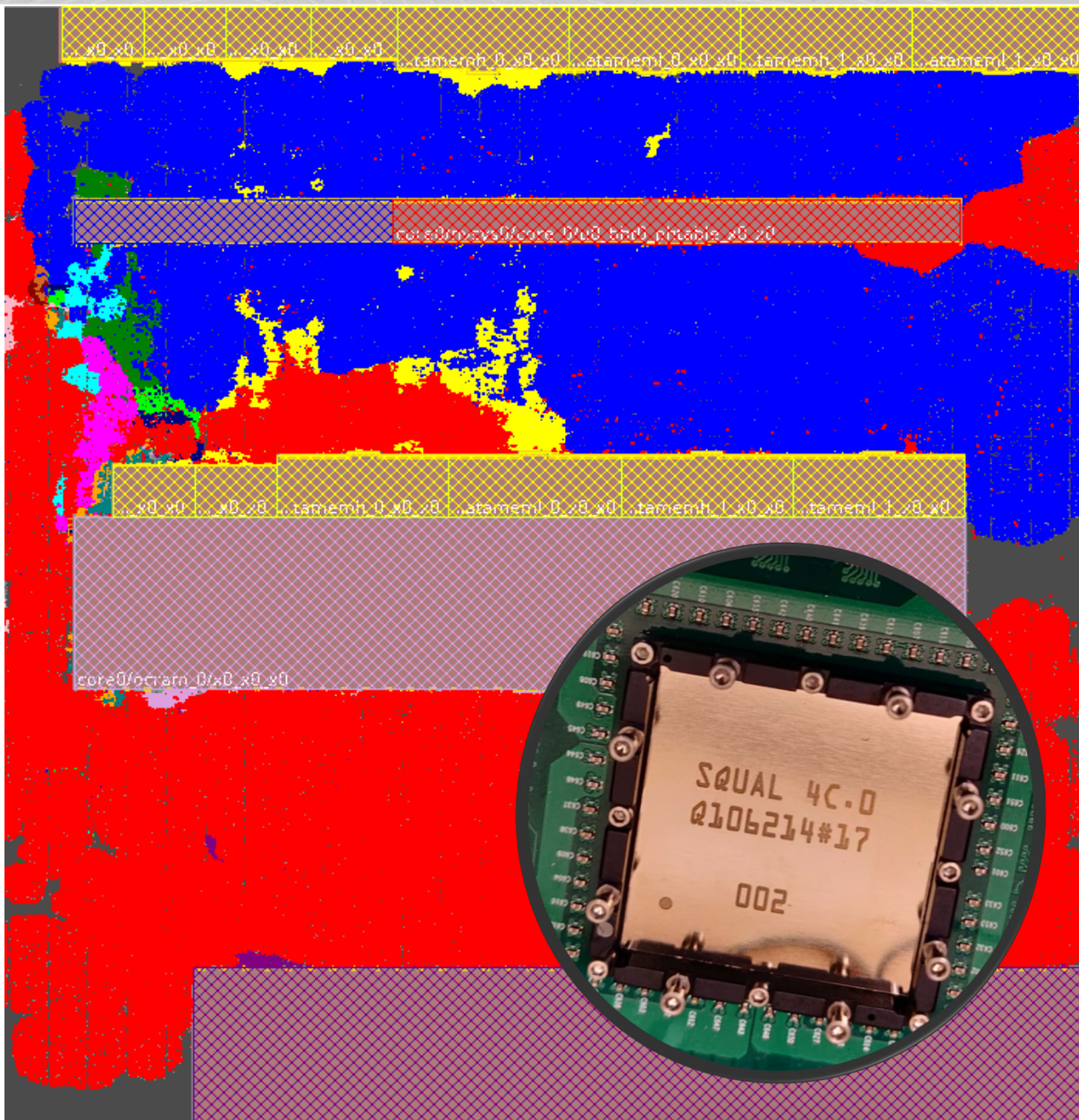
- ST 28nm FDSOI GEO P2 technology
- Specialized design with LEON5 and NOEL-V sharing resources, consumes less than 1 mm^2
- Proves implementation on target technology
- Technology hardness and processor core fault tolerance features demonstrated through SEE test campaign
- Collaboration between STM and Gaisler R&D teams
- Manufactured using European supply chain, fab in Crolles (FR)

Performance attained LEON5/NOEL-V:

- Typical corner: 1 GHz / 800* MHz
- Worst-case corner: 600 / 500* MHz

Schedule

- Test chips available at Gaisler
- Performed SEE characterization
- Test chip will be included in GOMX-5 LEO in-orbit experiment



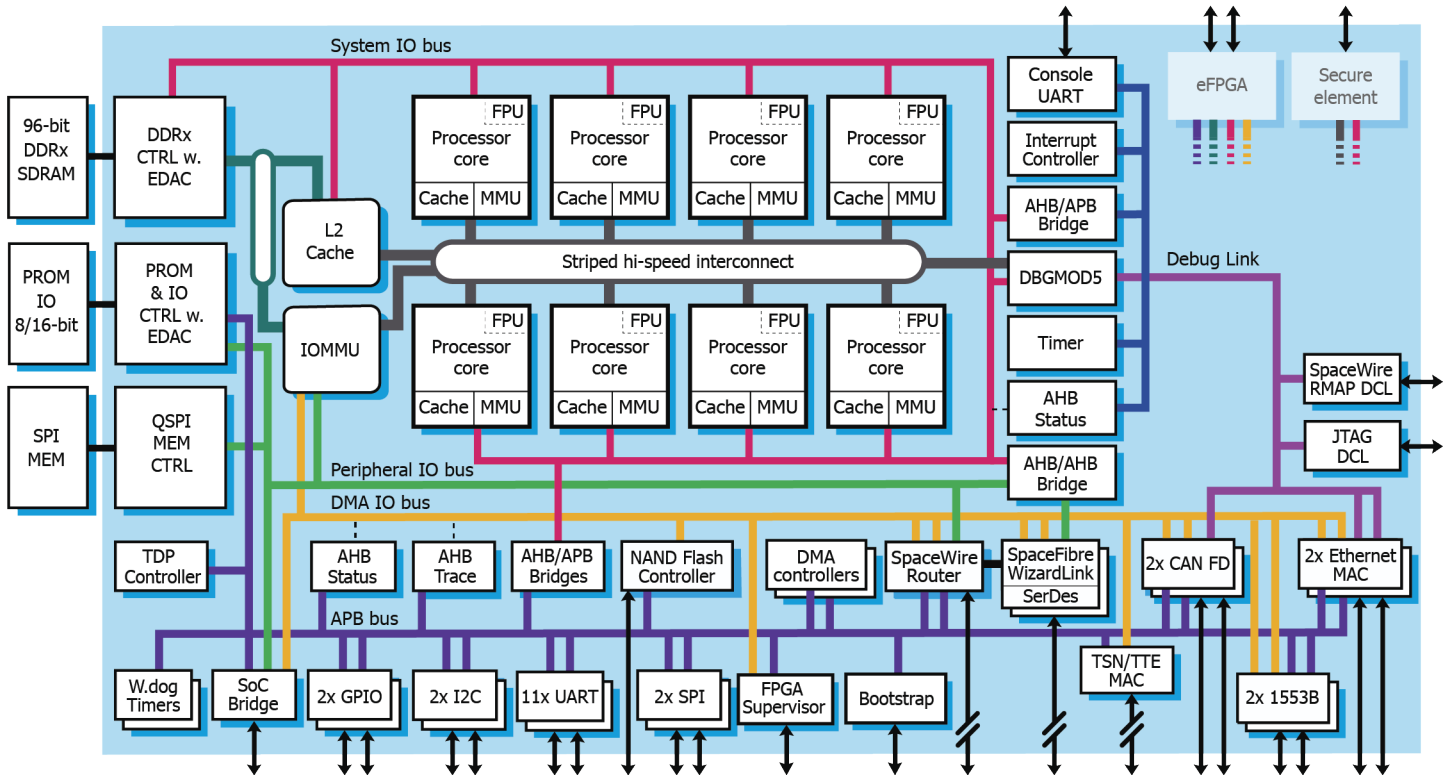
* Following this tape-out, NOEL-V has been further optimized and future implementations are expected to match LEON5 operating frequency.

GR765 – Octa-Core Processor

In development
No guarantee of product launch

Baseline Features

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- **1 GHz processor frequency - 26k DMIPS**
- 2+ MiB L2 cache, **512-bit** cache line, 4-ways
- **DMA controllers**
- **DDR2/3 interface with dual x8 device correction capability**
- 8/16-bit PROM/IO interface
- **(Q)SPI and NAND memory controller interfaces**
- **Secure Element, providing Secure (authenticated) boot (TBD)**
- **eFPGA ~30k LUT (TBD)**
- **High-pin count – LGA1752 package allows reduction of pin sharing**
- **Target technology: STM 28nm FDSOI**



GR765 – Octa-Core Processor

Baseline Features

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8 or NOEL-V RV64GCH**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- **1 GHz processor frequency - 26k DMIPS**
- 2+ MiB L2 cache, **512-bit** cache line, 4-ways
- **DMA controllers**
- **DDR2/3 interface with dual x8 device correction capability**
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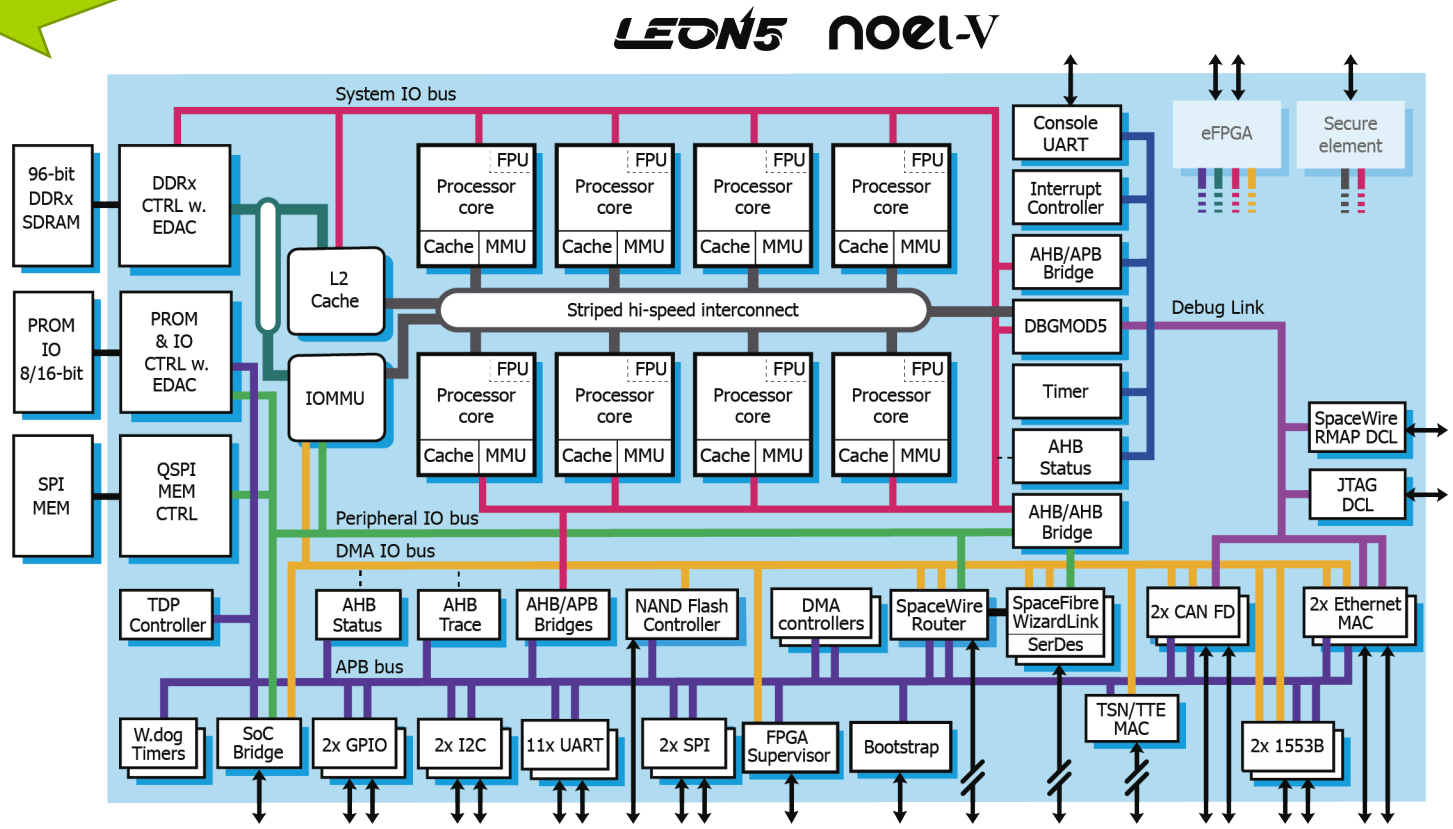


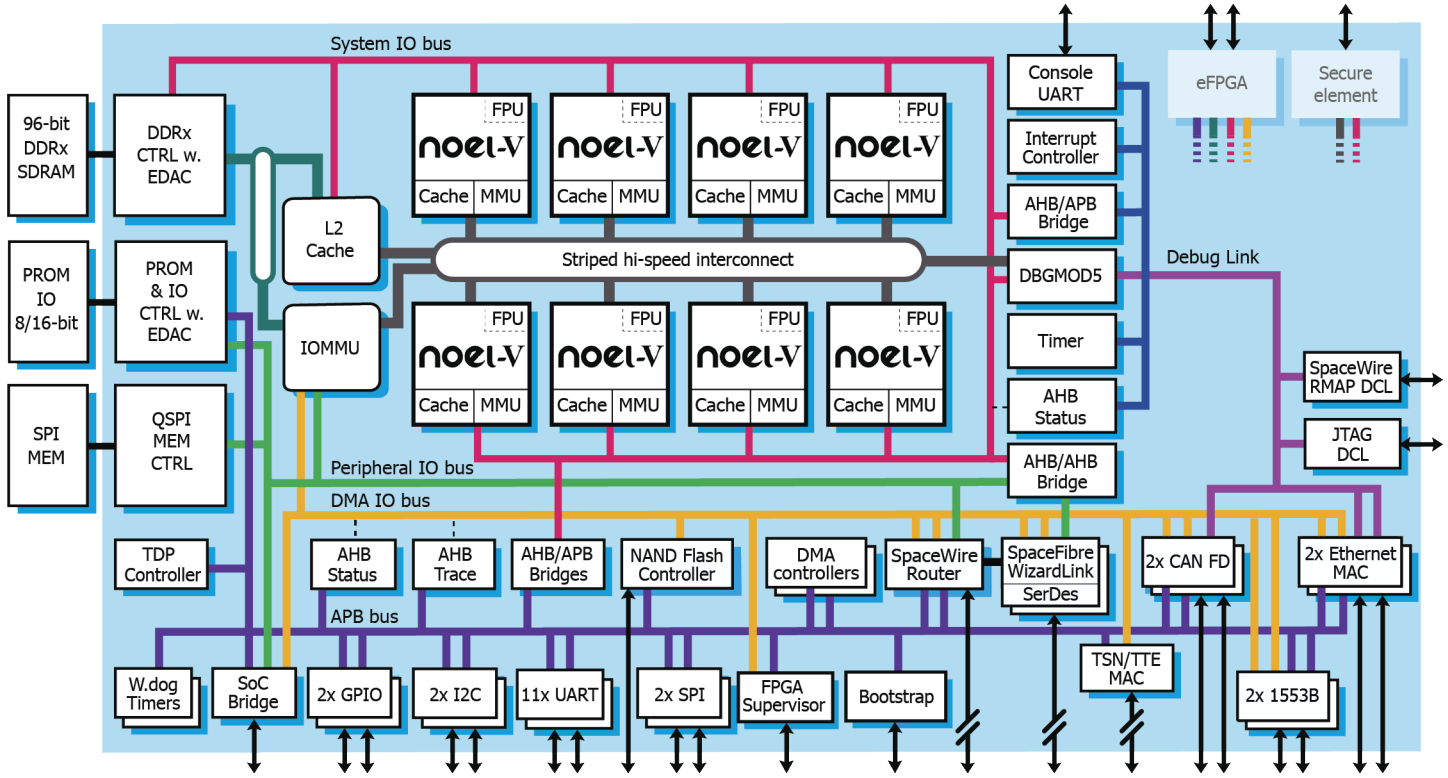
SPARC RISC-V®

GR765 – RISC-V Mode

In development
No guarantee of product launch

GR765 in RISC-V mode

- NOEL-V processor core provides the same microarchitectural improvements as the LEON5FT
- NOELV/GR765 provides RISC-V compatibility through conformance to the OS A (Embedded) RISC-V Platform Specification
- RV64GCH – 64-bit processor
  - 64 Base integer instructions (I)
  - MUL/DIV (M)
  - Atomics (A)
  - Half/Single/Double Precision Float (Zfhmin, FD)
  - Compressed instructions (C)
  - Hypervisor (H)
  - Bit manipulation (subset of) (B)
  - Physical Memory Protection (PMP)
  - MMU - 39 bit virtual addressing, separate I and D, fully associative, TLB
- RISC-V Advanced Interrupt Architecture (AIA)
- RISC-V IOMMU
- RISC-V Debug Module (DM)
- Cybersecurity features and Extended monitoring



Software

- Complete ecosystem
- A combination of Gaisler and 3rd party software

Tool chains, Operating systems and compilers

- Bare-C
- Linux
- RTEMS
- VxWorks
- Zephyr

Partner software

Time-and-Space Partitioning:

- FentISS XNG
- SYSGO PikeOS
- Wind River VxWorks RTOS

Boot loaders

- GRBOOT
- GRBOOT-STANDBY
- MKPROM2

Development tools

- TSIM3 simulator
- GRMON3 debugger
- GCC compilers
- LLVM/Clang compilers

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Development tools

- TSIM3 simulator
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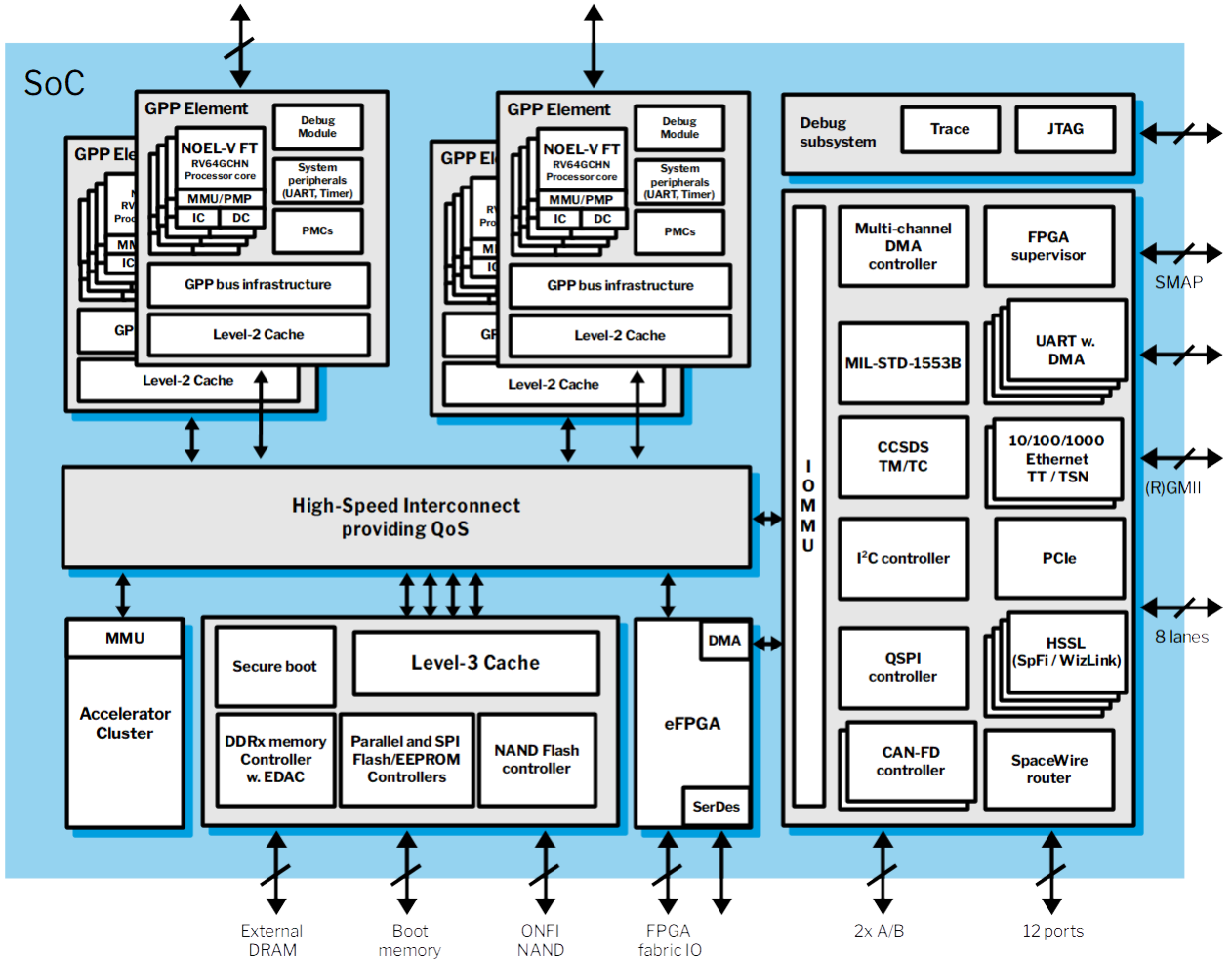
- LLVM/Clang compilers

GR7xV – 16-core NOEL-V Processor

- Fault Tolerant 64-bit RISC-V Hexadeca-core with islands (GPP elements) of four general-purpose processors each with dedicated L2 caches
- Accelerators for high-performance computation
- Architectural design currently performed within GR7xV activity within ESA ARTES programme
- Extends architecture applied in De-RISC and SELENE projects (H2020)
- Work on architecture also continues within EUMMSS (SNSA)
- Prototype implementation planned within DUROC project

In development
No guarantee of product launch



Summary

- NOEL-V is extensively configurable and portable between technologies and is immediately available
- Applied in designs targeting space applications and also terrestrial products
- One of the most feature complete open-source implementations available?
- Dual licensed in the same way as LEON line of processors – FT features kept proprietary
- Supported by Gaisler teams with decades of experience working with customers on SoC designs targeting FPGA and ASIC.
- Fault-tolerant radiation-hardened ASSP implementations scheduled for 2024 availability
- Bitstreams, RTL, and software: www.gaisler.com/NOEL-V

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