SiFive® Intelligence ™ X280

Optimized efficiency and control for the future of Space Exploration

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Why RISC-V?

- Open ISA: The only major global compute platform on an open standard
- Single ISA scales from microcontroller to datacenter
- Provides a faster, cleaner, more modern architecture, with software portability
- Taught in all Top Universities in US
- Ecosystem of the Future
  - 3200+ RISC-V Foundation members across 70 Countries

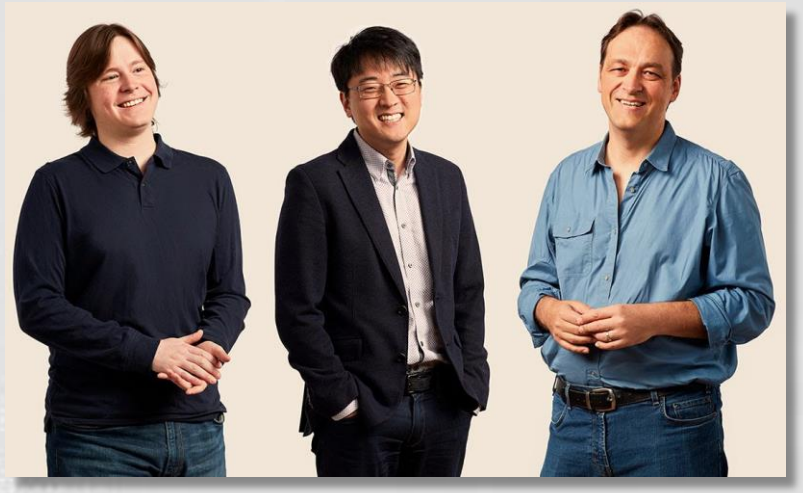
"Based on the already sizeable adoption of RISC-V, we forecast that the market will consume a total of 62.4 billion RISC-V cores by 2025"

- Semico Research

Why SiFive

- SiFive: RISC-V Founder and Brand Standard
- SiFive: US-Based Company
- SiFive: Builds on top of RISC-V and offers significantly (30-40%) more efficient power consumption and area at the same performance level versus competitive IP
- SiFive: Focused on higher performing cores (both scalar and vector performance)
- SiFive: Driving new markets including data-centric compute, aerospace, datacenter, automotive and AI
- SiFive: Strong ties into RVI resulting in rapid state of the art architecture implementation

The inventors of RISC-V!



SiFive's founders are the same UC Berkeley professor and PhDs who invented and have been leading the commercialization of the RISC-V Instruction Set Architecture (ISA) since 2010

Recognized as the
Most Respected Private Semiconductor Company
2018, 2019, 2020, ***2022***

Dedicated Focus on Aerospace and Defense

- **10+ A&D Design Wins**
  - RAD Hard FPGA for Satellite, Satcom etc.
- **20+ Engagement Opportunities**
  - Missile/Fire Control, Radar, HPC, Smart Munitions, Drones…
- **Invited and participating in DARPA Toolbox Initiative**
  - Increases access to Critical Tools, IP to Accelerate Innovation
- **Head of A&D Business Development Hired**

SiFive: Undisputed leader in RISC-V computing

Broadest portfolio of processors from embedded to high-performance computing

CPU Cores

SiFive Essential™

32 and 64-bit Processors

- Microcontrollers, IoT devices, real-time control, control plane processing
- Highly customizable to application specific requirements

SiFive Performance™

64-bit Application Processors

- Consumer, networking, infrastructure, enterprise
- Highest performance, most advanced RISC-V processor available

AI Cores

SiFive Intelligence™

Scalable 64-bit AI Processors

- Image processing, edge AI, cloud, training, inference
- High performance and efficiency for AI workloads with vector processing

Functional Safety

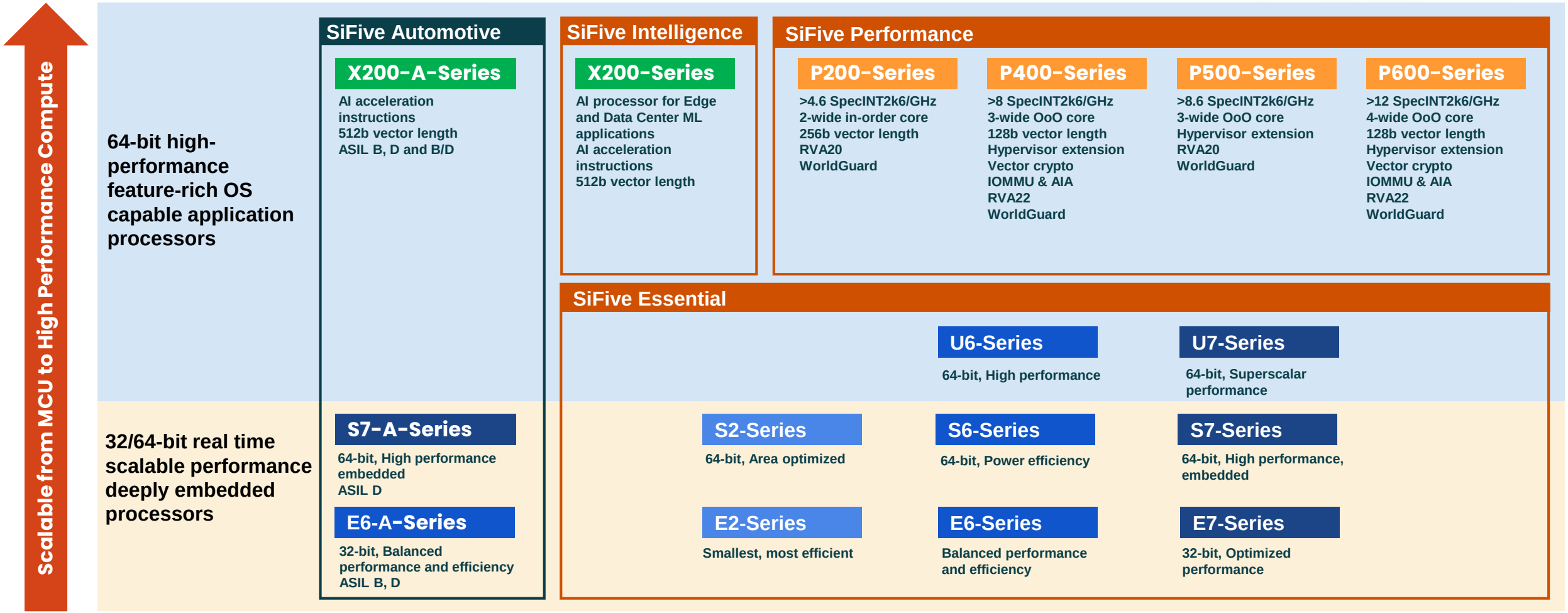
SiFive Automotive™

32/64-bit Safety Processors

- Broadest range of RISC-V safety processors
- Multi-core/cluster, vectors, virtualization, and security features
- Strong automotive RISC-V ecosystem

SiFive RISC-V Processor IP Portfolio

The Industries Broadest RISC-V IP Portfolio



SiFive® Intelligence™ X280 Processor

Optimized for the modern workload

- Enabling highly efficient, simpler system design
- SiFive leads industry with RISC-V features and AI acceleration
- Highly optimized for AI models and software frameworks
- Ideal companion to custom AI hardware accelerators
- RISC-V Vectors enable market leading performance and power efficiency
- Industry momentum in image processing through to data center compute

Market requirements for aerospace and defense

Autonomous rovers, vision processing, space flight, and guidance systems

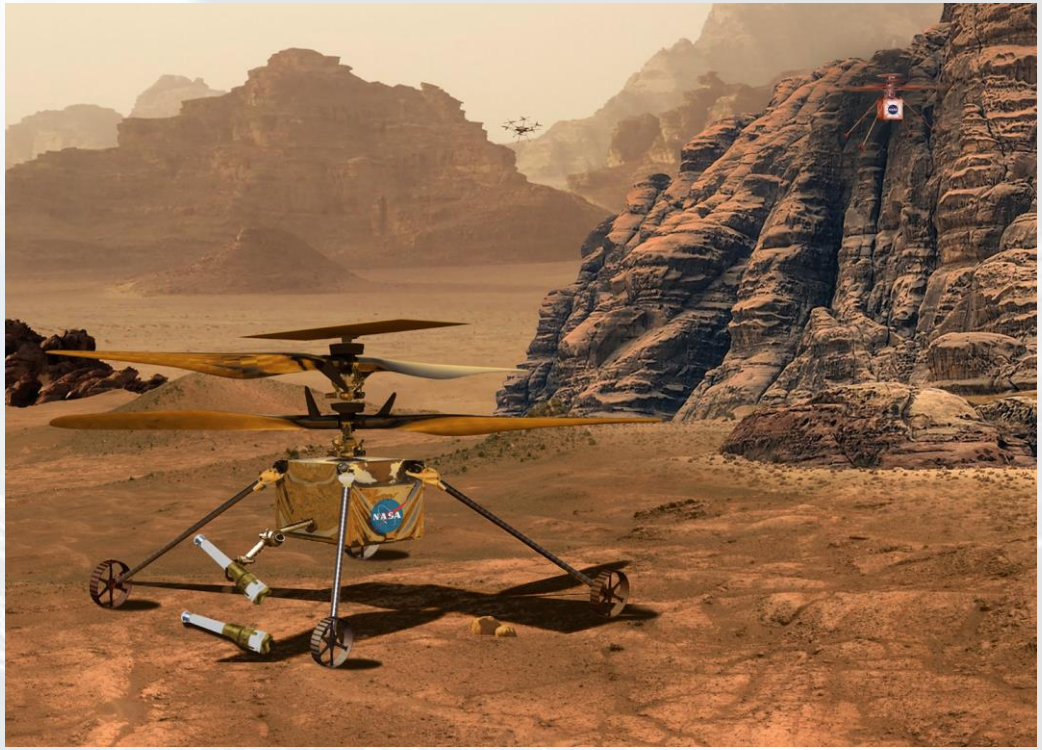


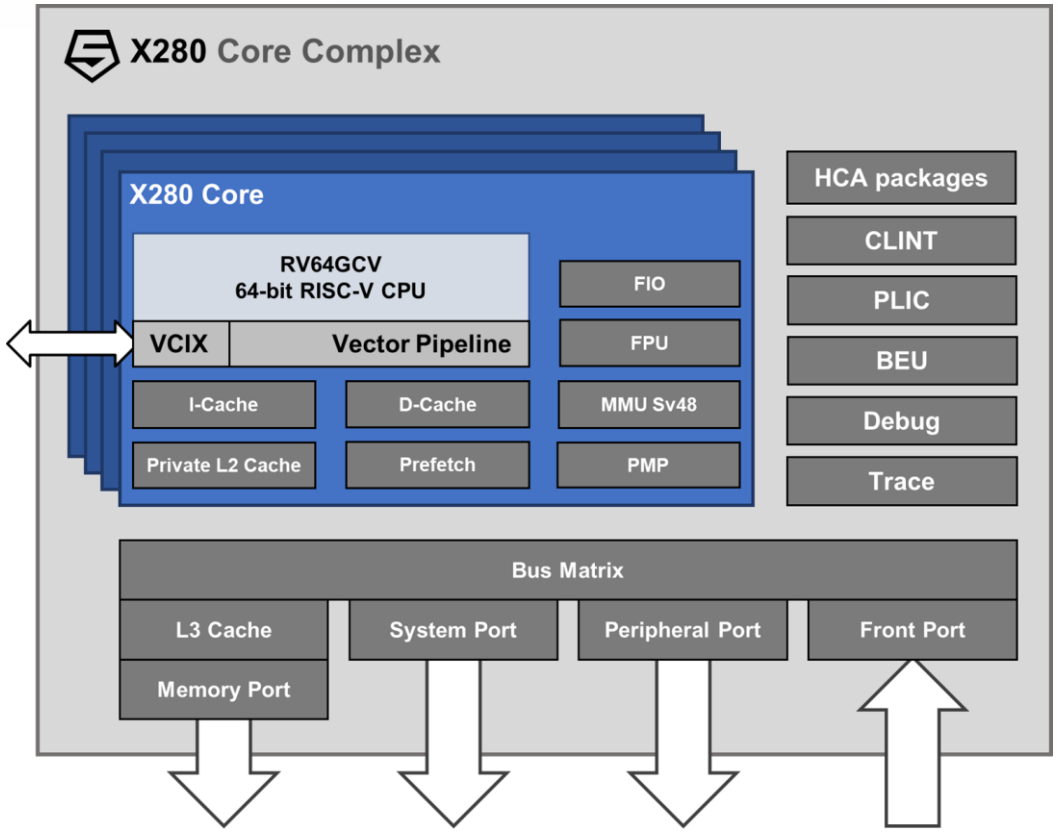
Image source: NASA

Robust operation in harsh environments

- Evolving requirements demand higher performance, future proof SoC
- Application and vector processor offering performance in fully programmable solution
- Vector processing brings advanced AI at the edge
- Multi-core, multi-cluster config for performance scalability and redundancy
- Open, standard software, for long term development

SiFive Intelligence X280 key features

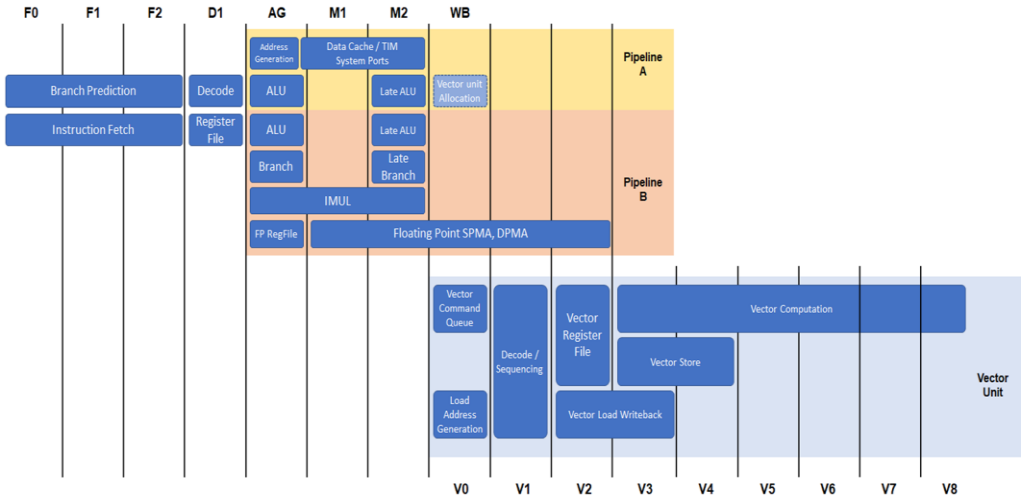
- Scalar processing
  - 64-bit RISC-V ISA, 8-stage dual-issue in-order pipeline
  - Linux capable applications processor with MMU & caching architecture
- Vector processing for AI/ML workloads
  - SiFive Intelligence Extensions, custom instructions that accelerate AI/ML performance critical operations
- 512-bit vector register length
  - RISC-V Vectors variable vector length computation supported, up to 4096-bits
- Performance
  - 5.8 CoreMarks/MHz 3.3 Dhrystone/MHz
  - 4.5 SpecINT2006/GHz 3.4 SpecFP2006/GHz (HiPerf config)
  - 4.8 TOPS (INT8 Matrix Multiplication)
- High performance memory subsystem
  - Multi-layer caching support for optimum data movement
  - Virtual memory support, up to 48-bit addressing
- Multi-core processor configuration with up to 16-cores



Best in class for combined scalar and vector performance

Overall computation performance outperforms the competition

- Many space compute algorithms require a mix of scalar and vector computation
- X280 scalar pipeline and vector pipeline are loosely coupled
- The scalar pipeline/ALU utilizes an optimized L1 Cache
- Vector unit streams from private L2 cache allowing the scalar ALU and vector ALU to both operate and access data in parallel.

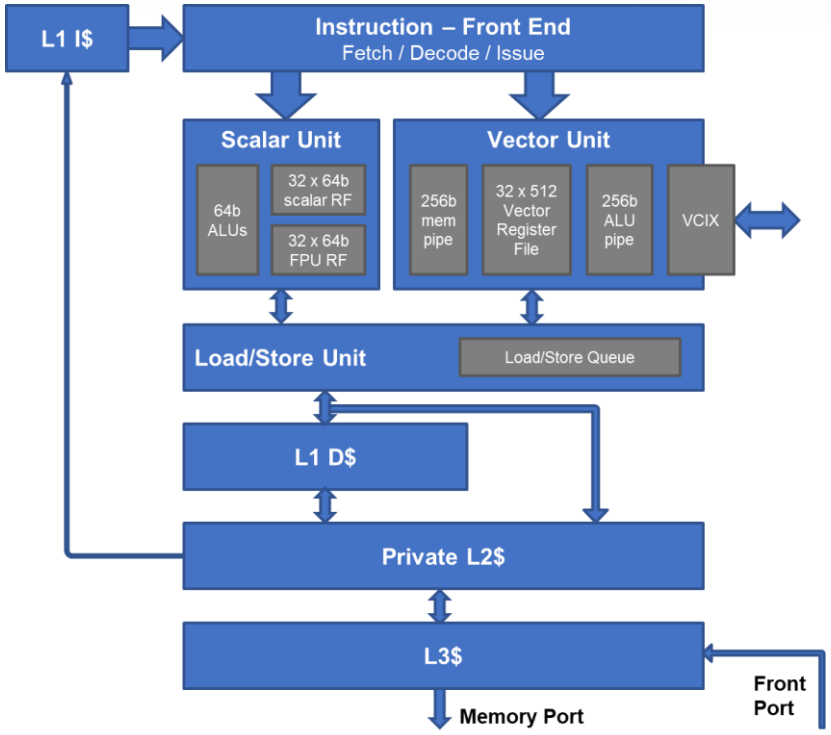


X280 shows industry-leading performance on typical space compute algorithms

X280, a highly optimized vector computation machine

X280 vector computation performance

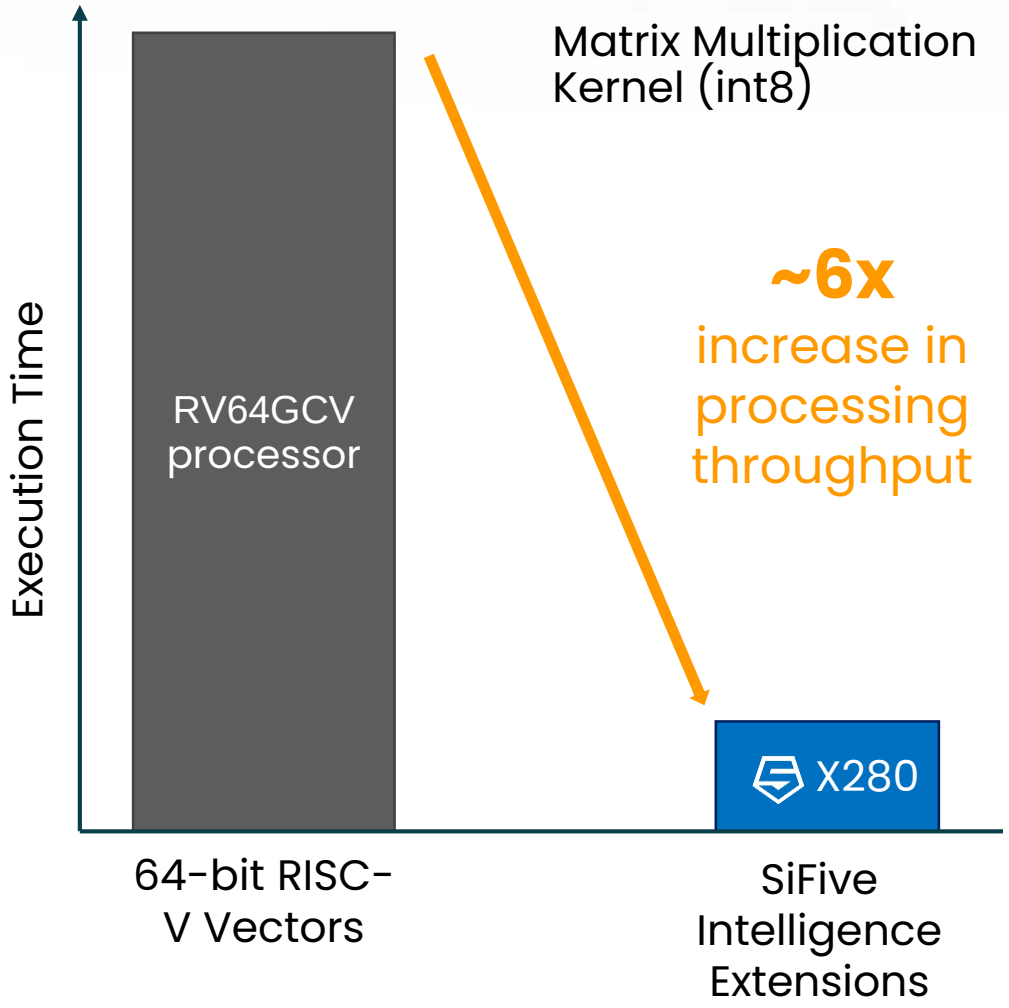
- Implements RISC-V Vector (RVV) ISA (version 1.0)
- Hardware vector length of 512-bits and software vector length of 4096-bits.
- Supports a broad range of datatypes, including integer, fixed point and floating point, as well a bfloat16, which is particularly useful in AI applications.
- By enabling its users to dynamically change the data size, RVV has a significant advantage over traditional SIMD
- SiFive Intelligence extensions add enhanced functionality such as native matrix multiplication
- Direct vector operation interface to customers hardware accelerators and instruction extensions with VCIX



SiFive Intelligence Extensions

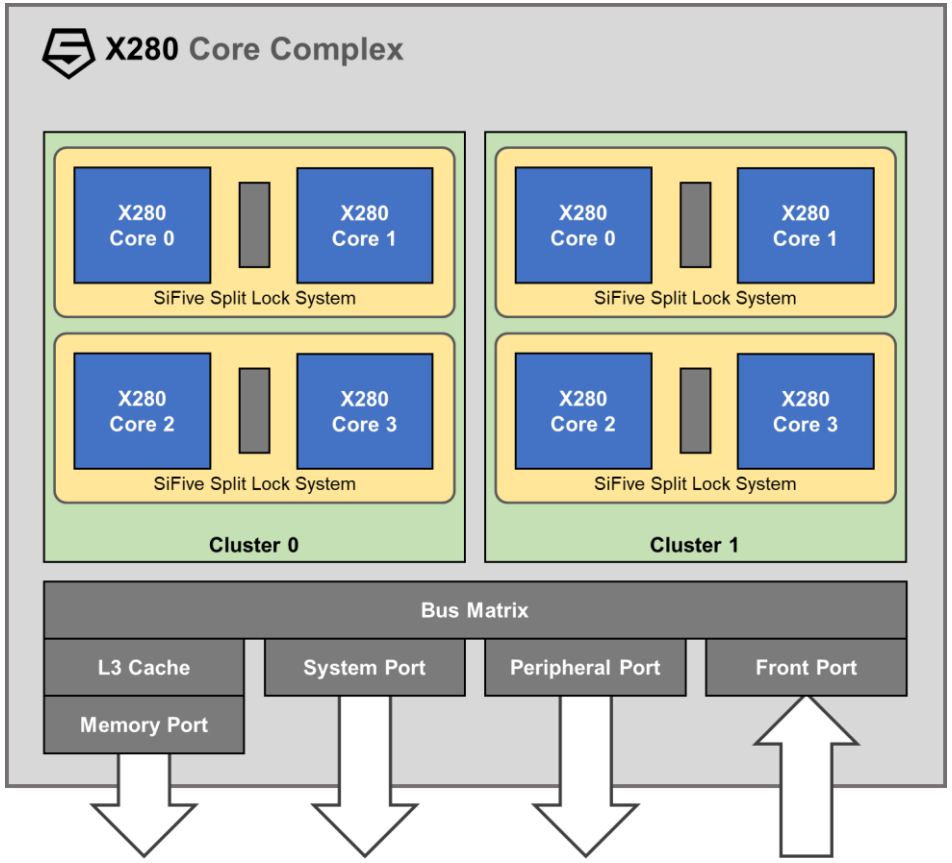
Acceleration instructions for matrix computation

- Large number of key space compute algorithms include matrix operation algorithms
- SiFive Intelligence Instructions add accelerating Matrix Multiplication (MatMul)
- [4][4](INT32) += [4][8](INT8)*[8][4](INT8)
  - [4][8] Matrix is 32 entries each INT8, 256bits
  - Fully utilizes a 512-bit vector register
  - Performs 128 MAC computation per cycle
  - Result as 16 elements of INT32, 512-bits per cycle
- Hybrid Quantization for FP32 to INT8
- Supported with LMUL1, 2 and 4
  - Software vector length extension
  - Single instruction, longer vector data length, smaller code size
- SiFive Intelligence extensions, coupled with X280 scalar, vector enables 60x performance improvement on key optimized space computer algorithms



X280 safety innovation – SiFive Split-Lock

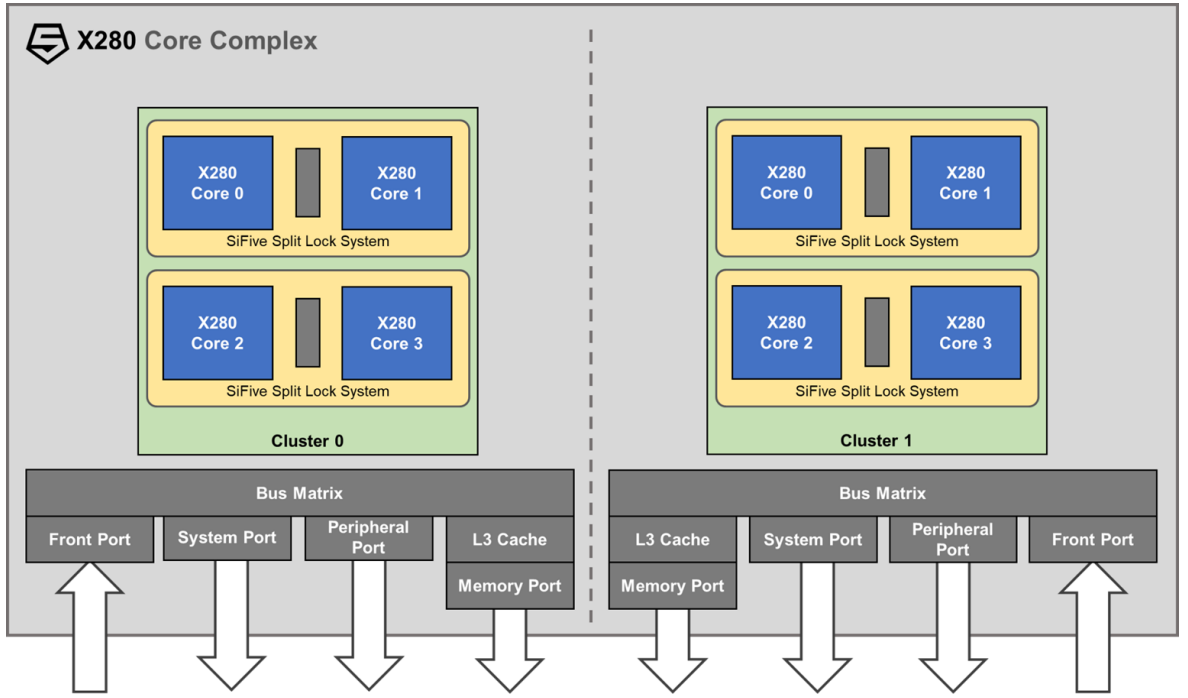
- Space electronics are particularly at risk from the effects of alpha particles or cosmic rays
- SiFive Split-Lock allows a pair of cores in a system to operate in either separate core mode or Dual Core Lock Step (DCLS) mode to offer additional redundancy to systems
- DCLS is used to detect system detect logic failures.
- Monitoring of outputs within Lockstep logic will identify a logic failure if the compared results are not identical
- Once a logic failure is detected the broader system will be responsible for any further appropriate application corrective actions



X280 safety Innovation – Cluster Isolation

Enhanced fault tolerance and isolation techniques

- Cluster isolation feature isolates a pair clusters so a core in one cluster cannot access a core in the other cluster thus providing complete isolation.
- If a core is making an incorrect access due to a random fault then the hardware will block these accesses while still enabling the clusters to be reset independently.
- When the pair of clusters are isolated the Level 3 shared cache is specifically split into 2 regions



SiFive Intelligence X280 advancing space exploration

Workload balancing

Scalar processing combined with RISC-V Vectors deliver market leading performance and power efficiency

Industry-leading performance

Best-in-class performance in typical spaceflight compute algorithms

Open software standardization

Full Linux capability simplifies programmability and tooling

SiFive continuous innovation

Multi-core, multi-cluster, Redundancy, Safety, Intelligence Extensions

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Thank you

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