Technolution

FreNox RISC-V

processor implementations for secure and reliable applications

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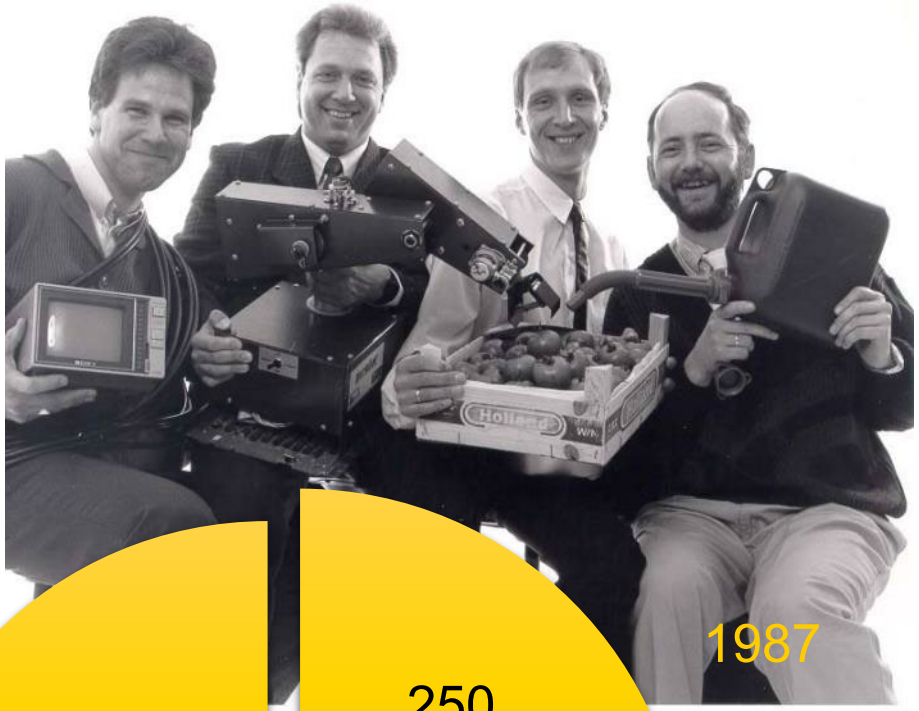
Redefining **solutions**

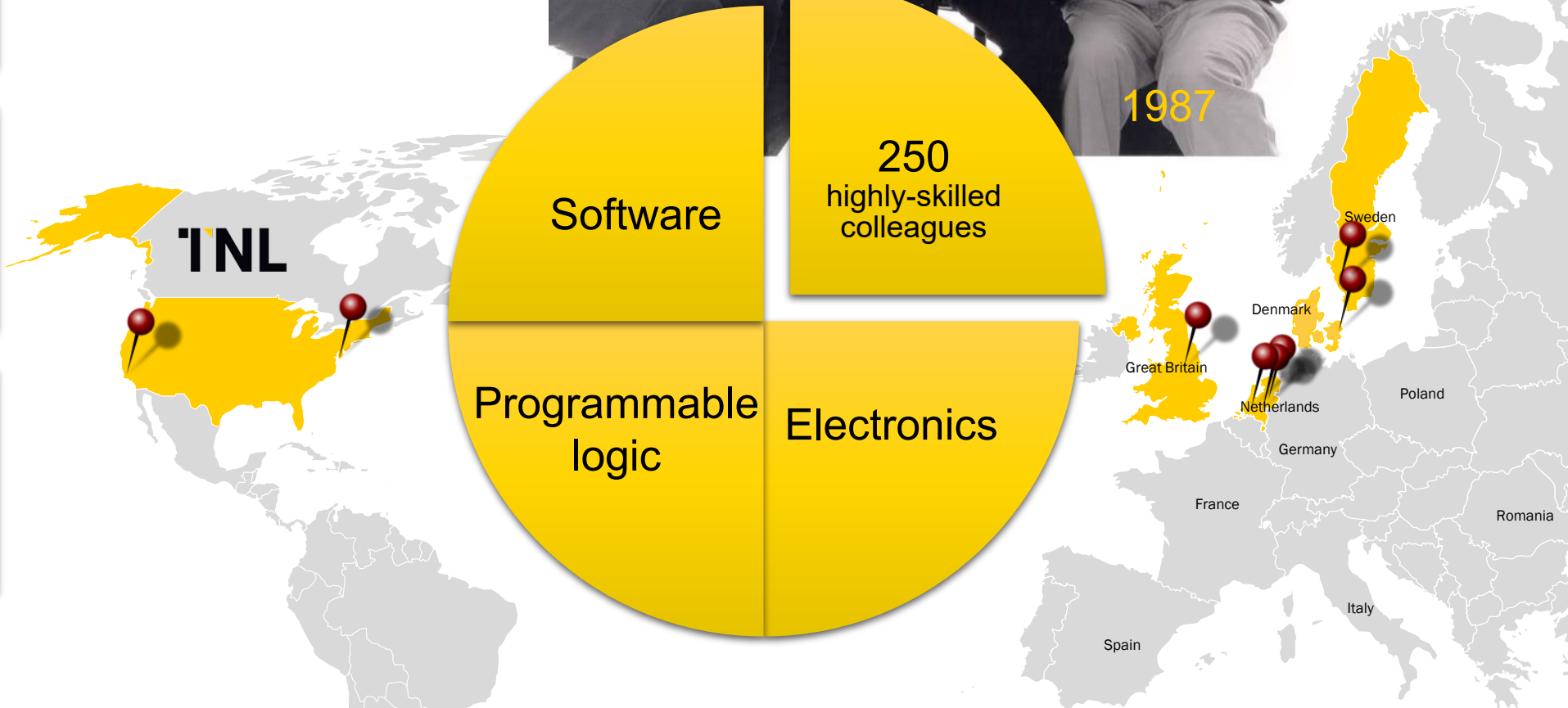
About Technolution

Passion for technology

Solutions that matter

Reliable technology





Software

250 highly-skilled colleagues

Programmable logic

Electronics

Technolution Advance
High-tech & big science

Technolution Prime
Security

Technolution Perform
Manufacturing

High-speed data acquisition & control

Classified line encryption & network diodes

AI computer vision & predictive maintenance

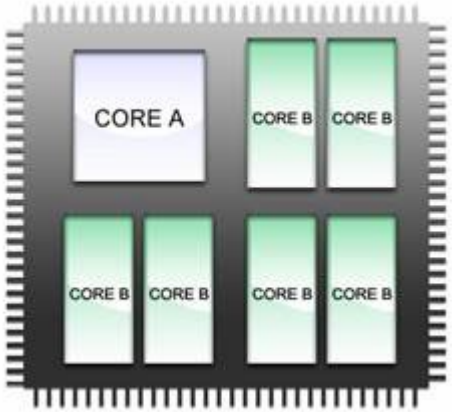
= open standard; ≠ open source

RISC-V®

Redefining
solutions

Flexibility & Portability

- Heterogeneous systems
- Hybrid solutions
  - Control flow in software
  - Data flow in hardware
- Security, safety & reliability
  - separation of concerns,
  - by executing each software component,
  - on multiple isolated cores in mixed criticality systems



Flexibility & Portability

- Technology agnostic platform development
  - Target multiple FPGA vendors

intel XILINX Microsemi a Microchip company NanoXplore

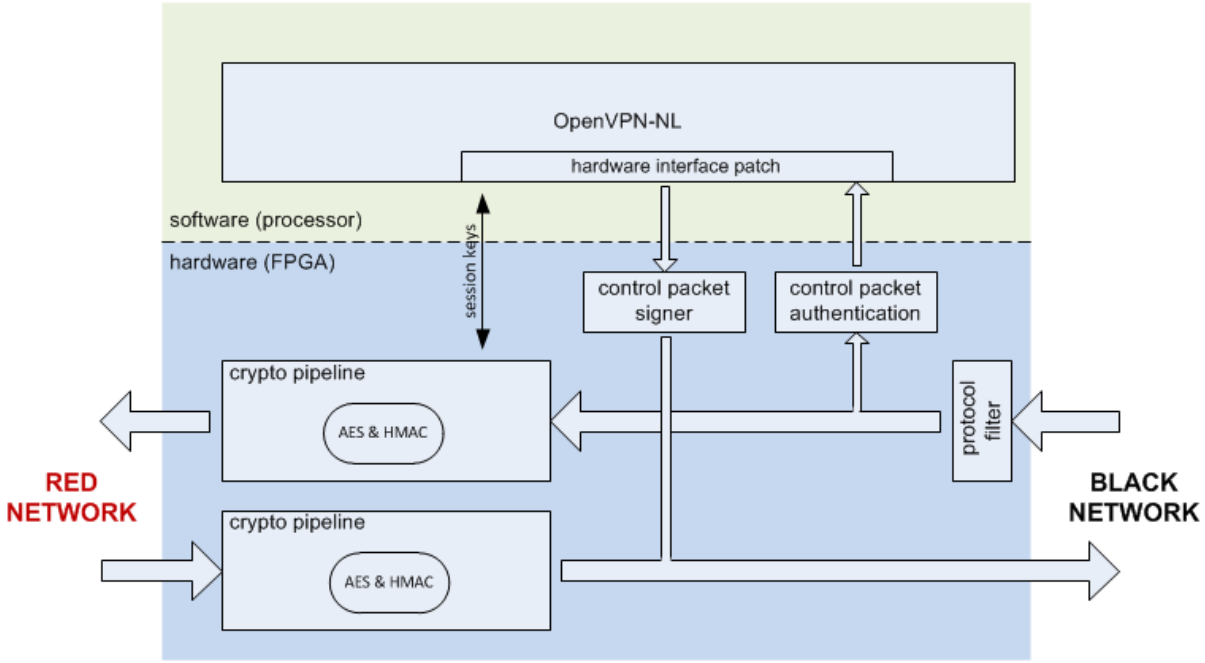
⇒ NIOS II soft processor (Intel)

⇒ MicroBlaze soft processor (Xilinx)

- Our RISC-V processor IP allows for portability without vendor lock-in
  - Re-using hardware sources ⇒ same processor
  - Re-using software tools ⇒ same compiler
  - Re-using software sources ⇒ same software

Secure line encryption

- Hardware VPN solution (NATO/EU Restricted)
  - Control flow in software / RISC-V®
  - Data encryption in hardware logic



Secure line encryption

- Hardware VPN solution (NATO/EU Restricted)
  - Control flow in software / RISC-V®
  - Data encryption in hardware logic

⇒ Full understanding of our custom implementation

⇒ Transparency for customer/evaluator

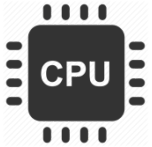
⇒ Lifecycle management (transparency & portability)

RISC-V® processor IP

Technolution
FOUNDING
Co-founder of the RISC-V® Foundation

- **FreNox** RISC-V IP
  - RISC-V processor family, 100% developed by Technolution
  - No dependencies on open-source implementations
  - Implemented in intel XILINX Microsemi a Microchip company NanoXplore
- **FreNox** RISC-V processor IP allows for portability without vendor lock-in
  - Re-using hardware sources ⇒ same processor
  - Re-using software tools ⇒ same compiler
  - Re-using software sources ⇒ same software

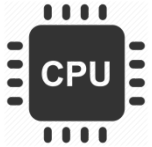
  } ease of qualification & certification
- **FreNox** RISC-V IP implemented in NLD/NATO/EU classsified security



FreNox-E

Embedded processor

- hardware
  - RV32I(M)
  - 32bits, mul/div
  - 5 stages - Harvard arch
  - cache or internal RAM
  - IO space
- software
  - Bare metal
  - FreeRTOS
  - ThreadX

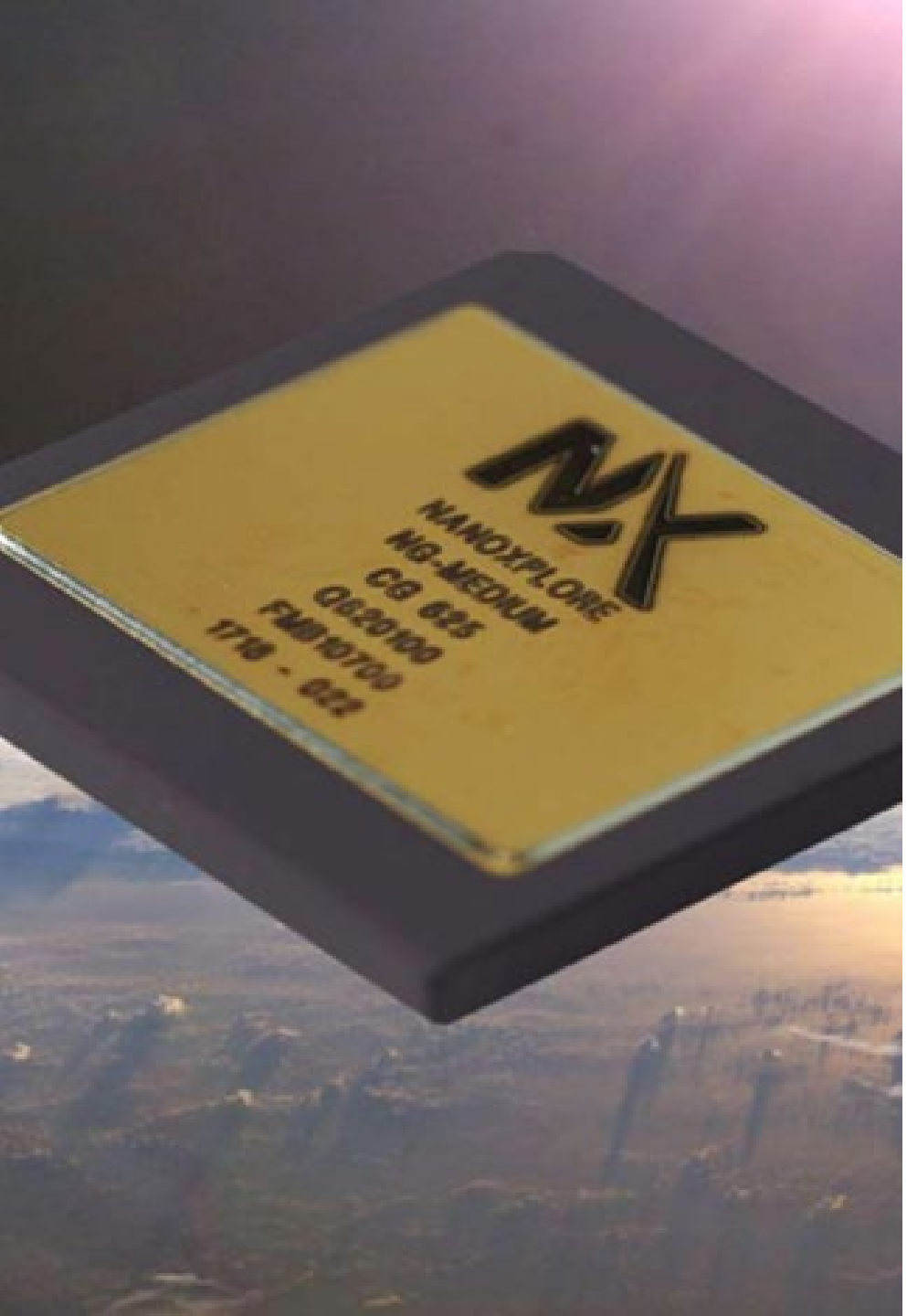


FreNox-S

Application processor

- hardware
  - RV32IMAS
  - 32bits, mul/div, atomic, supervisor
  - 5 stages - Harvard arch
  - iMMU, dMMU (1 - 128 entries)
  - 8 way associative cache (4 - 32k)
  - cache coherency (DMA)
  - IO space
- software
  - Linux
  - Buildroot

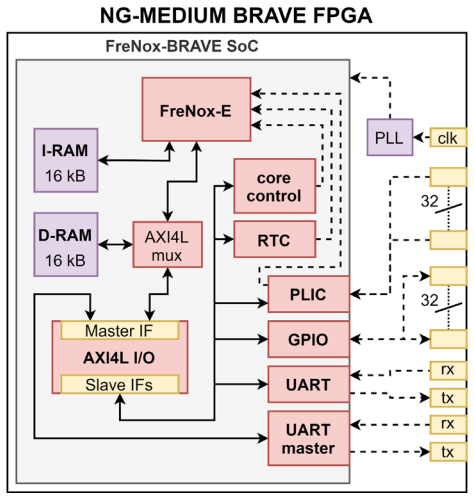
RISC-V®



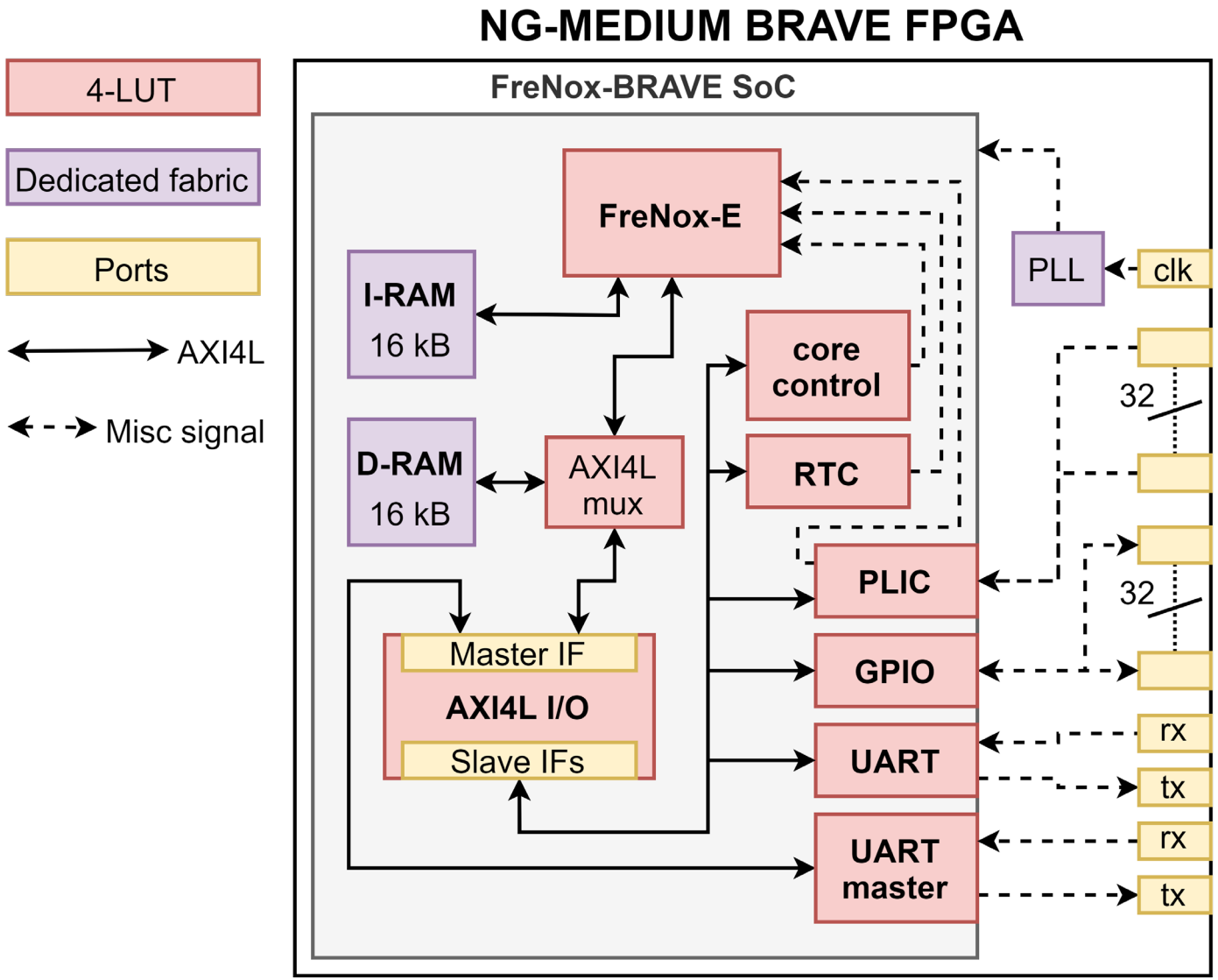
Radiation hardened FPGA

- Europe needs non-dependent access to critical space technologies
  - European radiation-hard FPGA

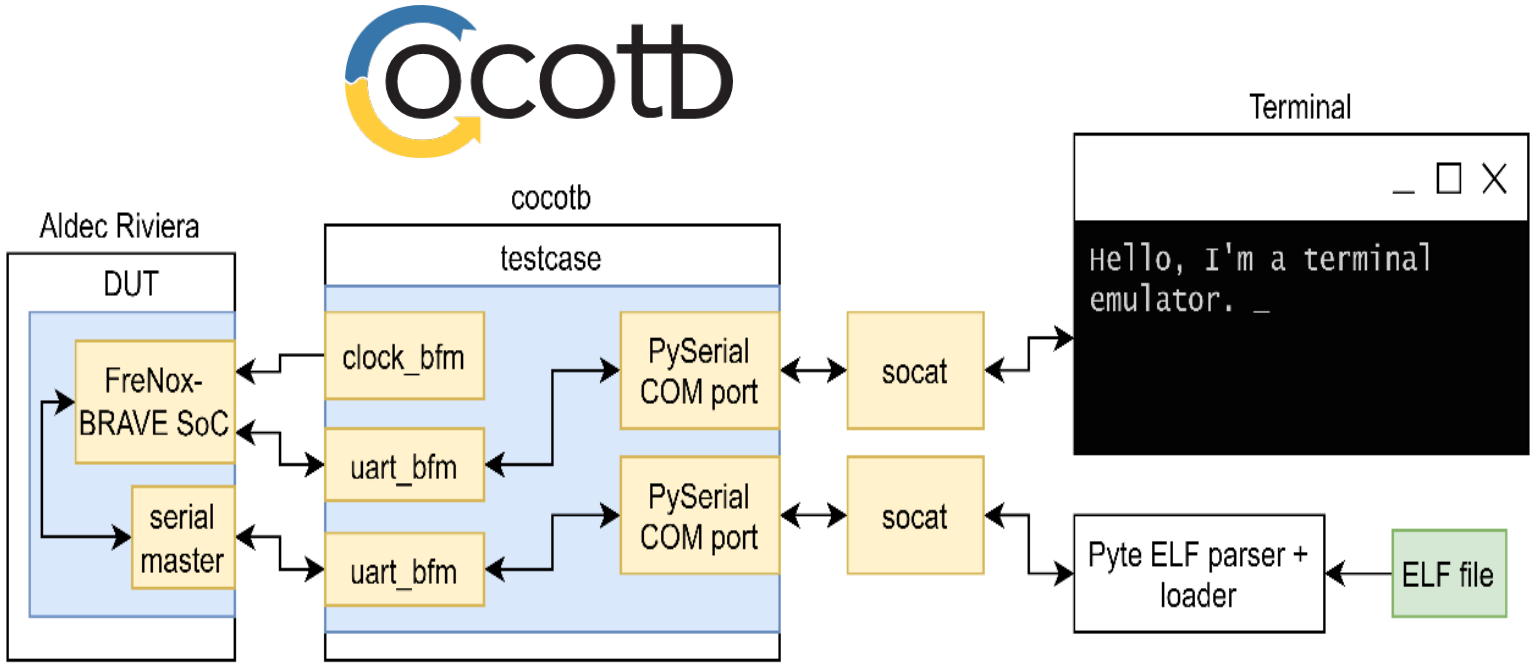
- **FreNox-E** SoC implemented and demonstrated in NG-Medium RH-FPGA



FreNox-E full System-on-Chip

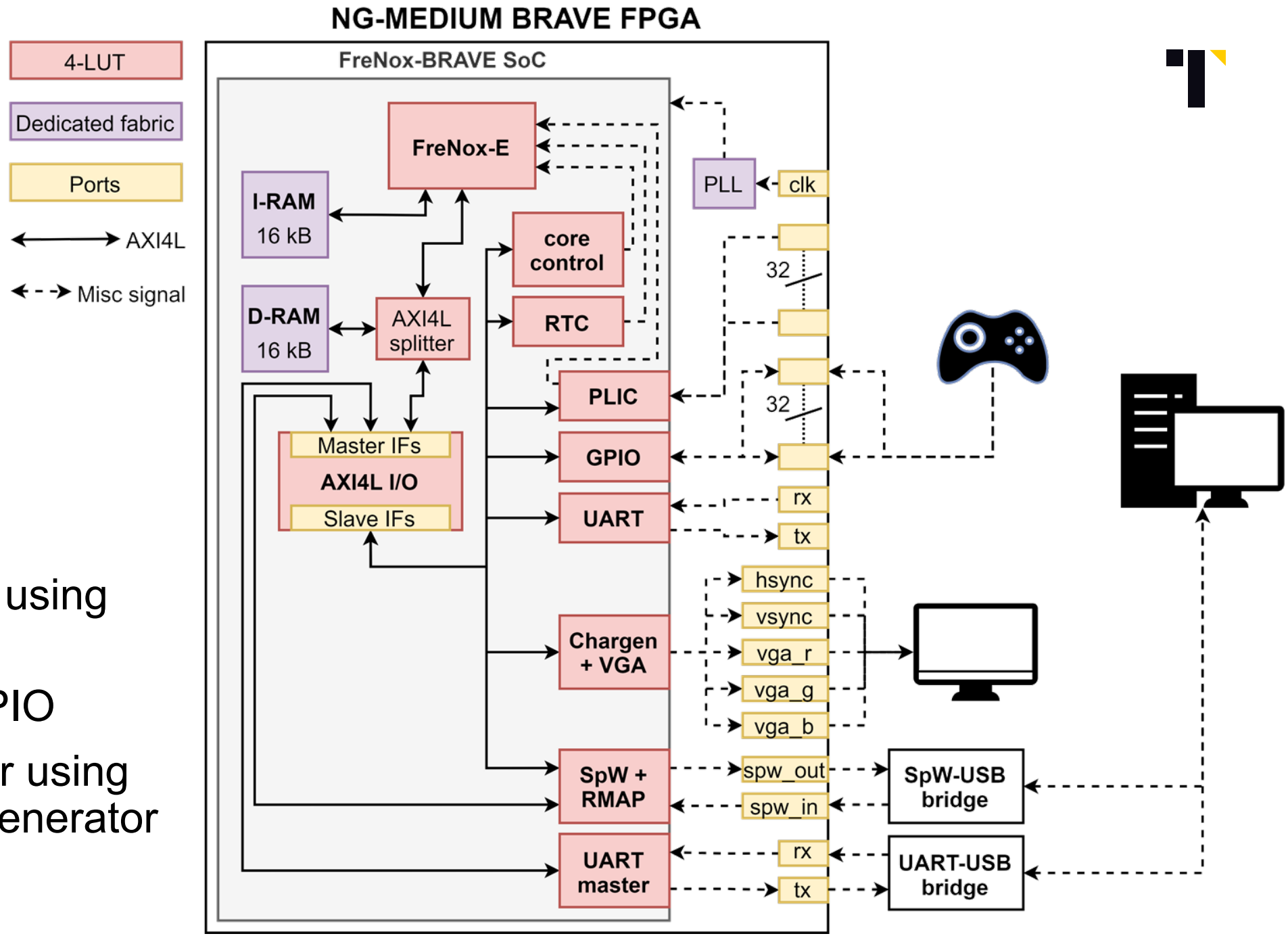


FreNox-E verification & validation



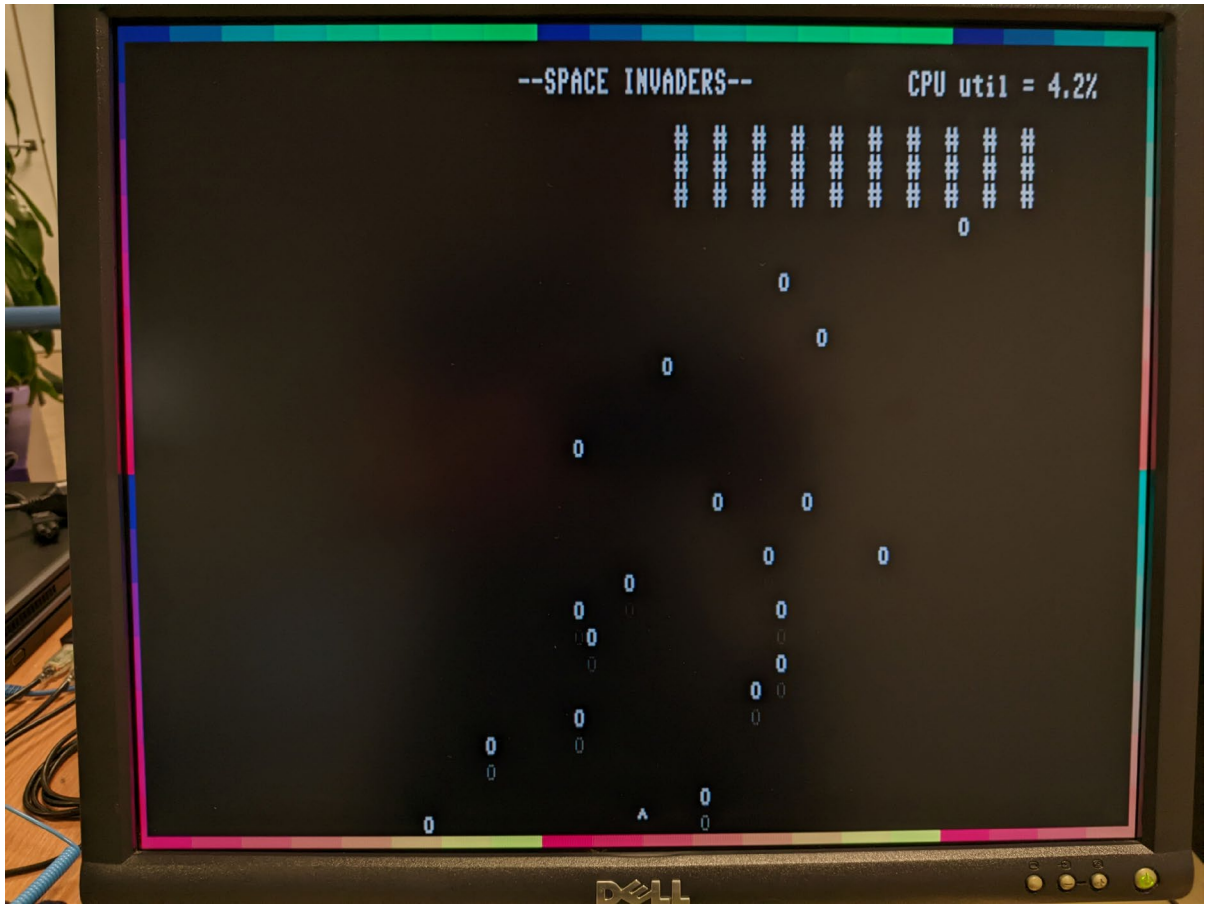
Verification by simulation

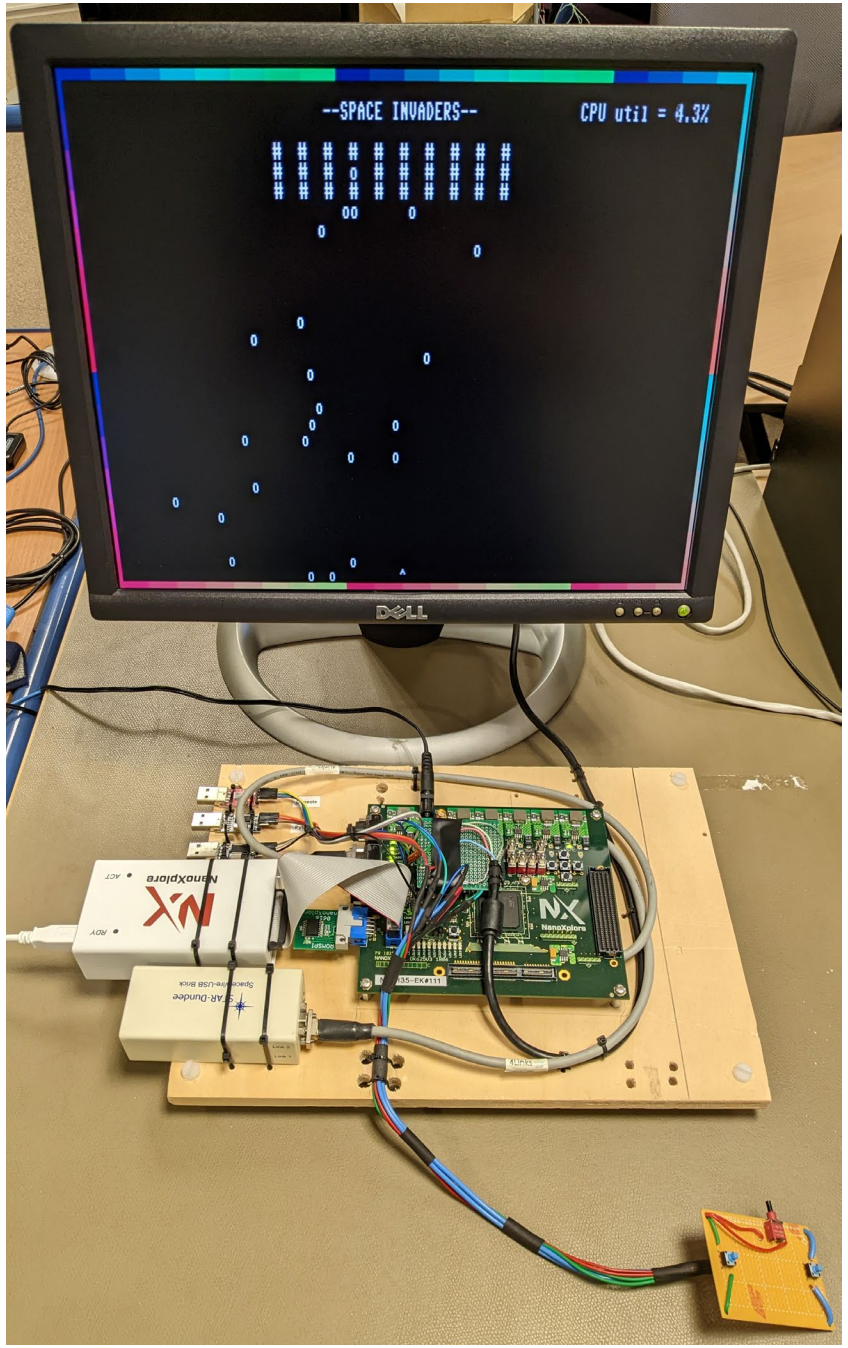
- Coroutine-based cosimulation testbench environment using Python
- Continuous Integration
  - Reliability, Repeatability, Predictability
  - Automated regression testing



- Upload software using SpW-RMAP
- Control using GPIO
- Output to monitor using VGA character generator

Demo: Space Invaders





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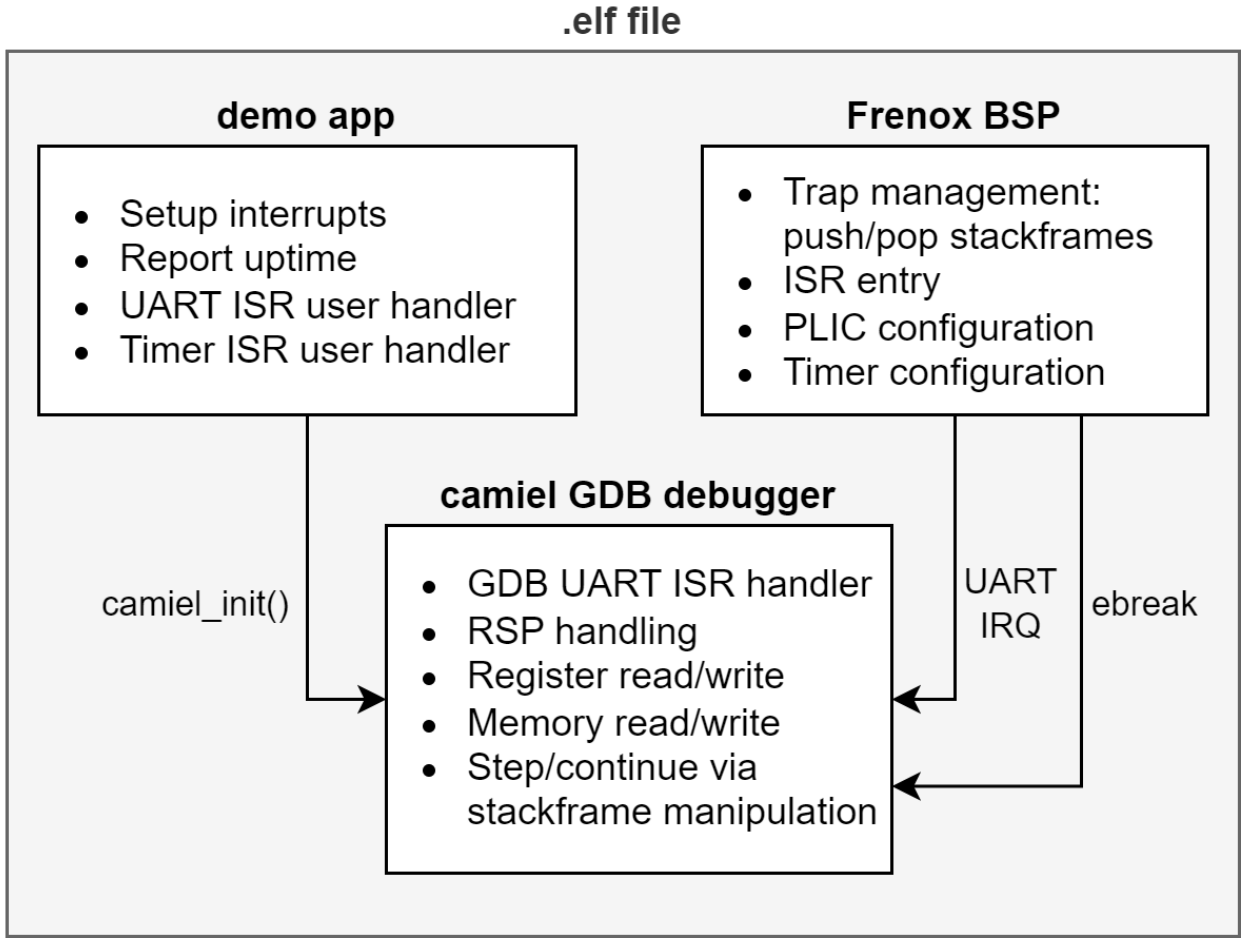
GDB remote interface

- Processor-agnostic GDB remote interface
- SW-implemented
- Entry via interrupts:
  - GDB UART RX IRQ
  - ebreak (for breakpoints)
- Control program execution via stackframe manipulation



CDPU: Control & Data Processing

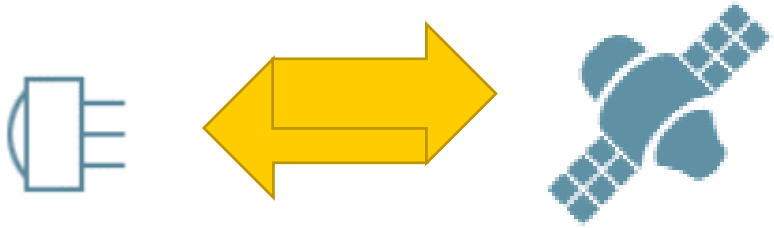
for SmallSat instruments

Netherlands Space Office

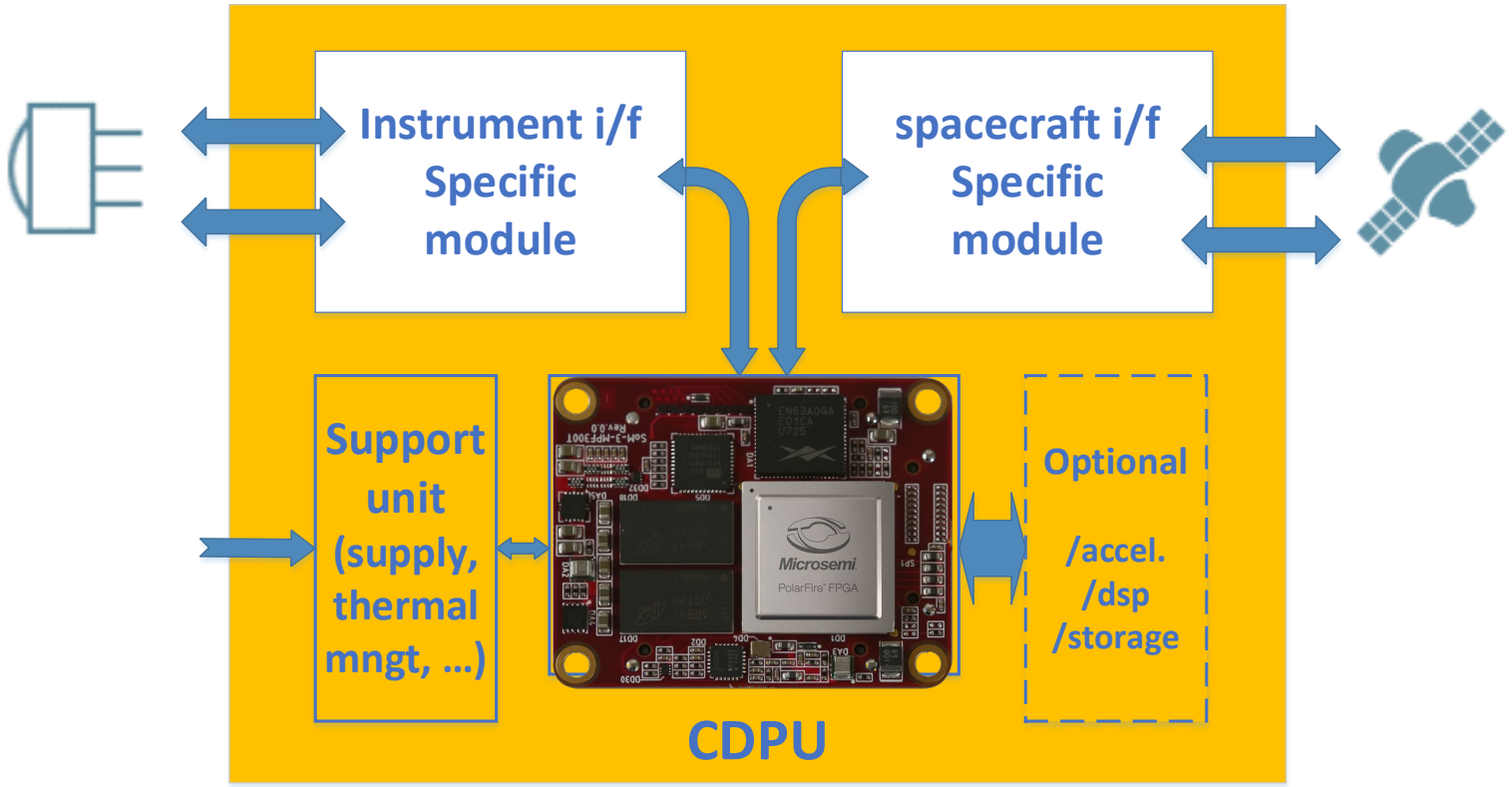
esa

Technolution

nlr



Flexible & reliable integration of sensor and platform



KDT-JU TRISTAN project

- European R&D project on RISC-V for high availability and space
  - High security/reliability for low-end processors

Continuation of fault-tolerance & security research:

→ Integration, validation and epxloitation of hardware-enforced fine-grained data labeling in RISC-V architecture

→ Integration and validation of Hardware Trojan detection techniques


Preventing Soft Errors and Hardware Trojans in RISC-V Cores

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Best Paper Award @DFT 2022

RISC-V® in summary …

- **FreNox** RISC-V IP
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- **FreNox** RISC-V processor IP allows for portability without vendor lock-in
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  } ease of qualification & certification

- **FreNox** RISC-V IP implemented in NLD/NATO/EU classsified security
- **FreNox-E** SoC demonstrated in NG-Medium RH-FPGA
- **FreNox-E** SoC designed in PolarFire FPGA for CDPU
- RISC-V fault-tolerance & security R&D activities in Horizon Europe and ESA-supported activities

Thanks for your attention!

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