RISC-V processor customization in the field

with Codasip Studio & Menta eFPGA

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Mike Eftimakis

VP Strategy & Ecosystem

Codasip

Company overview

- Founded in 2014
- 170+ employees
  - More than 80% in R&D
- Released the 1st commercial RISC-V core
  - Now over 2 billion cores shipped
- Unique combination of standard RISC-V with customization

European company

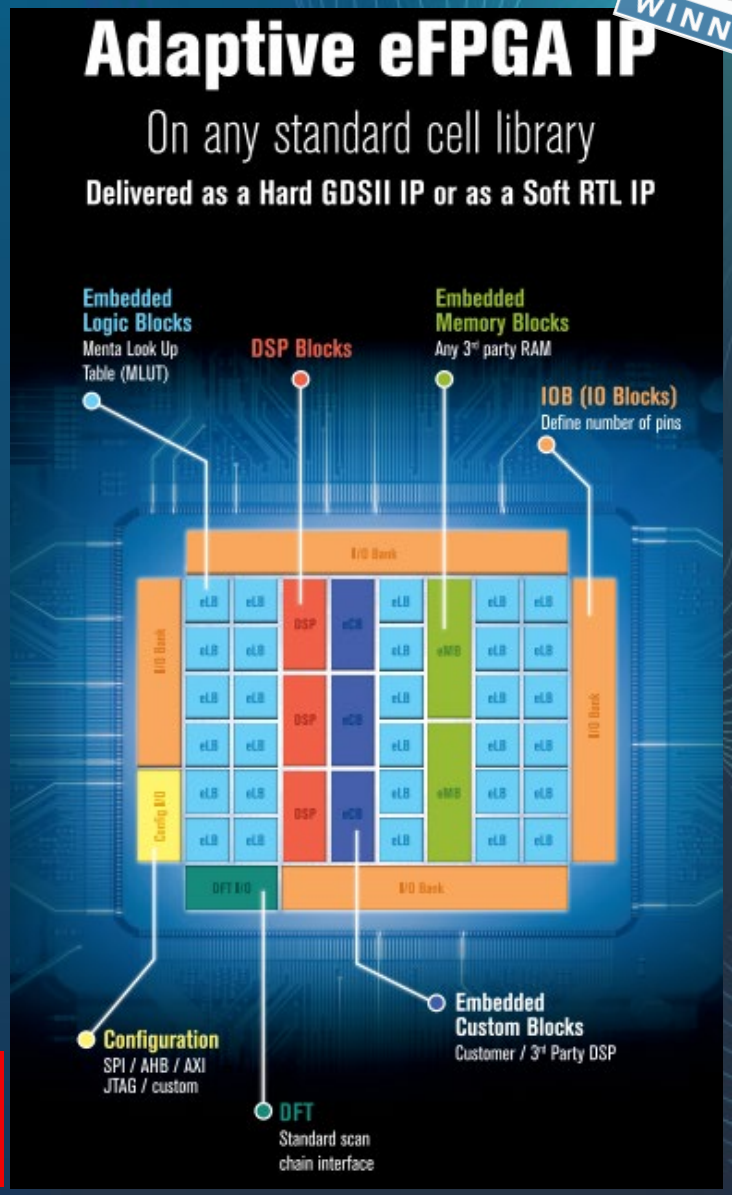
with sales offices around the world

MENTA eFPGA

European company and eFPGA leader

- Simple design flow integration (**soft or hard IP, standard cell**)
- **Design adaptive** IP (Fabric elements, DSP, Any Foundry, technology node, process options,…)
- **Best reliability & testability**
- **SEU immunity**
- **Rad Hard** (by design) on request
- Easy FPGA bitstream programming software
  - Origami Programmer – Best in class, home grown, integration into your own SDK
- 10+ partners – including CODASIP
- Proven technology, though innovative and state of the art (10+ years)
- **10+ tapeouts** on 8 different technology nodes

Easily augment flexibility and reduce cost by integrating Menta eFPGAs, supported by 13 years of experience and successes!



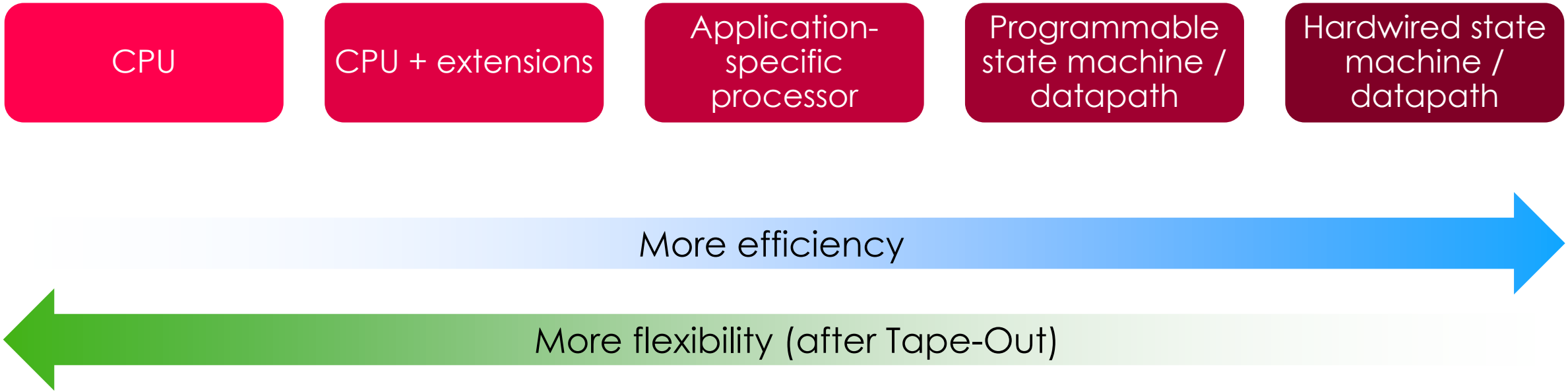
For more information about our products and services, visit www.menta-efpga.com

Concept

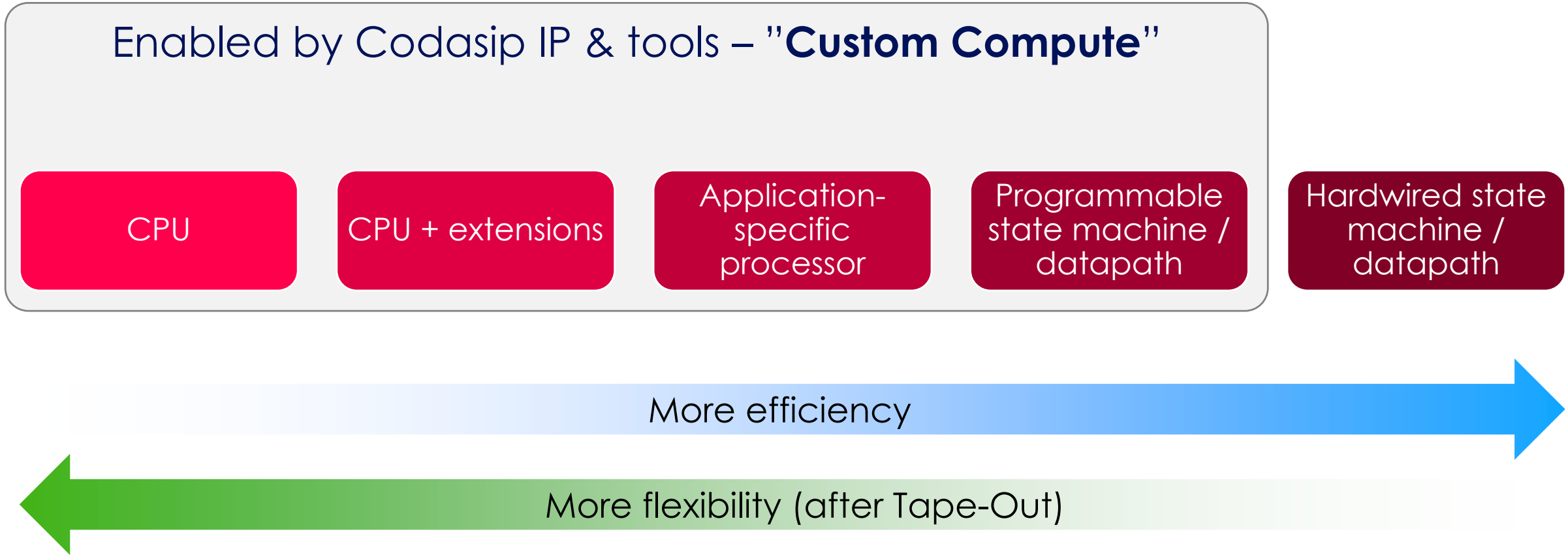
How to optimize and still be flexible?

- Technical optimization
  - HW tuned for maximum efficiency
  - Future proofing
- Financial optimization
  - Reusing the same silicon for several products
  - Investing for the long term
  - Reduce development costs
- Operational optimization
  - Reconfigure devices in the field
  - Adapt to unknown situations

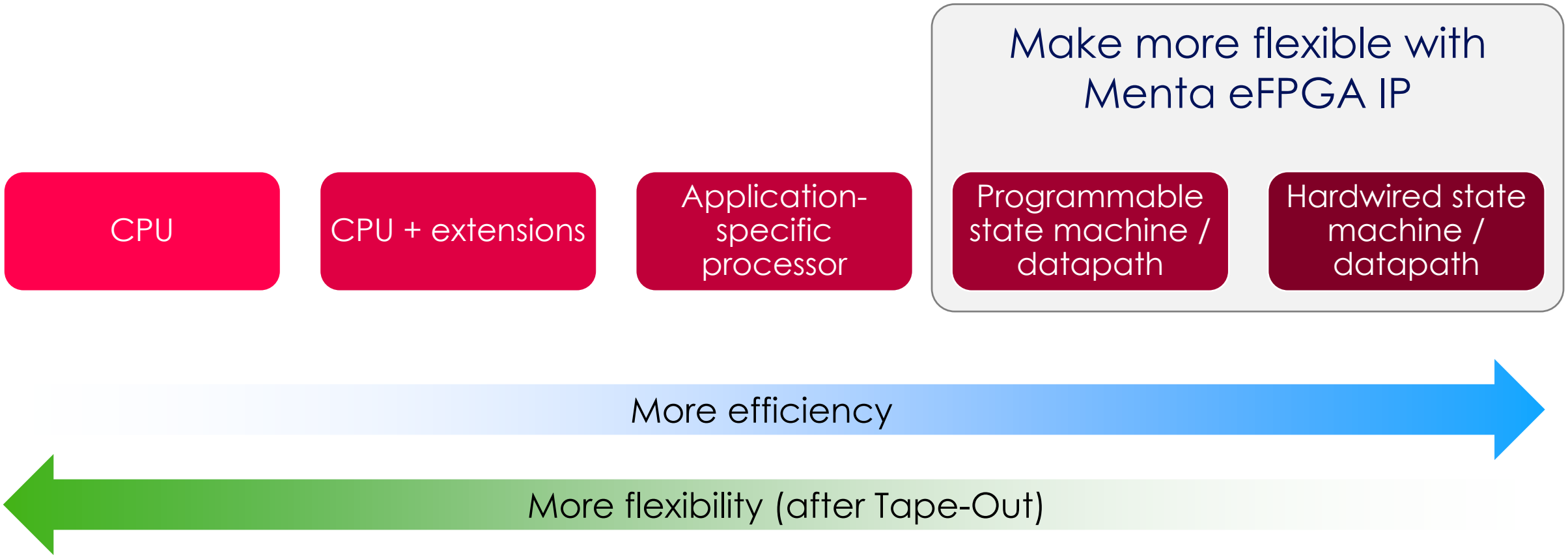
Flexibility vs efficiency



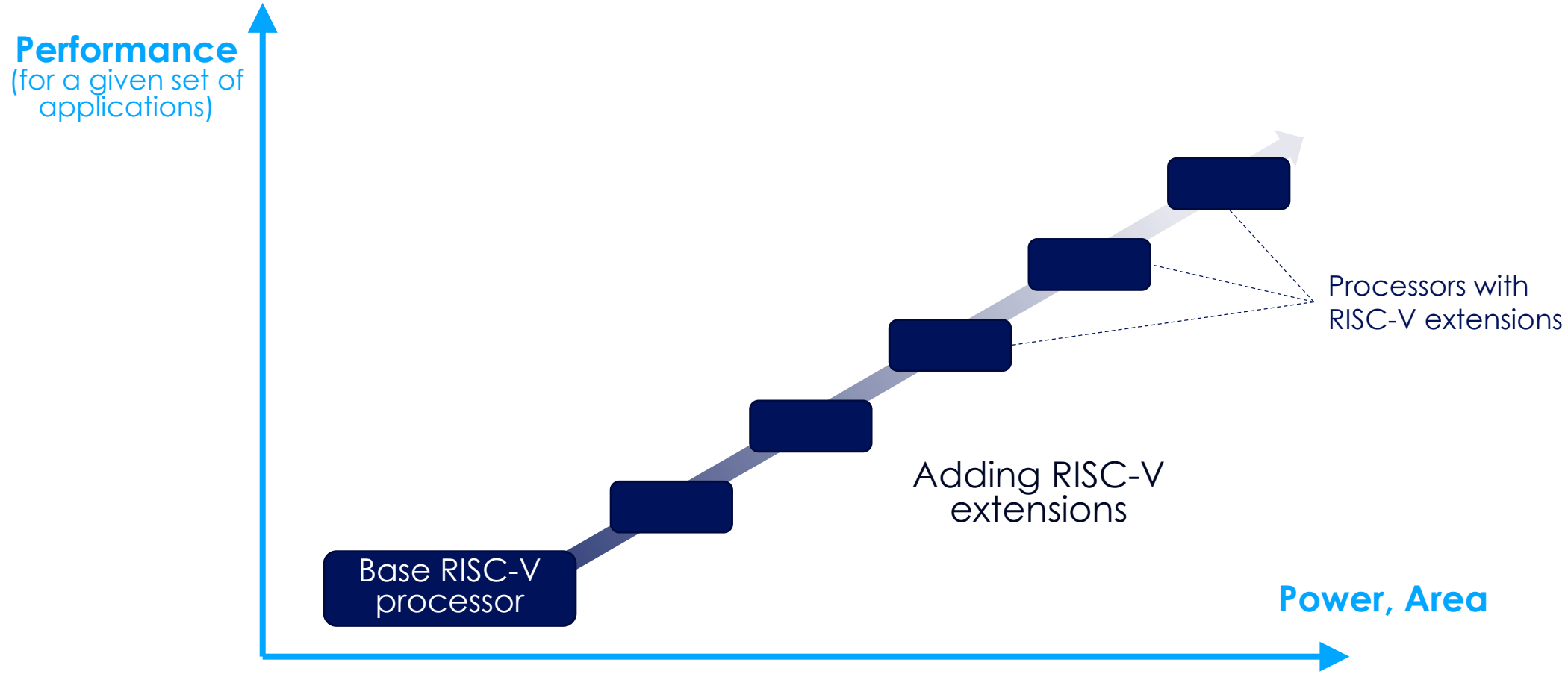
Flexibility vs efficiency



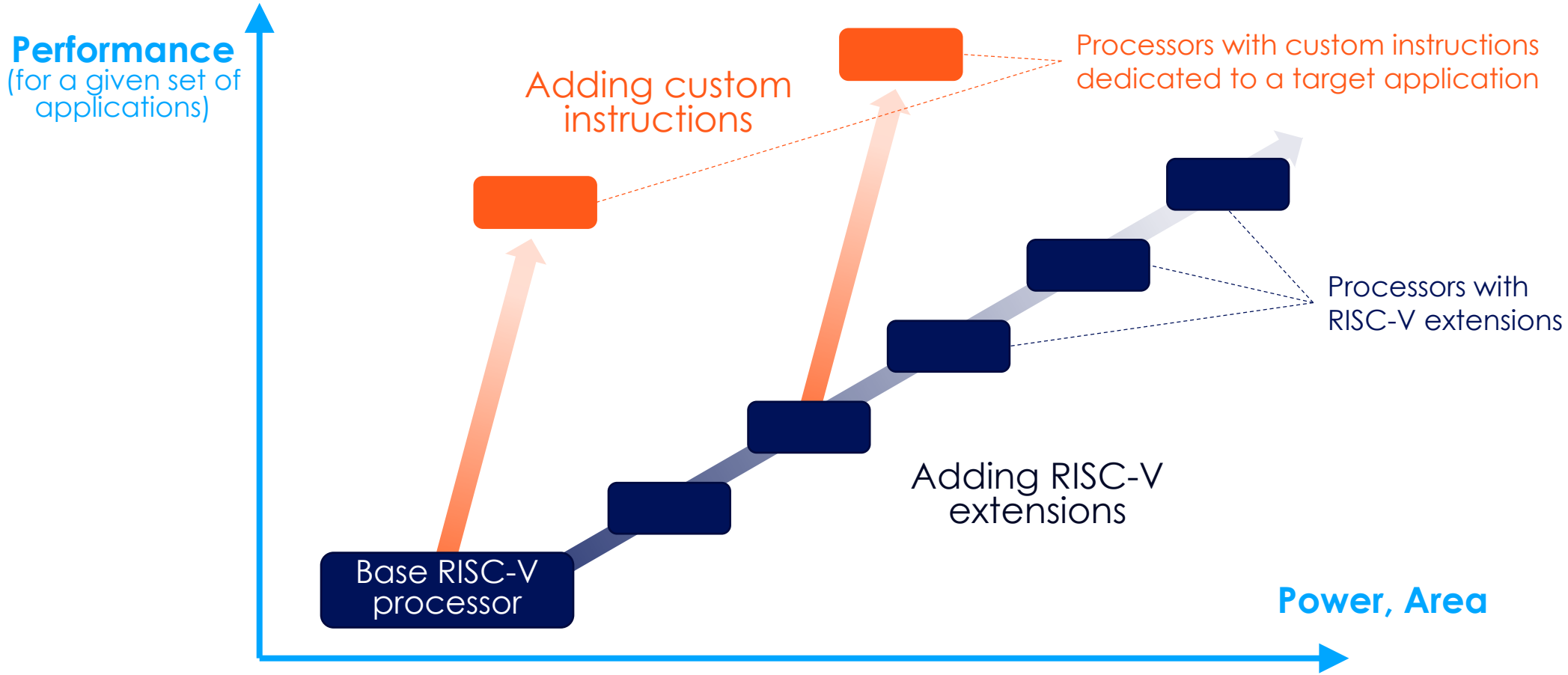
Flexibility vs efficiency



RISC-V extensions

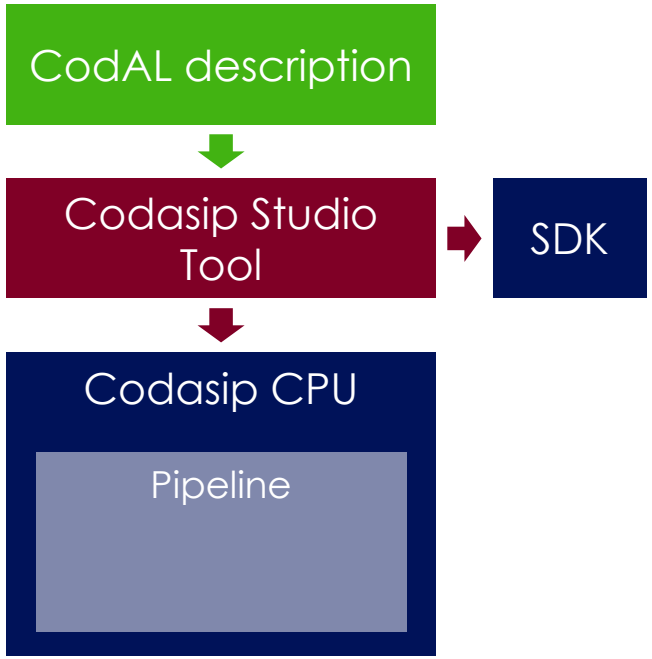


RISC-V custom instructions



Processor customization

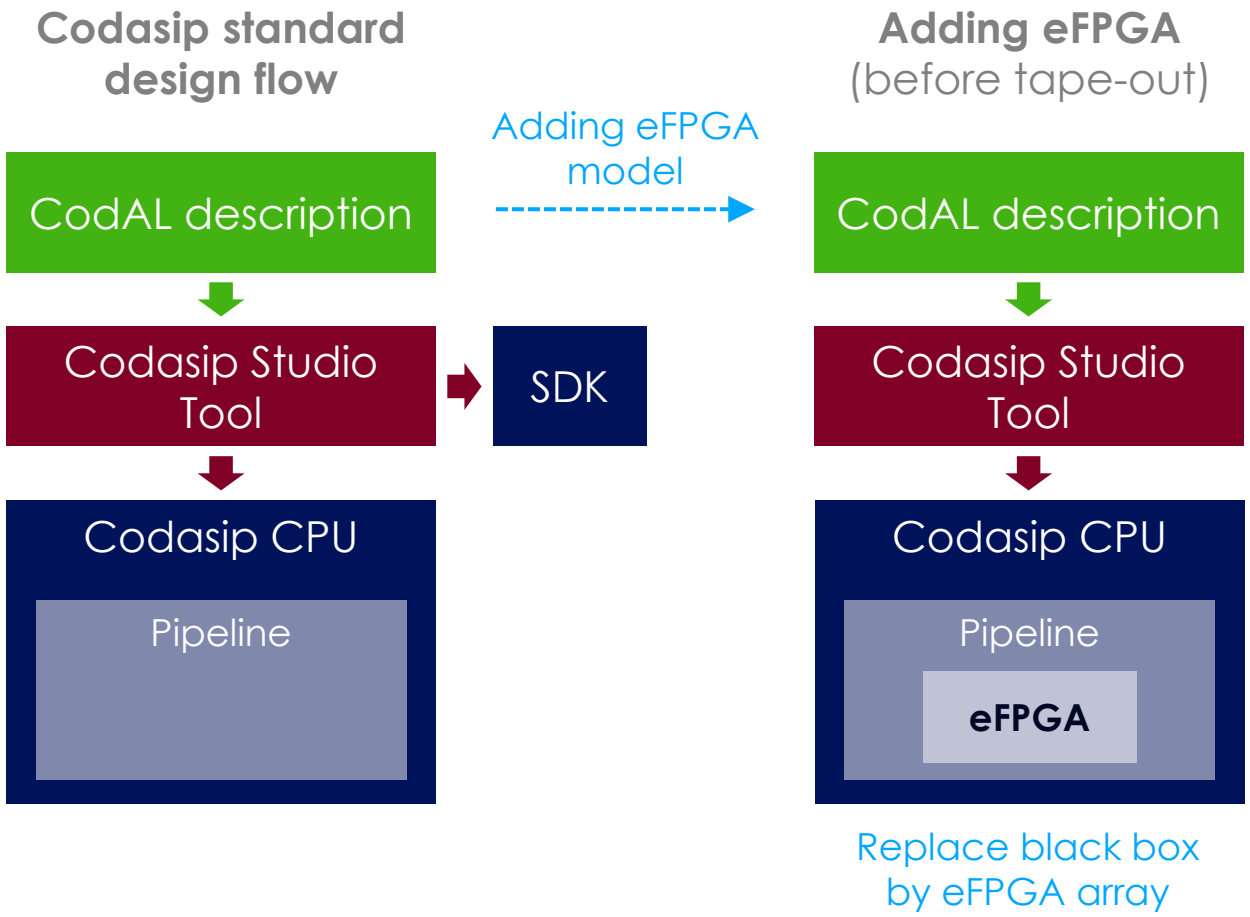
A fast and efficient development flow for custom RISC-V processors



- RISC-V CPU IP
  - In high-level language (CodAL)
  - Fully verified
- Users can modify the CPU
  - Profile different options
  - Add instructions
  - Architectural changes
- Tool generates everything
  - HW – RTL, testbench
  - SW – Compiler, debugger, models, libs

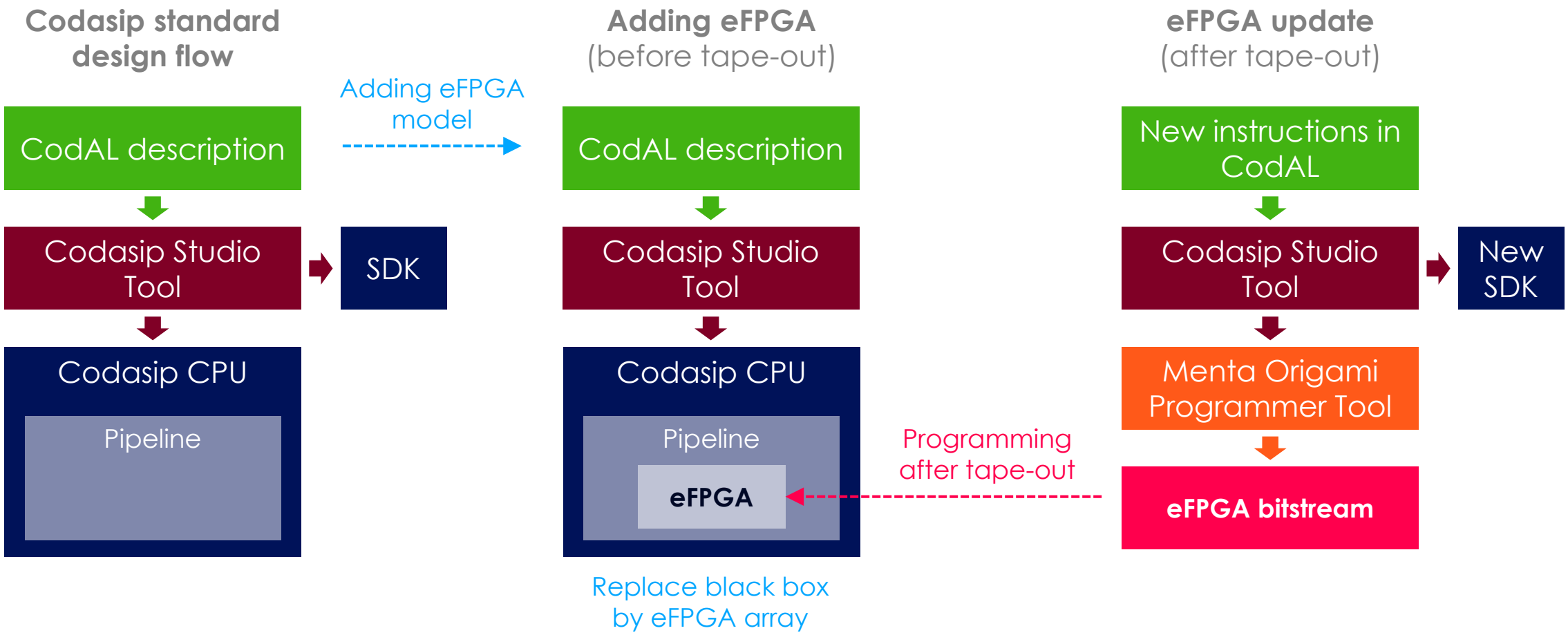
Enabling flexibility

Integrate Menta eFPGA inside the CPU pipeline



Enable re-configuration after Tape-Out

Generate and load new instructions, and enable SW development



A new capability

Combining Custom Compute and eFPGA

- Technical optimization
  - ✓ HW tuned for maximum efficiency
  - ✓ Future proofing
- Financial optimization
  - ✓ Reusing the same silicon for several products
  - ✓ Investing for the long term
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Thank you.

Now, it's your turn!

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