SMCS \textit{lite} and DS-Link Macrocell Development

Microelectronics Final Presentation Days, ESTEC, 6-7 March 2001
Presentation overview

- Background and Introduction
- Rationale for SMCSlite
- The IEEE-1355 Link and Protocols
- SMCSlite Description:
  - Features
  - Implementation
  - Applications
- SMCSlite Validation
- SMCSlite Test Board
- SMCSlite Commercialisation
- DS-Link Macrocell
- Summary and Conclusions
Background and Introduction

- Increasing complexity of sensors (CCD cameras, spectrometers etc.) lead to higher data rates between sensor front-end and data processing unit ⇒ more emphasis on noise, limited pin count, power consumption, error handling etc.

- Wide variety of interface types, data rates and requirements often lead to custom designed i/f solutions.

- Standardised communication introduced for inter-processor / inter-module domain in the form of IEEE-1355 high-speed (≥100 Mbit/s) serial links.

- A communication controller providing three IEEE-1355 links (~200 Mbit/s each) exists in the SMCS332, targeted at processor elements etc.

- A derivative of the SMCS332, the SMCS\textit{lite} was developed to cover typical needs of interface units, providing one link together with control units for autonomous / remote control operation.
The IEEE-1355 Link and Protocols

- Defines a full-duplex, bit serial, point-to-point link with a raw data rate of up to 200 Mbit/s. Two signals per direction with data - strobe encoding for clock recovery on the receiver side.

- Layered protocol implements flow-control, parity check, link reset and restart procedures. Link disconnection is detected by timeout (missing NULL tokens on link).

- The IEEE-1355 only defines a transport medium between two nodes. Routing requires additional headers but is possible in a network using routing devices.

- IEEE-1355 being used in current and future missions, such as Rosetta, MarsExpress, ISS, First-Planck etc. Astrium involved in key projects.
Rationale for SMCSlite

- Connecting a non-intelligent node to a processing element requires both communication controller and controller (FPGA, Controller etc.).
- An SMCS332 with three IEEE-1355 links may be overdimensioned for some applications, or additional circuitry is still required for GPIO, or interfacing to ADC, DAC etc.
- Need for a smaller (one link only) SMCS with more system support for non-intelligent nodes.
- Target requirements for the design of the SMCSlite were:
  - Small package (≤100 pins)
  - Low power consumption and radiation-tolerant manufacturing
  - Sufficient I/O control lines to control and operate I/O devices
  - Configurable memory interface for standard SRAM and FIFO
  - Additional system support (timer, UART)
  - Single clock supply
SMCS\textit{lite} Description: Features

- One IEEE-1355 link with 2.5 to 200 Mbit/s transmit rate. Link disconnect detection and parity check at token level, optional checksum generation/check at packet level.

- \textit{SMCS\textit{lite}} supports both transparent mode (pure IEEE-1355) and header generation for the transaction layer protocol of the SMCS332. Between 0 and 8 header bytes can be automatically generated by the \textit{SMCS\textit{lite}}.

- Single 5 MHz clock required.
**SMCS\textit{lite} Description: Features (cont.)**

- **block diagram of SMCS\textit{lite} shows functional blocks and interfaces**

- **Provision of several interface types:**
  - FIFO interface
  - ADC and DAC interface
  - RAM interface
  - UART interface
  - GPIO interface
  - JTAG
  - Timer / Event counter
  - Host interface
SMCSlite Description: Features (cont.)

- **FIFO Interface:**
  - Provides the control signals full, write, empty and read, depending on the direction of the data flow (receive/transmit)
  - Data received from the FIFO interface is sent over the IEEE-1355 link grouped in packets. The length of a packet (in bytes) can be specified either by setting an internal counter or by external signals.
  - Can be programmed to use 0 to 7 wait states

- **ADC/DAC Interface:**
  - 16-bit data bus to connect ADC and DAC
  - AD conversion started by either timer or by request from link
  - 8-bit programmable multiplexer (address generator) provided for analog signal multiplexing if required.
  - Control of the DAC also by link.
SMCS\textit{lite} Description: Features (cont.)

- **RAM Interface:**
  - 16-bit data and 16-bit address bus with four chip select lines.
  - 4 internal 8-bit wide address boundary registers for memory partitioning.
  - Configurable wait-states 0 to 7.

- **GPIO Interface:**
  - Up to 24 bidirectional signal lines with individually selectable in/out direction.
  - GPIO port lines shared with other functions, 8 are dedicated GPIO, 16 are shared with ADC address and host data bus.
  - Data is read/written from/to the GPIO via link.
SMCS\textit{lite} Description: Features (cont.)

- **UART Interface:**
  - Two independent UARTs; one is shared with GPIO port lines.
  - Optional hardware handshake (rts/cts).
  - UART transfer rate programmable via 12-bit register up to \(~780\) kbit/s.

- **Host Interface:**
  - Allows control by local host (controller, FPGA etc.) if required.
  - Multiplexed 8-bit address and data bus.

- **Timers:**
  - Two 32-bit on-chip timers; each with a 32-bit counter and 32-bit reload register.
  - Can be operated cascaded or independent.
  - Can set an external signal when timeout is reached.
SMCS\text{l}ite Description: Features (cont.)

- **Configuration:**
  - After reset the SMCS\text{l}ite can be configured via link or by an external controller connected to the host port.

- **JTAG:**
  - Standard IEEE-1149.1 interface with JTAG functions bypass, extest, sample/preload, all-tristate and IDcode.

- **Shared I/O:**
  - Some of the a.m. functions share I/O pins; some functions are mutually exclusive
SMCS\textit{lite} Implementation

- Design was done in VHDL and logic synthesis.
- A test bench was developed for test and verification purposes.
- Target library and process is Atmel W&M (ex Temic/MHS) MG1RT library (0.6 µ) and SCMOS2RT process.
- Total dose performance of the RT process is $\geq$50 krad, 30 MeV SEU (@5V), LET immune.
- Implementation in a 90kgate array.
- Package is 100 pin MQFP.
- Power consumption:
  - 80 mA at 150 Mbps
  - 60 mA idle
SMCSlite Programming

- Programming the SMCSlite over the link is done using a simple link protocol or over host interface.
- Link protocol is one command byte and (if necessary) one or more data bytes.
- All internal registers are 8-bit wide. Two link commands (read and write) suffice to address all functions and registers of the SMCSlite.
- SMCSlite provides registers and ports. A register contains one byte, whereas a port (e.g. a FIFO, UART etc) behaves like a FIFO (more data can be read/written from/to a port).
- Register / port addressing, ADC/DAC, Memory interface can be accessed by a simple read or write to their corresponding register address. Packet oriented access is also possible (for FIFO, Host, UART and memory).
SMCS\textit{lite} Programming (cont.)

- Memory connected to the SMCS\textit{lite} can be block accessed.
- Read / write SMCS\textit{lite} registers:
  
  \begin{itemize}
  \item Command: read register
  
  \begin{align*}
  &7 \quad 6 - 0 \\
  &1 \{ \text{register address} \} \quad \text{EOPx}
  \end{align*}

  \begin{itemize}
  \item control bit: read register
  \end{itemize}

  \begin{itemize}
  \item to
  \end{itemize}

  \begin{itemize}
  \item SMCS\textit{lite}
  \end{itemize}

  \begin{itemize}
  \item from
  \end{itemize}

  \begin{itemize}
  \item 7 \quad 6 - 0
  \end{itemize}

  \begin{itemize}
  \item \{ \text{register address} \} \quad \text{register value} \quad \text{EOPx}
  \end{itemize}

  \begin{itemize}
  \item Byte 0
  \end{itemize}

  \begin{itemize}
  \item Byte 1
  \end{itemize}

  \item Command: write register
  
  \begin{align*}
  &7 \quad 6 - 0 \\
  &0 \{ \text{register address} \} \quad \text{new register value} \quad \text{EOPx}
  \end{align*}

  \begin{itemize}
  \item control bit: write register
  \end{itemize}

  \begin{itemize}
  \item Byte 0
  \end{itemize}

  \begin{itemize}
  \item Byte 1
  \end{itemize}

- Read / write SMCS\textit{lite} ports:

  \begin{itemize}
  \item Command: write to port
  
  \begin{align*}
  &7 \quad 6 - 0 \\
  &0 \{ \text{port address} \} \quad \text{data byte 0} \quad \ldots \quad \text{data byte n} \quad \text{EOPx}
  \end{align*}

  \begin{itemize}
  \item control bit: write
  \end{itemize}
  \end{itemize}
SMCS\textit{lite} Applications

- **Main application areas:**
  - **Embedded Systems:**
    - Interface with special ASICs (compression chips), mass memory units, sensor frontends (ADC / DAC), standard I/O
  - **Communication device for processor systems:**
    - Single-link interface for microcontrollers and/or microprocessors
SMCS\textit{lite} Applications (cont.)

- **SMCS\textit{lite}** connected to ADC and DAC without local control:

```
+----------------+        +----------------+
|     UART1      |        |     DAC        |
|  Data [15:0]   |        |  WR          |
| SMCS\textit{lite} |      |  ADDR       |
|                |        |  DATA       |
| GPIO          |        |  DATA       |
| HOCI          |        |  CS         |
|               |        |  R/CREADY   |
|               |        |  READY      |
|                |        | SMCS\textit{lite} |
|                |        | Analog MUX  |
|                |        | SEL        |
|                |        |            |
|                |        |            |
+----------------+        +----------------+
```

IEEE-1355

- IOB10/DAC_WR
- IOB11-13/DAC_ADDR
- IOB8/ADC_CS
- IOB9/ADC_R/C
- IOB22/ADC_RDY
- IOB0-7/ADC_SEL

DAC
- WR
- ADDR
- DATA

ADC
- DATA
- CS
- R/C
- READY

Analog MUX
- SEL

In this configuration, SMCS\textit{lite} is connected to the ADC and DAC without local control. The diagram illustrates the data flow and connections between UART1, DAC, ADC, and Analog MUX.
SMCSlite Applications (cont.)

- **SMCSlite as communication front-end for a microcontroller:**

  ![Diagram of SMCSlite connections](image)

  - IEEE-1355 to SMCSlite
  - SMCSlite to DPRAM
  - DPRAM to uP, DSP, Sequencer
  - uP, DSP, Sequencer to SMCSlite
  - SMCSlite to IEEE-1355
SMCSlite Applications (cont.)

- SMCSlite connected to several external memory banks:

![Diagram showing SMCSlite connected to several external memory banks](image-url)
SMCS\textit{lite} Validation and Test

- **Objective**: Validation of design and functional test
- **Full design validation** performed on VHDL test bench
- **SMCS\textit{lite} hardware device tests** performed in two sessions:
  - First session under DIPSAP-II project (CEC)
  - Full test coverage achieved under ESA funded project “SMCS\textit{lite} Development”:

<table>
<thead>
<tr>
<th></th>
<th>Test Session 1</th>
<th>Test Session 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO I/F</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>RAM I/F</td>
<td>Partly</td>
<td>Yes</td>
</tr>
<tr>
<td>HOST I/F</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Timer</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>SMCS\textit{lite} Protocol</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>JTAG I/F</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>UART I/F</td>
<td>Partly</td>
<td>Yes</td>
</tr>
<tr>
<td>Header Generation</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Checksum</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>DAC</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Ext Interrupt</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>GPIO</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Link</td>
<td>Partly</td>
<td>Yes</td>
</tr>
</tbody>
</table>
SMCSlite Test Board Block Diagram

- SMCSlite 1
- SMCSlite 2
- DP-RAM 8k x 16
- FIFO 8k x 16
- FIFO 8k x 16
- SMCSlite Test Board
- 1355/LVDS
- PC
- SUN Workstation
- Mosaic LINK
- Mosaic SUN 1355
- JTAG/RS232
- PC JTAG/RS232
- SUN1355
- Mosaic
- Mosaic LINK
- 1355/LVDS
SMCS lite Test Board
SMCSlite DS-Link Macrocell

- **Objective:** provide ESA with a DS-Link macrocell compliant with the IEEE 1355 standard.

- **Activities:**
  - extract the present DS-Link macrocell (as used in the SMCS332 and SMCSlite) developed by Astrium as a stand-alone object,
  - provide an interface block between a serial link according to IEEE 1355-1995 DS-SE and an 8-bit wide parallel port.
- corresponds to the SMCS332 front-end operation in transparent mode.
SMCS\textit{lite} DS-Link Macrocell (cont.)

- The following events (only) will be signalled:
  - EOP\_1 Receipt
  - EOP\_2 Receipt
  - Parity Error
  - Disconnect Error
  - Null Received
  - FCT Received
  - Data Received

- Macrocell delivered to ESA along with a test bench and license for its use by ESA staff in simulation activities at its ESTEC premises
SMCS\textit{lite} Status and Commercialisation

- Design performed in VHDL and logic synthesis in 98Q1/Q2. A test bench was developed for test and verification purposes.
- Target library and process is Atmel W&M (ex Temic/MHS) MG1RT library and SCMOS2RT process (the same as used for the SMCS332).
- First samples manufactured in August 1998 and tested at MHS. Samples delivered to Astrium in 1998, week 36
- Evaluation completed.
- User Manual available at ESTEC SpaceWire page: \url{http://www.estec.esa.nl/tech/spacewire/}

- Availability as standard product from Atmel W&M expected in 2001; negotiations are complete.
- Atmel part number: T7906E
Summary and Conclusion

- The SMCSlite provides a means of interfacing a non-intelligent front-end or other device to a single IEEE-1355 link with up to 200 Mbit/s.
- Includes circuitry for command execution and protocol generation as well as additional on-chip features such as timers, FIFO control, ADC/DAC interfaces etc. to simplify the interface with non-intelligent subsystems without a local controller.
- Implementation in a radiation-tolerant ASIC technology (~90 kgates) of Atmel W&M, resulting in a compact 100-pin package.
- Test board implemented for hardware tests.
- Macrocell extracted as re-usable object.
- Commercialization as Atmel standard product.