ESA 13345 : Building Blocks for System on a chip contract
ESA 13345/#2 : Design of a System On a Chip Initial Analysis

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Summary

- Contract History
- Objective of the study
- Description of the SCoC
- Continuation of the study

Contract history

- COO2 is phase 2 of ESA 13345 contract called “Building Blocks for System on a Chip”.
- ESA 13345 contract is managed by Sandi Habinc at ESTEC. It includes :
  - #1 : development and Industrialization of an ERC32 VMEbus Interface Device
  - #2 : Initial Analysis of the Development of a System-On-a-Chip device
  - #3 : Development of a System-On-a-Chip device
- COO2 has an amount of about 20 Keuro and is the first work package of the standard ESA ASIC design flow : “Initial Analysis”.
- COO2 was notified early to study System On a Chip content.

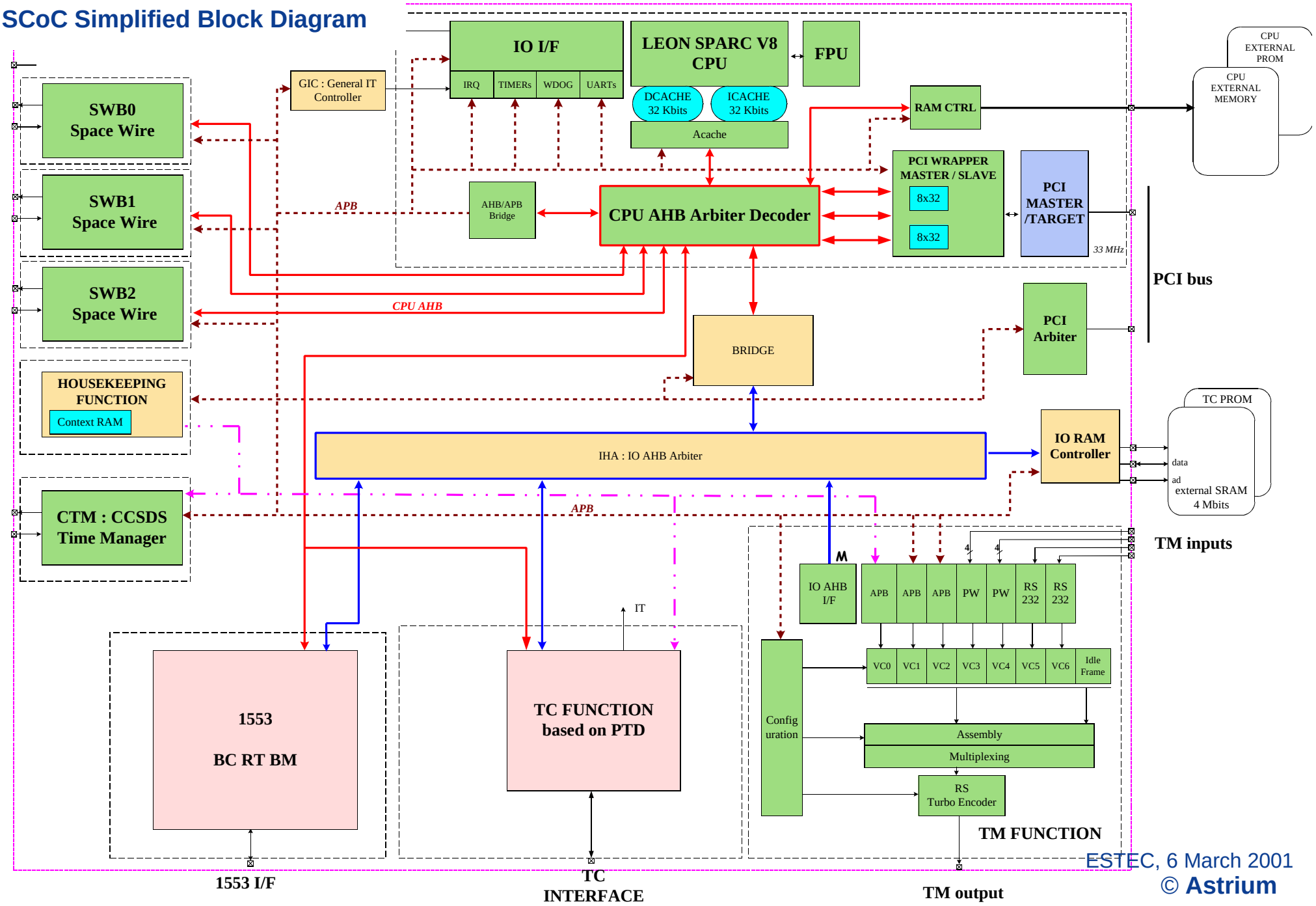
Objective of the study

- **Design a large ASIC called « System On a Chip » intended for space flight**
- **Possibly manufacture it**
- **Use VHDL blocks coming either :**
  - **From commercial vendors** ➢**Easy access for other users**
  - **From ESA** ➢**Stay property of ESA**
  - **From the background of the company** ➢**Stay property of the company**
  - **Developed in this activity** ➢**Become property of ESA with rights of use for the designer**

Description of the chosen System on a Chip

- The Agreed System on a Chip is called SCoC for Spacecraft Controller on a Chip
- It includes the main digital functions able to perform the Data Handling of a Spacecraft :
  - The processor based on LEON with its FPU
  - A SOC bus based on AMBA bus (trademark of ARM)
  - A parallel bus at board level : PCI (VME was abandonned)
  - A fast serial link : SpaceWire Link
  - An Elapsed Management Time function to monitor time
  - A serial bus for control of remote equipments : 1553 (could be CAN)
  - A Telecommand function based on PTD design
  - A Telemetry function including 8 VCA channel, a VCM, a Viterbi/Reed Solomon function and a Turbo Encoder

SCoC Simplified Block Diagram



Continuation of the study

- A board with a large XILINX is under development to breadboard parts of SCoC (baseline Virtex 2000 E, possibly Virtex II 6000).
- SCoC is gradually integrated at VHDL level
- SCoC is simulated in VHDL with VHDL emulators for the environment
- Breadboard on the Xilinx board for debug will start in May

- A3M study (Advanced Avionics Architecture and Modules) will use 4 of these boards for hardware test of their multiprocessor.