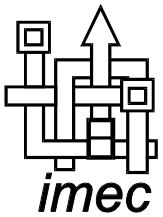
ESA-ESTEC GSTP4 - Analog Silicon Compiler for Mixed Signal ASICs

PDFE: A *P*article *D*etector *F*ront-*E*nd ASIC



PDFE: collaborators

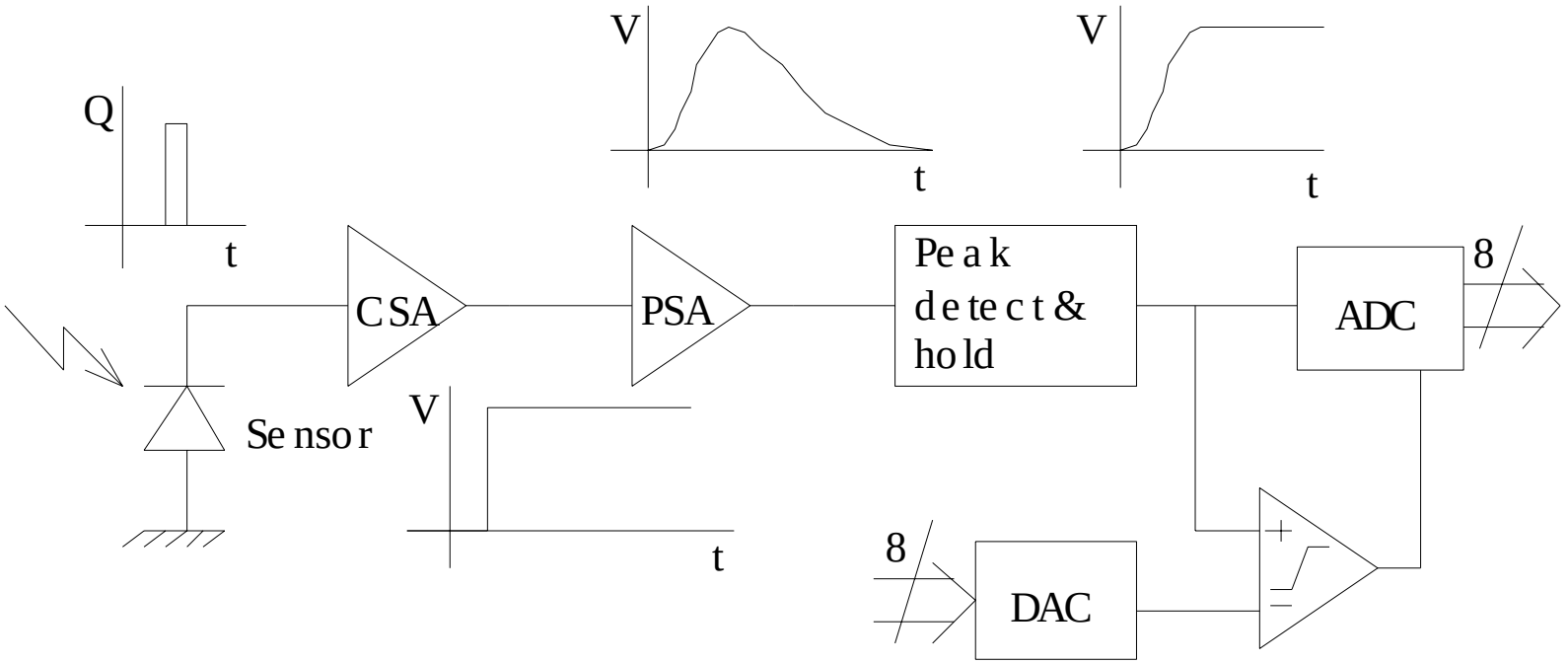
- PDFE is the result of a collaboration between
  - ESA-Estec
    - S. Habinc, B. Johlander, T. Sanderson
  - KULeuven, ESAT-MICAS
    - G. Gielen, J. Vandenbussche, G. Van der Plas
  - IMEC, Invomec
    - C. Das, K. Marent, S. Redant, J. Wouters
- PDFE is designed by IMEC, Invomec

Presentation overview

- Basic functionality
- Concept
- PDFE characteristics:
  - functionalities
  - block diagram
  - specs
  - programmability
- Some analog cells
- Digital part
- Simulations
- Radiation hardness
- Evaluation PCB's & some measurement results
- Status & Conclusions

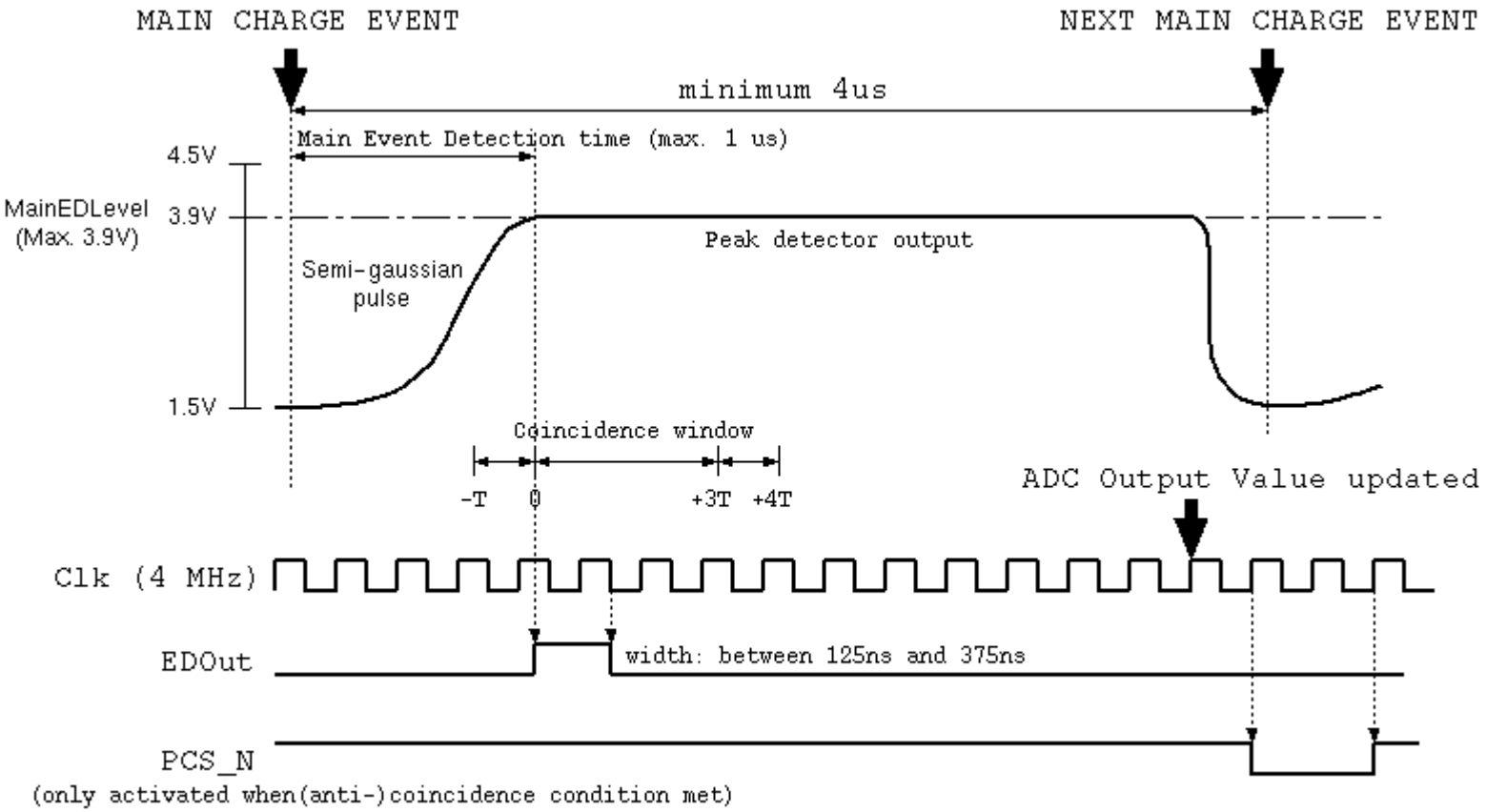
Basic functionality

- CSA
- PSA
- Peak detection
- DAC and discriminator
- ADC



Basic functionality: 1 conversion cycle

- One full cycle takes 4µs



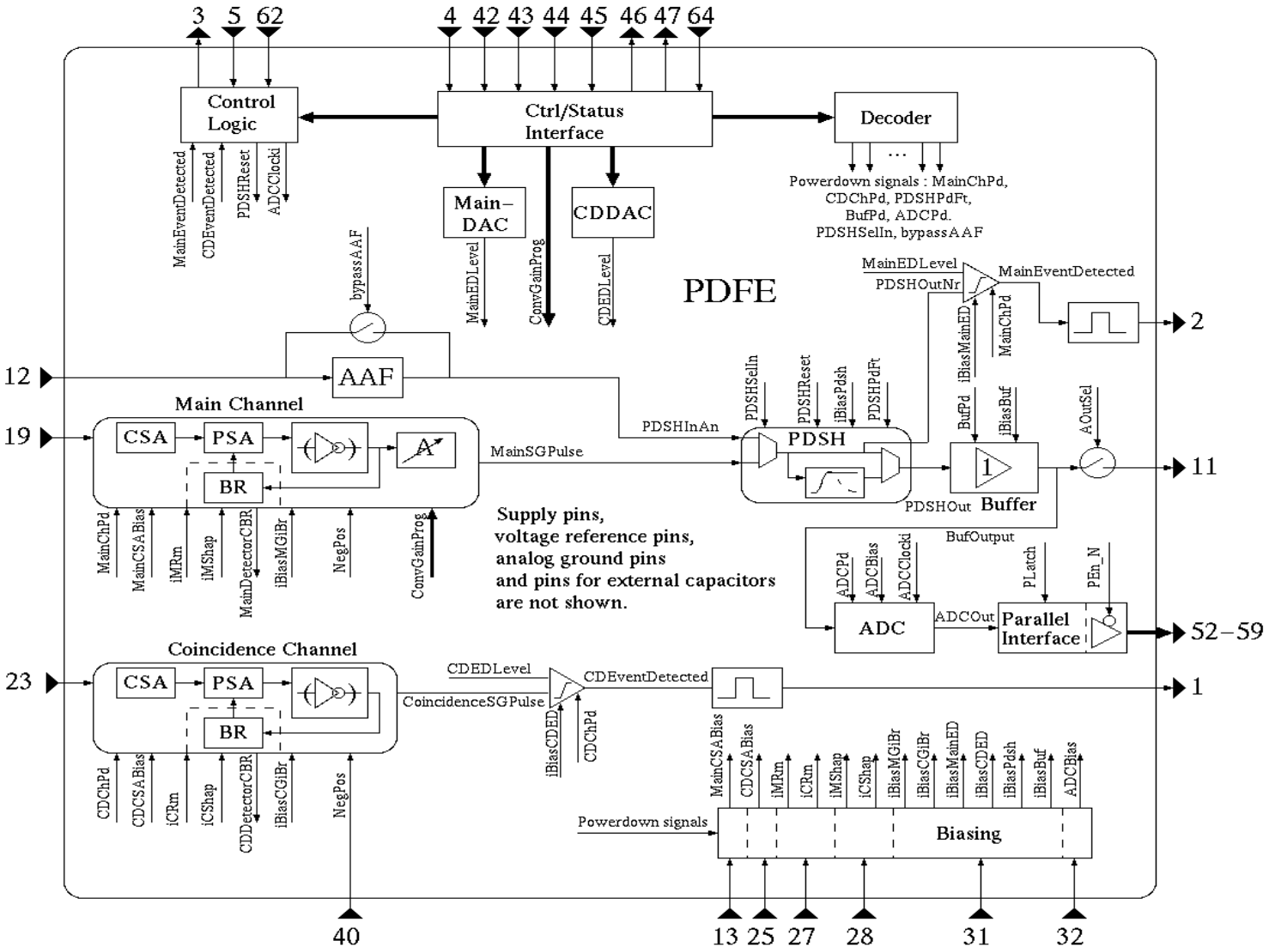
Concept

- Miniaturized Microcontroller based Read-out Electronics for Space Application (Energetic Particle Instrumentation)
- PDFE together with a 8052-based Microcontroller
- Architectural design drivers:
  - Low noise, low power
  - Low mass $\Longleftrightarrow$ Low chip count
  - Single supply voltage $\Longrightarrow$ simple power supply
  - Integrated ADC
  - Integrated standard space craft interface
  - Re-usability and scalability
    - because high NRE cost & long development time
  - Tolerance against single event effects and total ionizing dose
  - Mixed analog and digital signals
  - Testability and reliability (monolithic)

Main PDFE functionalities

- Main channel: charge amp, pulse shaping, baseline restorer, peak detector S/H
- (Anti-)coincidence channel
- Internal or external (anti-)coincidence gating
- Build-in 8-bit discriminators
- Gain adjustment (+/-5%)
- Linear 8-bit ADC, two-step flash
- Completely event driven
- Cascadable 32 bits serial control/status interface (scalability)
- 8-bit parallel output interface
- All internal registers SEU protected
- Low speed low amplitude digital I/O (to limit noise)
- Non-active blocks powered down

PDFE block diagram



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Main specifications

- Detector capa: 100 pF
- Detector leakage: 1 nA
- Full Scale input: 0.1 pC
- Conversion gain: 30 mV/fC
- Noise (ENC): 800 e^- rms (@ 100 pF)
- Peaking time: 1 µs
- Counting rate: 250 Ks/s @ 2.5 fC
25 Ks/s @ 0.1 pC
- Baseline drift: 15 mV
- Nonlinearity: 1 LSB
- Number of channels: 2
- ADC resolution: 8 bit
- ADC INL and DNL: ½ LSB
- Power supply: 5 V
- Power consumption: One channel: 15 mW
ADC: 30 mW
Total: 70 mW
- Ambient temperature: -40 to 65 °C
- Technology: 0.7-µm CMOS, mixed-signal, Alcatel Microelectronics
- Package: 64-pins quad flat pack
56 pins used

Programmability

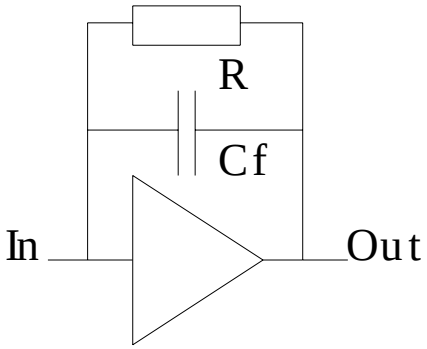
- Using the serial control/status interface
  - Coincidence channel enable/disable
  - Coincidence or anti-coincidence gating
  - Internal or external coincidence input
  - Discriminator levels (two 8-bit DACs)
  - Conversion gain adjustment (+/-5%)
  - ADC stand-alone
  - Power down
- Using digital pins (VSS - VDD strapped)
  - Charge sign
  - Analog or digital (ADC) output
  - Parallel output interface (ADC):
    internal or external control of the update
    (non-latching or latching mode; PROM or µP bus)

PDFE:

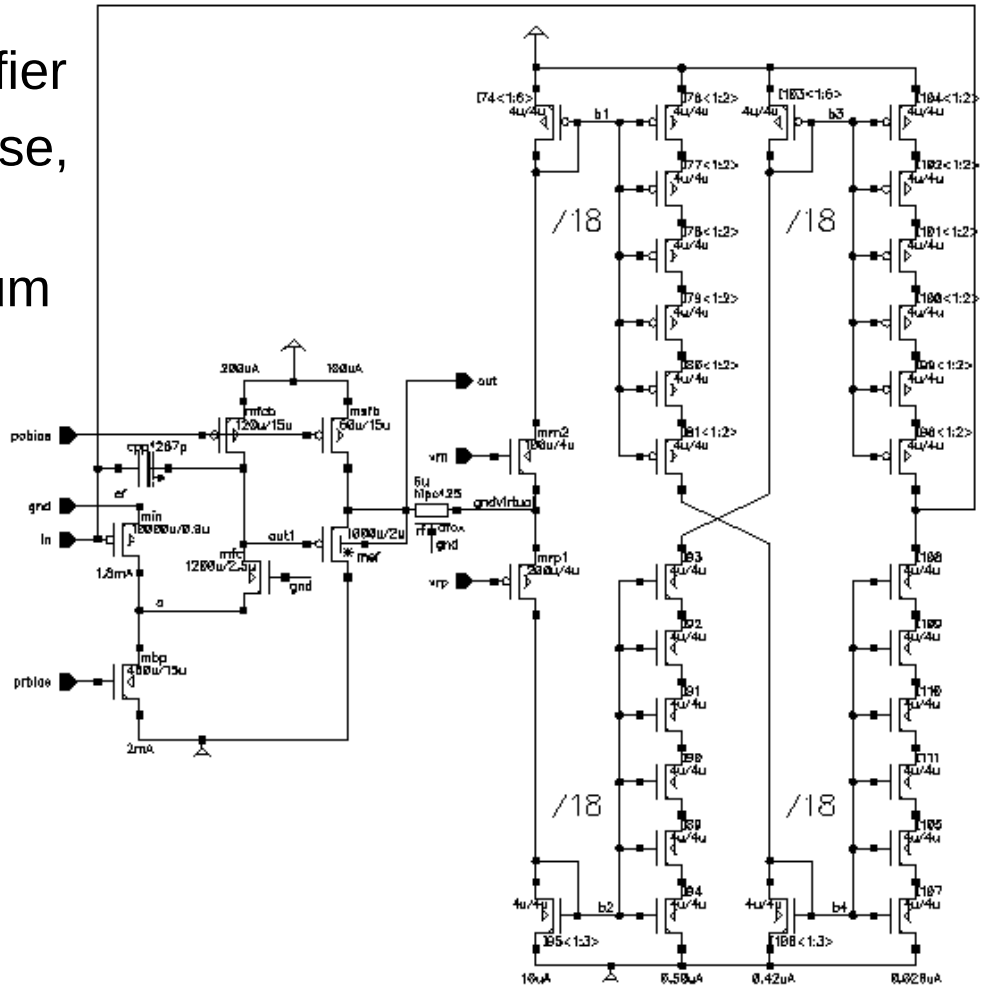
An Instrument on a Chip

Analog circuits / 1

- CSA
  - Charge sensitive amplifier
  - Integrates a charge pulse, into a voltage step
  - Input transistor: minimum noise (1/f & thermal):
    - W/L=10,000µ/0.9µ
    - I=1.8mA

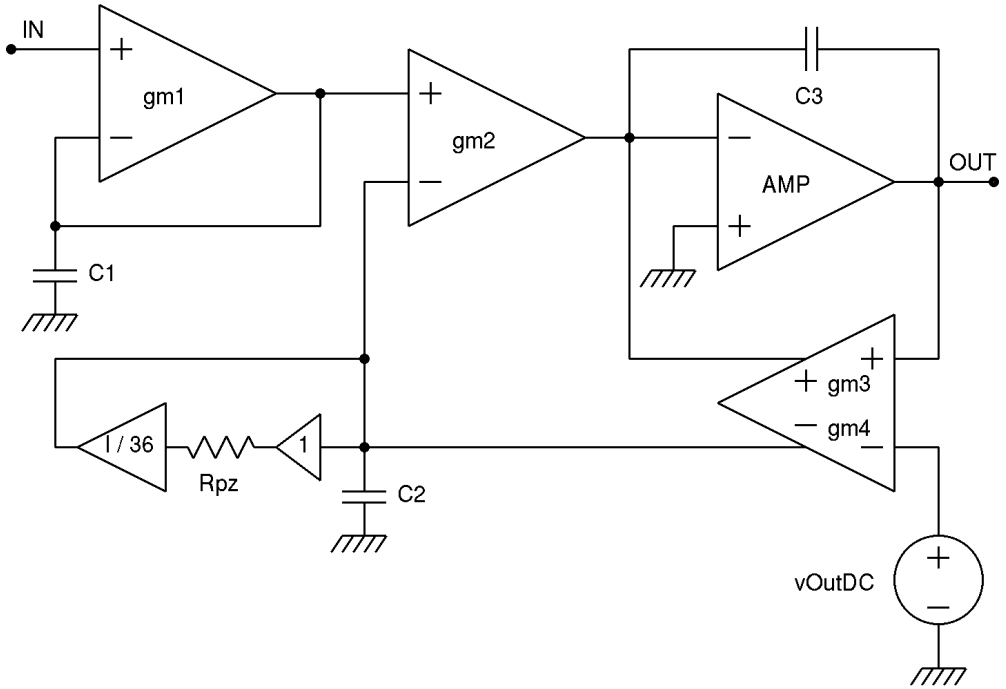


Delta Vout= Qin*Cf



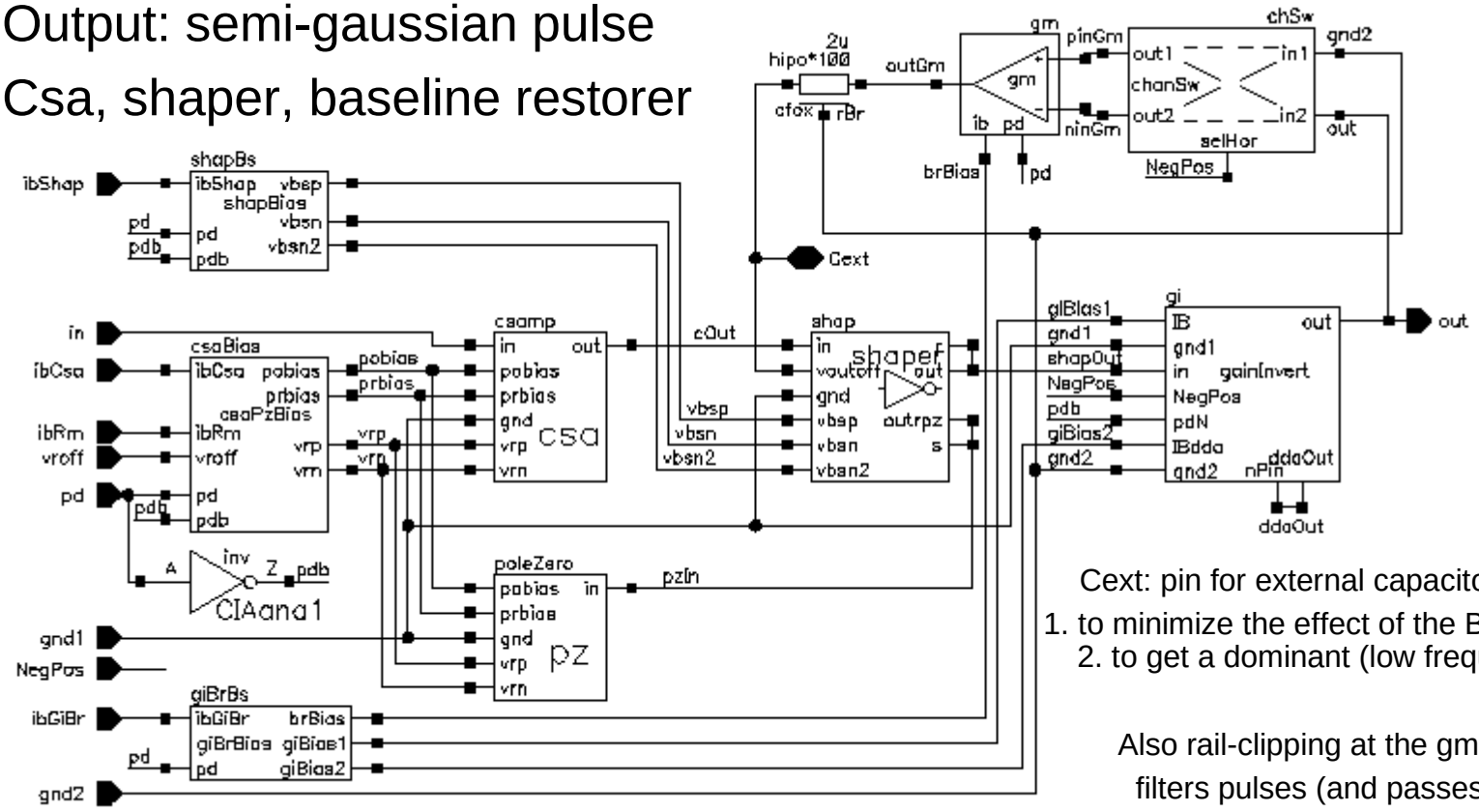
Analog circuits / 2

- Shaper (PSA, Pulse Shaping Amplifier)
  - Gm-C bandpass filter
    Optimises noise performance and counting rate
    - first-order high pass (differentiation)
    - second-order low pass
  - Rpz: pole-zero cancellation
  - vOutDC: sets output DC level; used by the BaselineRestorer



Analog circuits / 3

- Channel
  - Input: charge pulse
  - Output: semi-gaussian pulse
  - Csa, shaper, baseline restorer



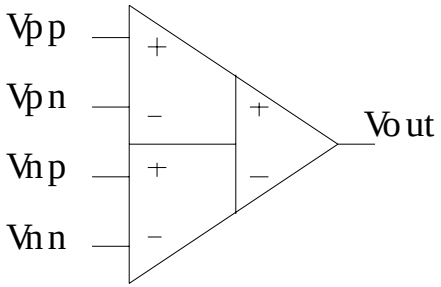
Cext: pin for external capacitor, 100nF.

1. to minimize the effect of the BR on pulses
2. to get a dominant (low frequent) pole

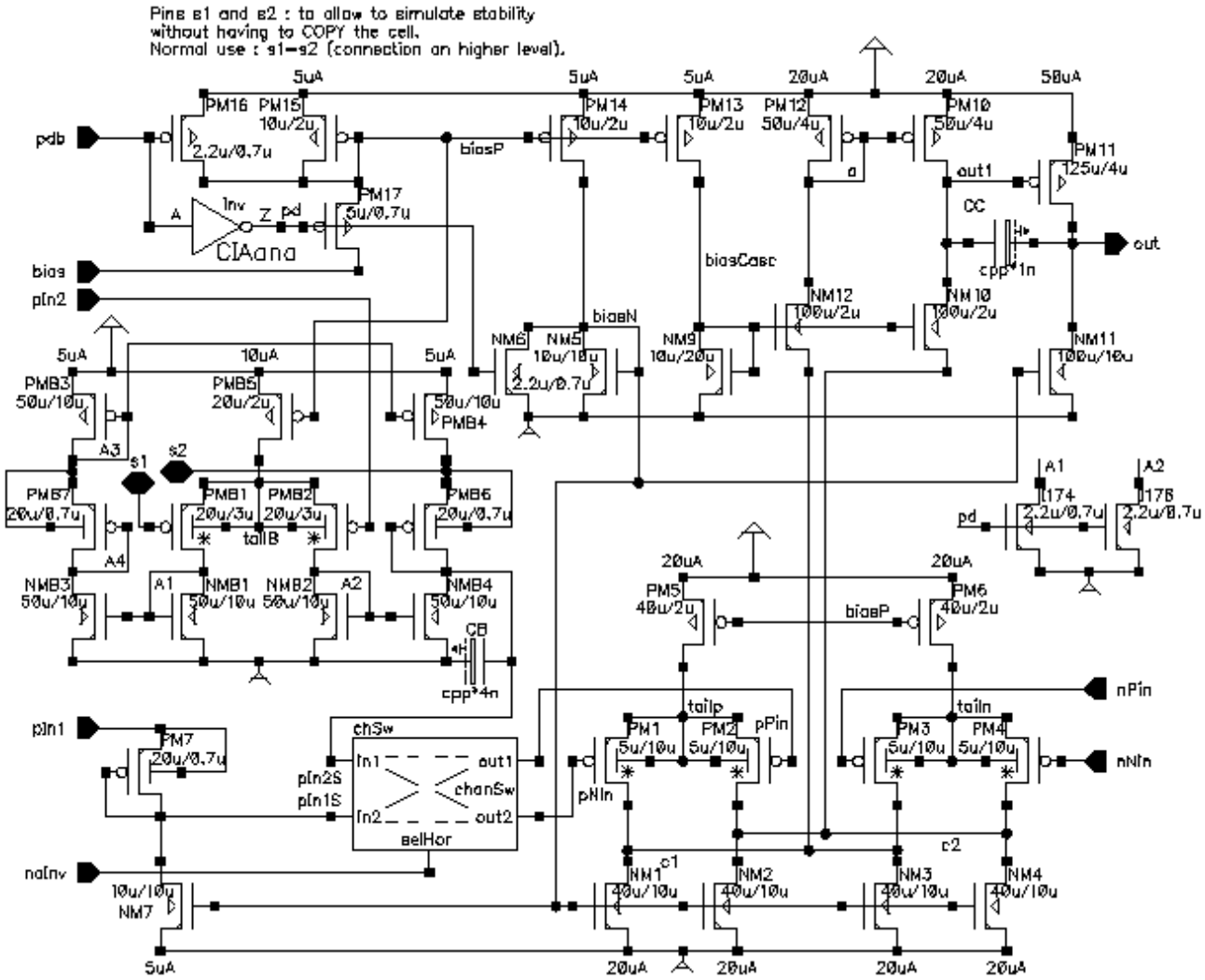
Also rail-clipping at the gm output filters pulses (and passes DC); non-linear filtering!

Analog circuits / 4

- DDA
  - Differential difference amplifier
  - Used to levelshift and invert *without* resistors (hence low power)



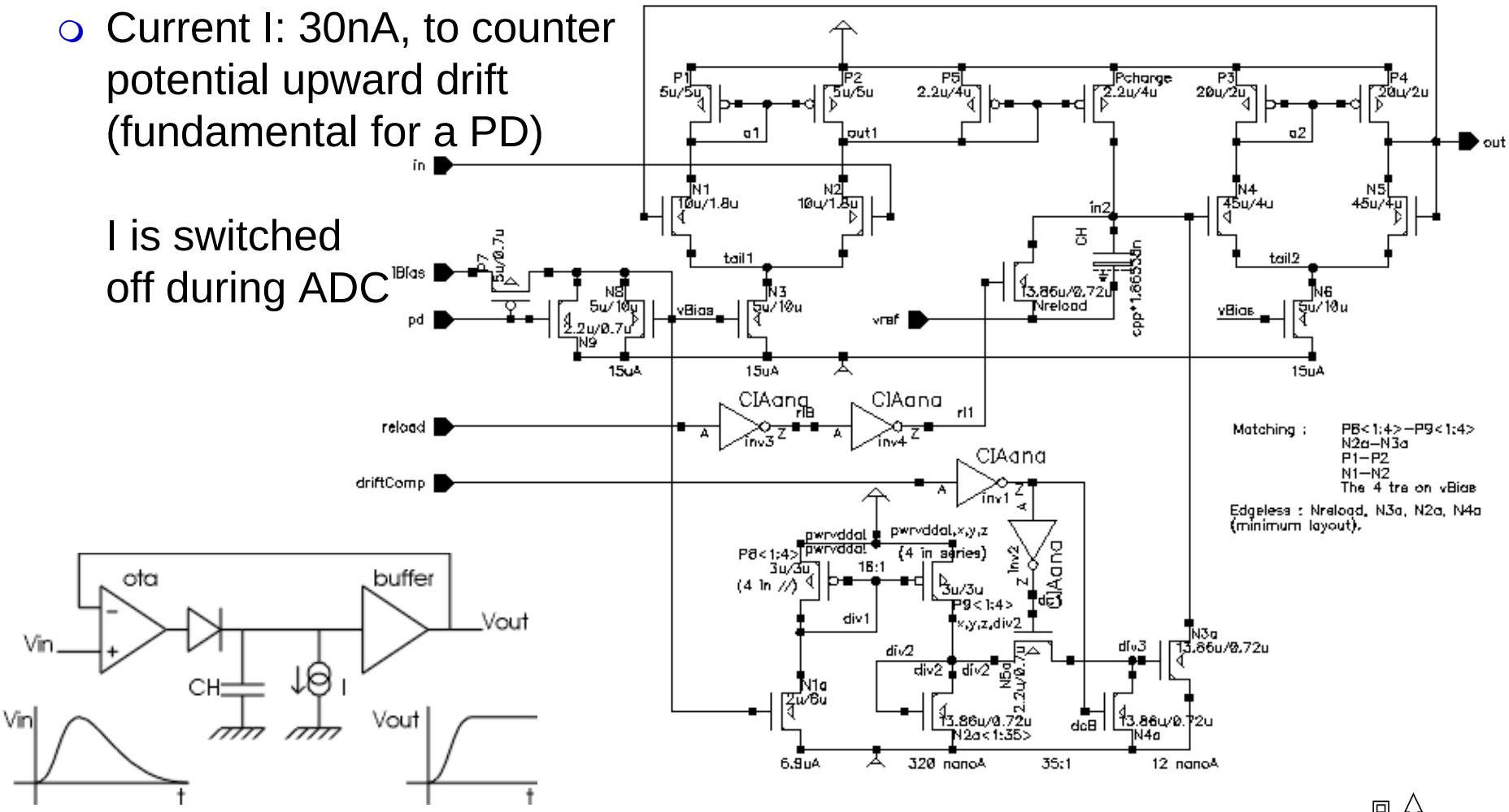
$$Vout = Aol*[(Vpp-Vpn)-(Vnp-Vnn)]$$



Analog circuits / 5

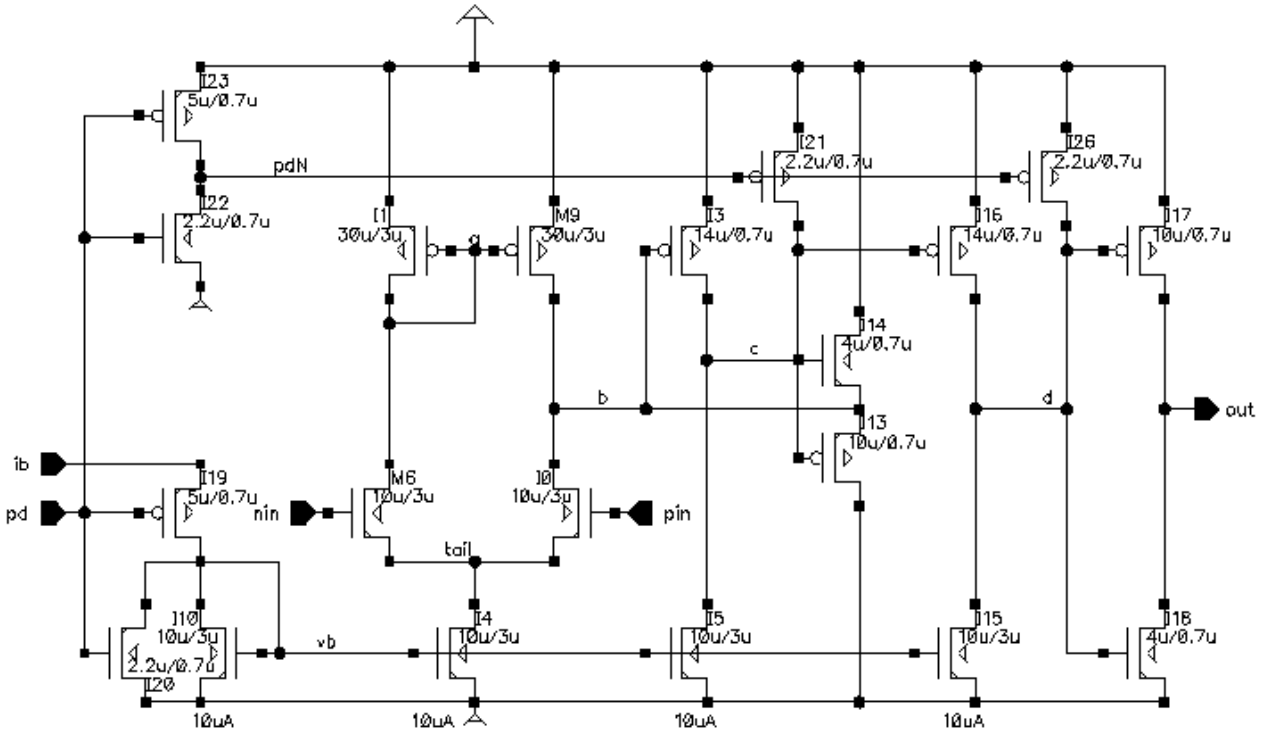
- Peak Detector Sample&Hold
  - Current I: 30nA, to counter potential upward drift (fundamental for a PD)

    I is switched off during ADC



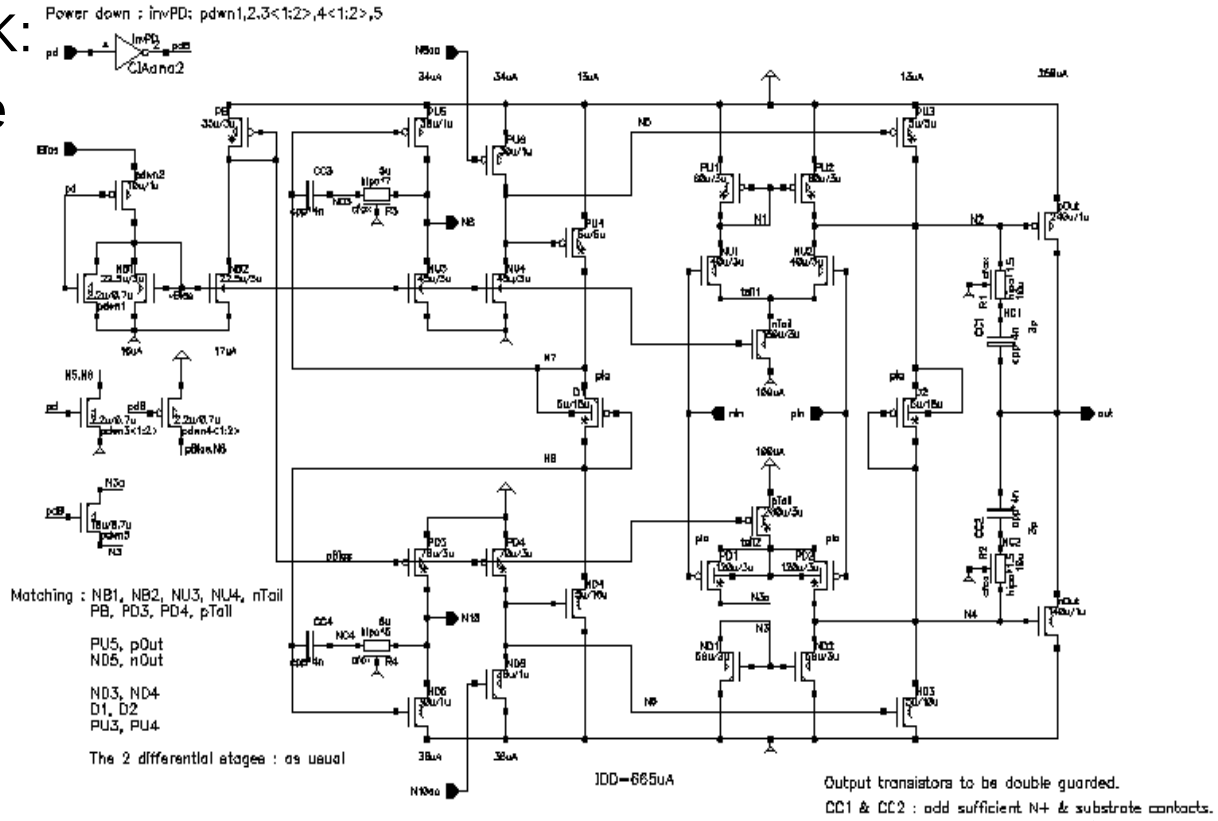
Analog circuits / 6

- Comparator
  - Very fast: 50ns @ 10mV differential input
    Because node b cannot move far



Analog circuits / 7

- ClassAB opamp
  - Only capacitive loads. Drives ADC and/or analog output.
  - Output stage quiescent current is well controlled, for low power
  - Standard cells: not OK:
    - (internal) slew rate too low
    - power too high

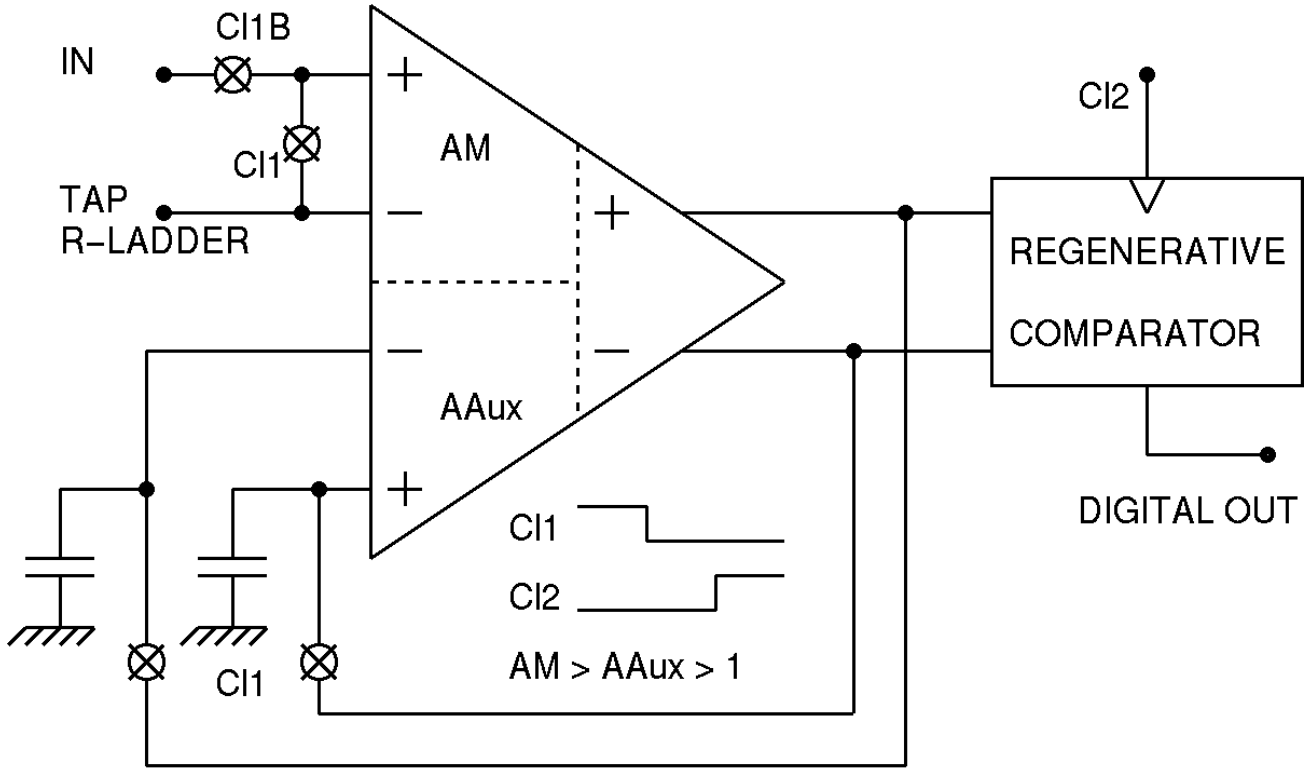


ADC / 1

- Architecture:
  - Two-step flash
    4 MSB's first; then 4 LSB's
  - Two resistive ladders, 16 units each
    - coarse ladder low resistive
    - fine ladder high resistive
  - Comparators
    - CMOS : Vos = 10 mV (3-sigma)
    - 1LSB = 11 mV
    - ⇨ auto - zeroing necessary
  - 250 K conversions/s
  - 30 mW

ADC / 2

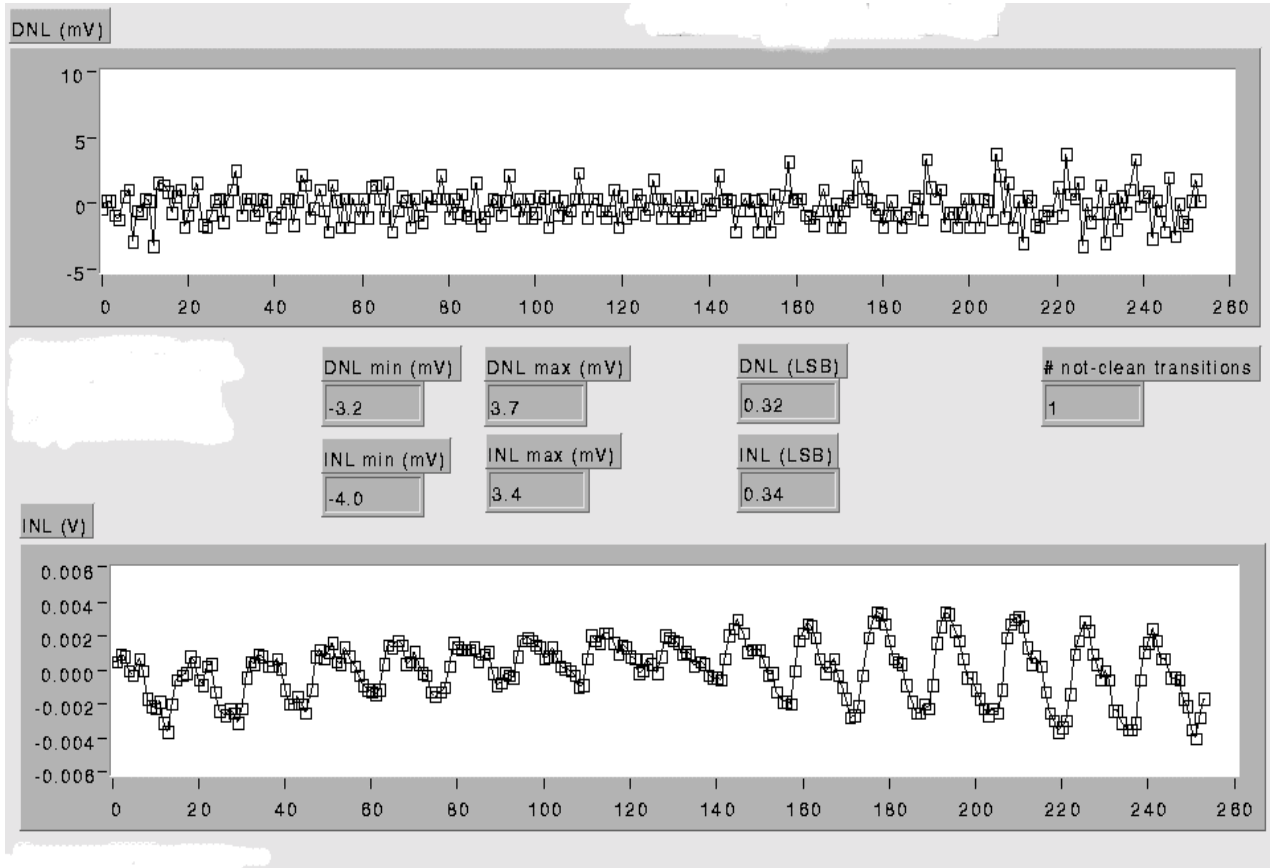
- Clocked comparator
  - Auto-zeroing (or correlated double sampling) ⟹ Offset < 100µV
    Only possible because no continuous operation



Residual offset = VosMain/AAux + DiffClockFeedThrough*AAux/AM

ADC / 3

- Measurement results
  - LabVIEW / GPIB setup
  - ADC stand-alone
  - DNL = 0.32 LSB
    INL = 0.34 LSB



Digital part

- Serial interface, 32 bits
  - Control (input)
    - operating modes
    - various controls (e.g. gain)
    - discriminator levels
  - Status (output)
    - voting & parity errors
    - some pin settings
  - Cascadability (scalability)
- Parallel output (ADC). Latching or none-latching.
- 4 MHz clock, 1500 equivalent gates, VHDL, decoding&control
- To minimize disturbances of the analog
    - event driven (PDFE quite, except some 30 FF's, until peak latched)
    - I/O: TLL, very long rise & fall times

Mixed mode simulations / 1

- Table with main functional modes

PDFE : modes — Rev. 04.11.99

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RESET_N (pin)	Test (pin)	AOutSel (pin)	Bit8	Bit9	Bit10	Main chan / PSACSAOn	Main DAC, ED / EDOn	Coinc chan, DAC, ED / CDOn	PDSH / PDSHOn	Buffer / BUFOn	ADC / ADCOn	Extinp (=~PSACSAOnB)	BypassAAF	quiet	Reload	driftComp	EDDirect	CoEDDirect	ADCMode	XCoInhReload	External coincidence	Anti-coincidence	Description
	Input signals					power up / signals						to ana					digital set						
1	0	0	0	0	0	1	1	1	1	1	1	0	X	0	EN	EN	0	0	0	0	0	1	Coincidence detection mode; anti-coincidence mode; digital out Default mode 0
1	0	0	0	0	1	1	1	1	1	1	1	0	X	0	EN	EN	0	0	0	0	0	0	Coincidence detection mode; coincidence mode; digital out
1	0	0	0	1	0	1	1	0	1	1	1	0	X	0	EN	EN	0	0	0	0	1	1	Charge amplification mode; anti-coincidence mode; digital out
1	0	0	0	1	1	1	1	0	1	1	1	0	X	0	EN	EN	0	0	0	0	1	0	Charge amplification mode; coincidence mode; digital out
1	0	0	1	0	0	1	1	1	1	1	1	0	X	0	EN	EN	0	0	0	0	1	1	Charge amplification mode; anti-coincidence mode; digital out; coinc chan on, isolated
1	0	0	1	0	1	1	1	1	1	1	1	0	X	0	EN	EN	0	0	0	0	1	0	Charge amplification mode; coincidence mode; digital out; coinc chan on, isolated
1	0	0	1	1	0	0	0	0	0	1	1	1	0	0	X	X	0	0	1	0	NA	NA	ADC-only mode
1	0	0	1	1	1	0	0	0	0	0	0	X	X	1	X	X	0	0	0	0	NA	NA	Quiet mode (everything in power down, except crystal oscillator and part of ADC)
1	0	1	0	0	X	1	1	1	0	1	0	0	X	0	X	X	0	0	0	0	NA	NA	Coincidence detection mode; analog out Default mode 1
1	0	1	0	1	X	1	1	0	0	1	0	0	X	0	X	X	0	0	0	0	NA	NA	Charge amplification mode; analog out
1	0	1	1	X	X	0	0	0	0	1	0	1	1	0	X	X	0	0	0	0	NA	NA	Buffer-only mode (AAF bypassed); quasi-quite mode (as quite mode, but buffer on)
1	1	1	0	0	0	1	1	1	1	1	1	0	X	0	EN	EN	0	0	0	0	0	1	Testmode : as 00000, but buffer to pin bufOut (to observe PDSH)
1	1	1	0	0	1	0	1	0	1	1	0	1	1	0	EN	1	1	0	0	1	NA	NA	Testmode PDSH and MDED (via PDSH). MDED output direct to EDOut
1	1	1	0	1	0	1	1	0	0	1	0	0	X	0	X	X	1	0	0	0	NA	NA	Testmode : as 0101X, but MDED output direct to pin EDOut
1	1	1	0	1	1	0	0	1	0	0	0	X	X	0	X	X	0	1	0	0	NA	NA	Testmode coincidence channel (main channel etc. off), CDED output direct to ICoOut
1	1	1	1	0	0	1	1	0	1	1	0	0	X	0	EN	0	1	0	0	1	NA	1	Testmode : as 00010, but ADC off, buffer to pin bufOut and MDED output direct to EDOut
1	1	1	1	0	1	0	1	0	0	0	0	1	1	0	X	X	1	0	0	0	NA	NA	Testmode : direct test of MDED and MDDAC
1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	X	X	0	0	1	0	NA	NA	Testmode : as 00110 (= ADC-only mode), but AAF bypassed
1	1	0	0	0	1	0	1	0	1	1	1	1	1	0	EN	EN	0	0	0	0	1	1	Testmode : as 00010, but main channel off, external input to PDSH
1	1	0	X	1	X	0	0	0	0	0	0	X	X	1	X	X	0	0	0	0	NA	NA	Testmode 1 digital part
1	1	0	1	X	X	0	0	0	0	0	0	X	X	1	X	X	0	0	0	0	NA	NA	Testmode 1 digital part
1	1	1	1	1	0	0	0	0	0	0	0	X	X	1	X	X	0	0	1	0	NA	NA	Testmode 2 digital part
1	1	1	1	1	1	0	0	0	0	0	0	X	X	1	X	X	0	0	0	0	NA	NA	Testmode 3 digital part
0	X	X	X	X	X	0	0	0	0	0	0	X	X	1	X	X	0	0	0	0	NA	NA	Powerdown mode (everything in power down, except crystal oscillator and part of ADC)

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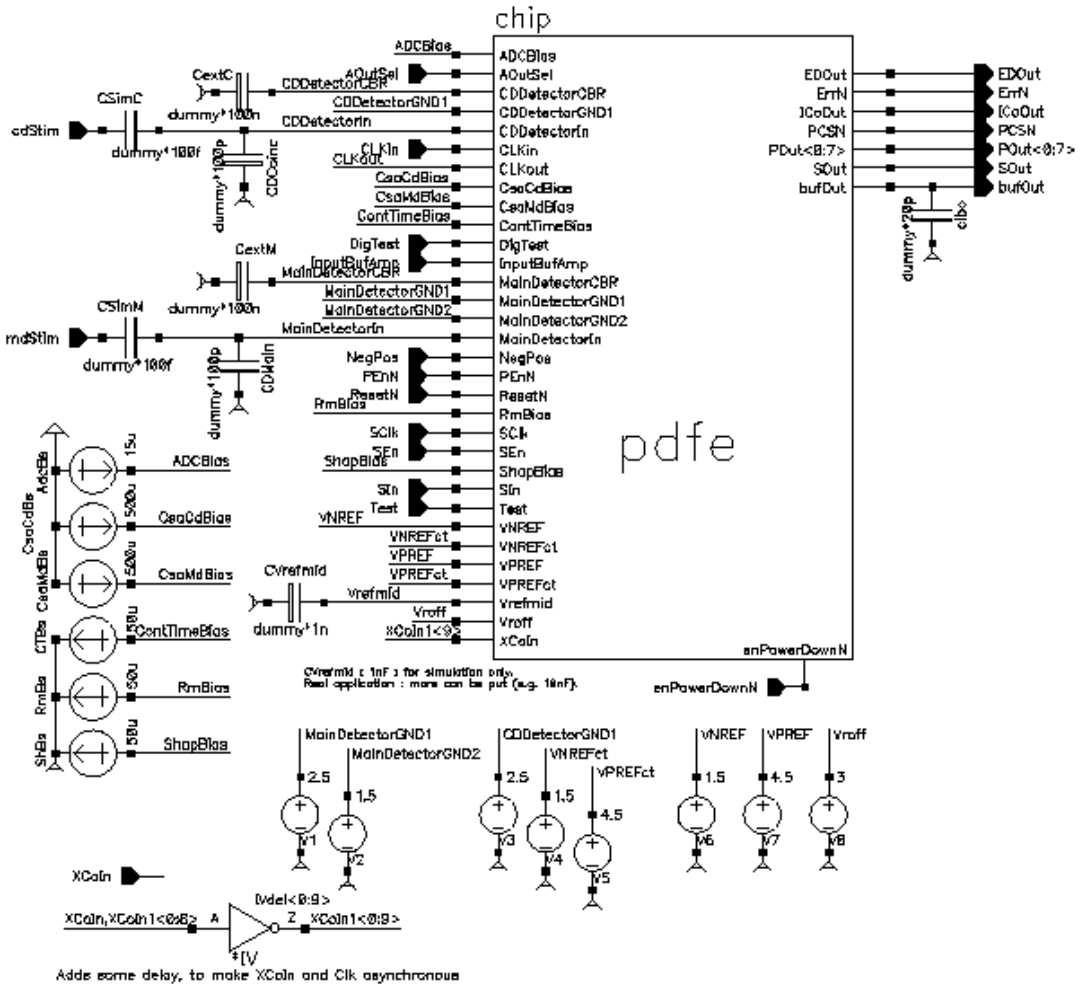
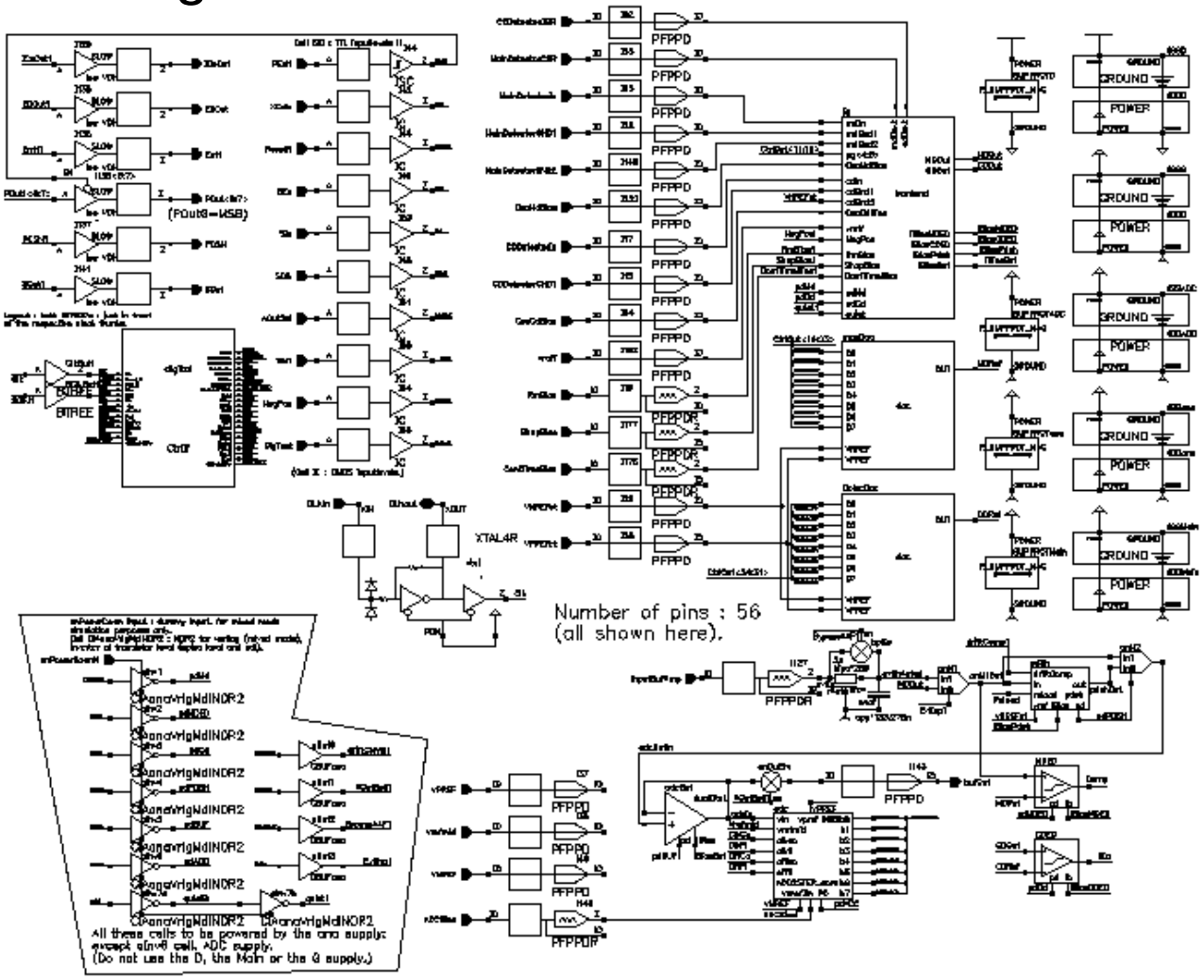
Mixed mode simulations / 2

- Chip + external components: simulation schematic



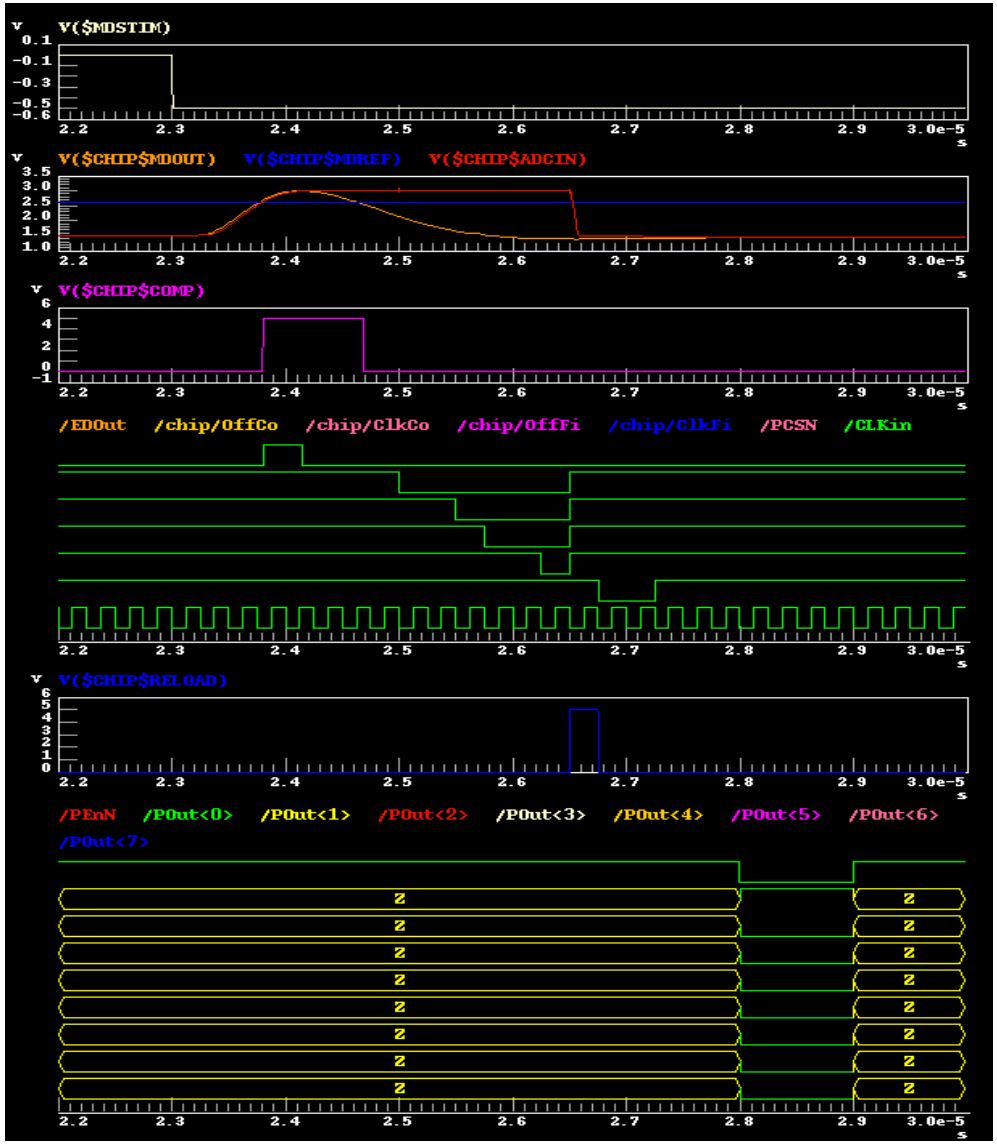
Mixed mode simulations / 3

- Chip: toplevel design schematic

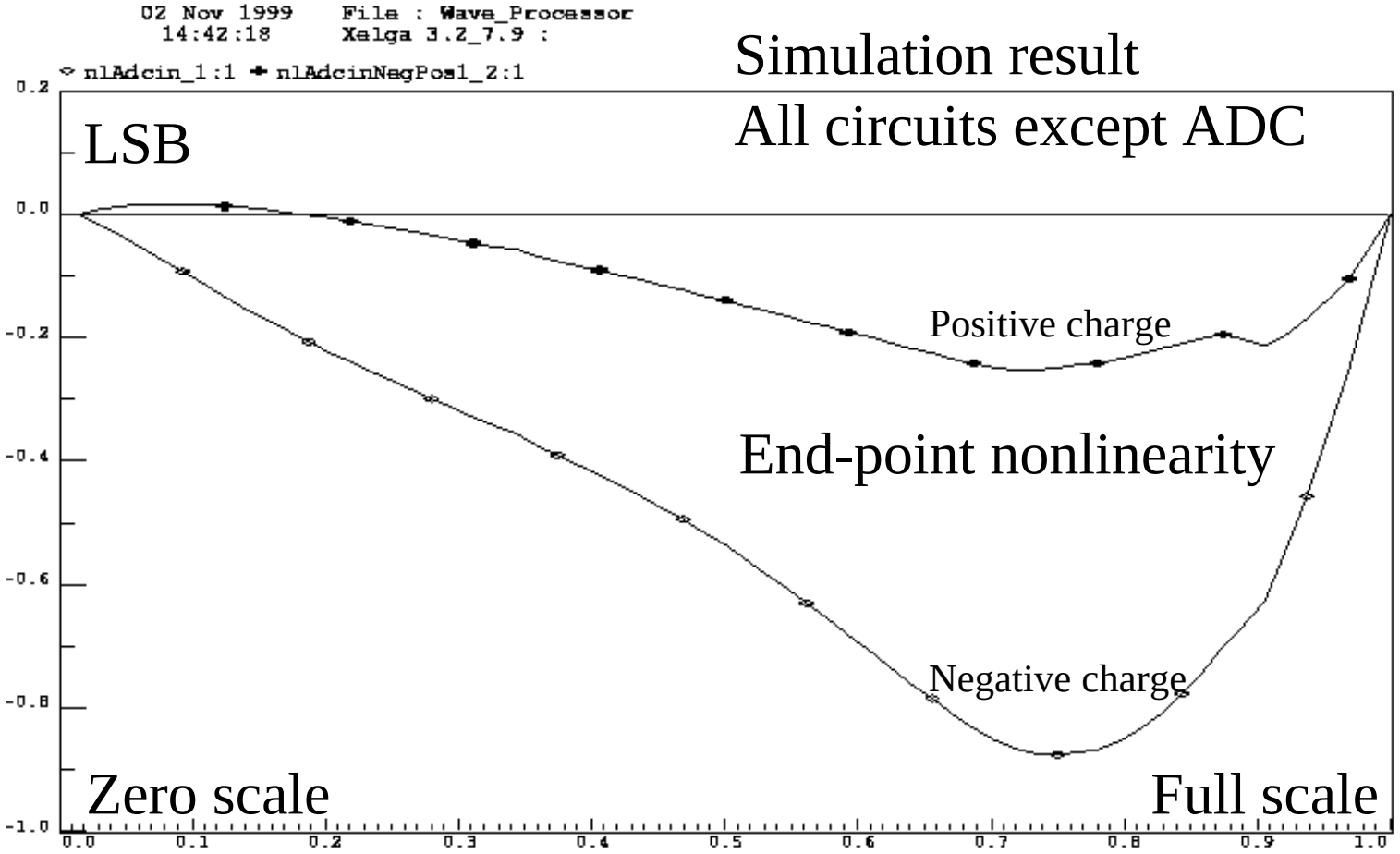


Mixed mode simulations / 4

- Co-simulation: spice - verilog
- Essential for PDFE:
  - Many operating modes
  - Complex interaction analog ⟺ digital
    - event driven
    - asynchronous
    - loops



Nonlinearity



Best Straight Line nonlinearity < 0.5 LSB

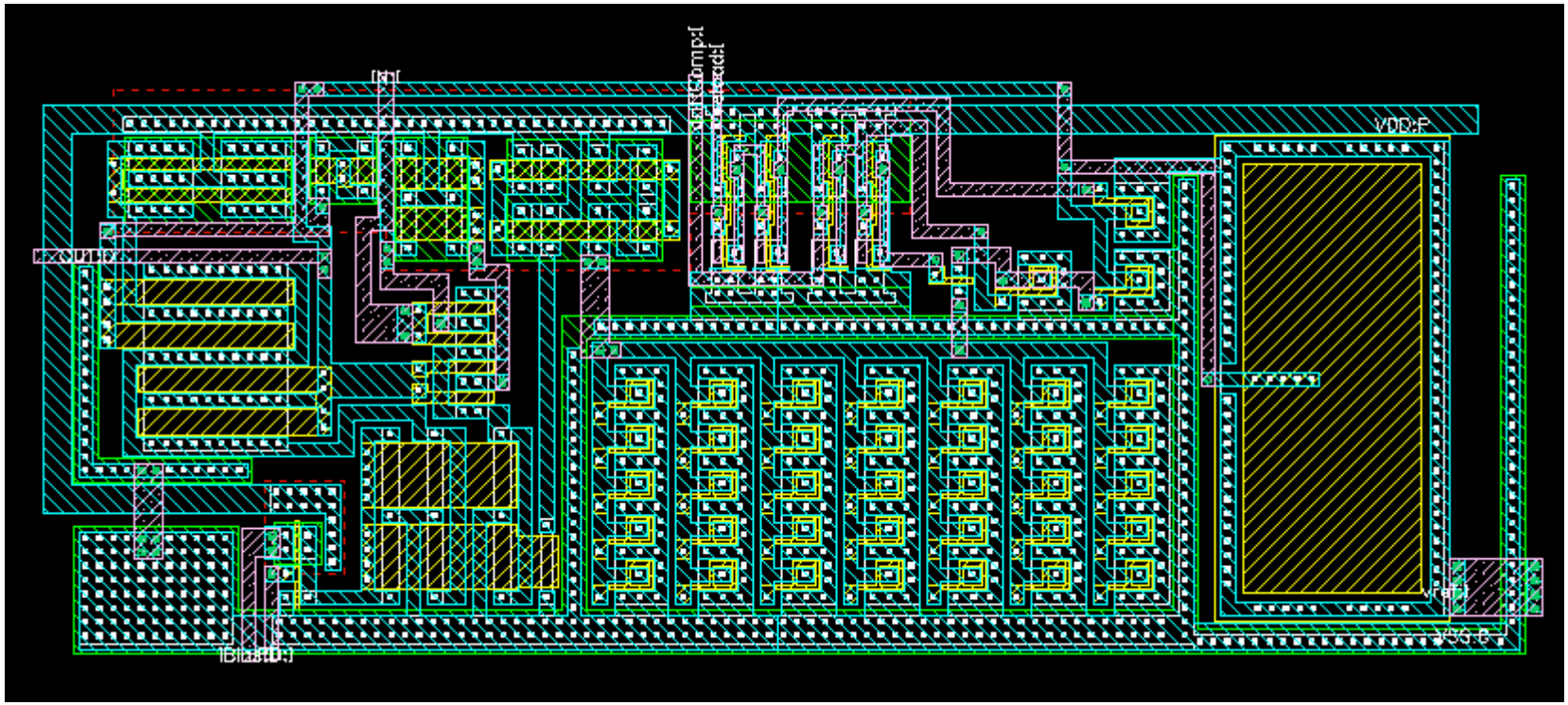
Errors somewhat proportional with signal

Radiation Hardness

- Total Dose: analog and digital part: good up to 12 krad.
  - Parasitic MOS transistor field-oxide leakage: gate-all-round layout for critical NMOS devices (determined by simulation)
  - Gate oxide threshold voltage drift:
    corner analysis, and assume that no Worst Case wafer (limited volume)
- Single Event Upsets: digital part
  - Cell level: foundry library screened for least sensitive cells
  - Rt (register transfer) level:
    - feedback avoided as much as possible (no FSM's)
    - parity bits
    - majority voting for critical registers (EDAC)
- Single Event Latch-up
  - Thin epi layer on top of a heavily doped and hence low impedance substrate $\Longrightarrow$ intrinsically robust for latch-up. Latches up under Cf256.

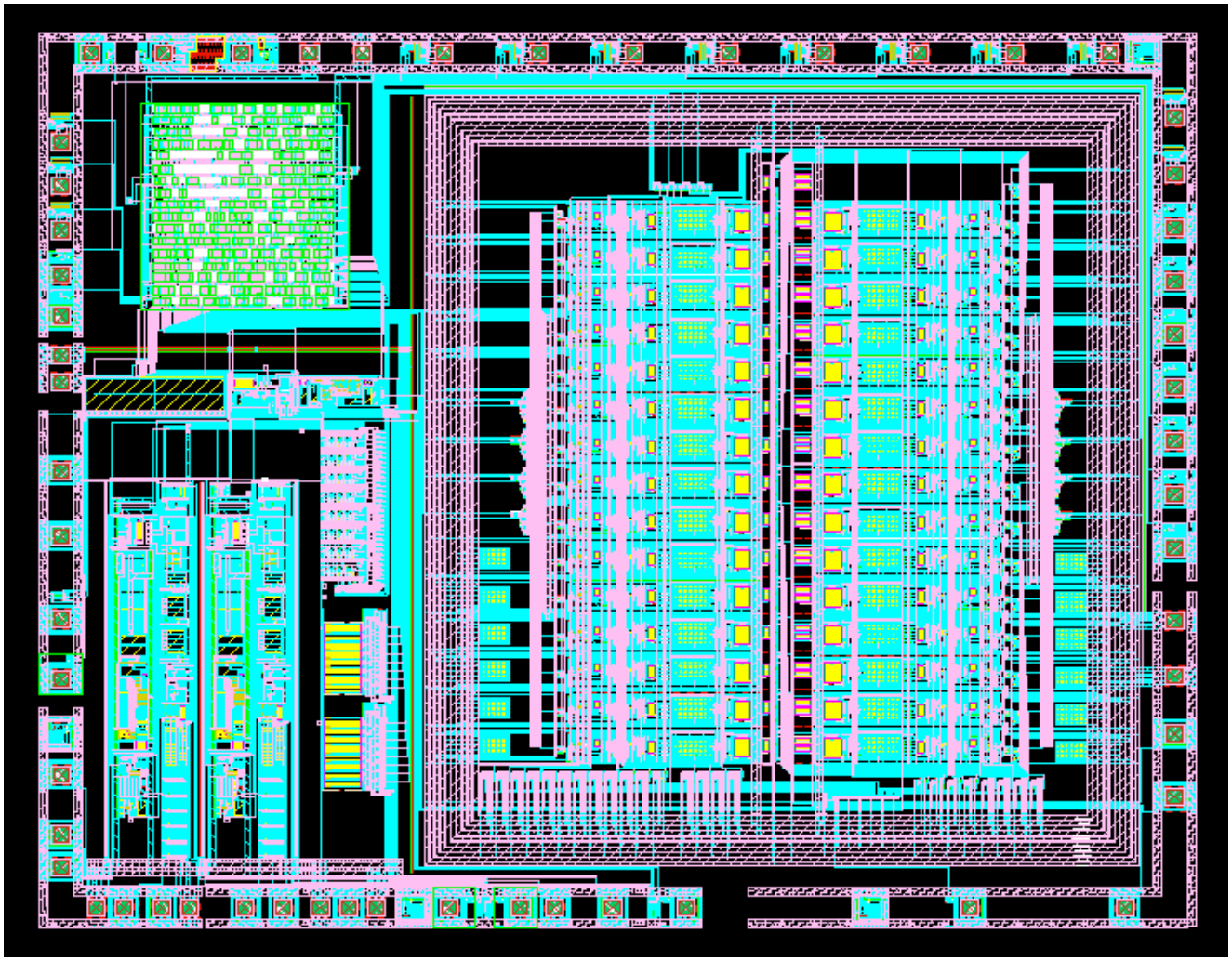
Edgeless transistor layout

- Significantly increases the total dose immunity
- Applied in the peak detector's anti-drift current source



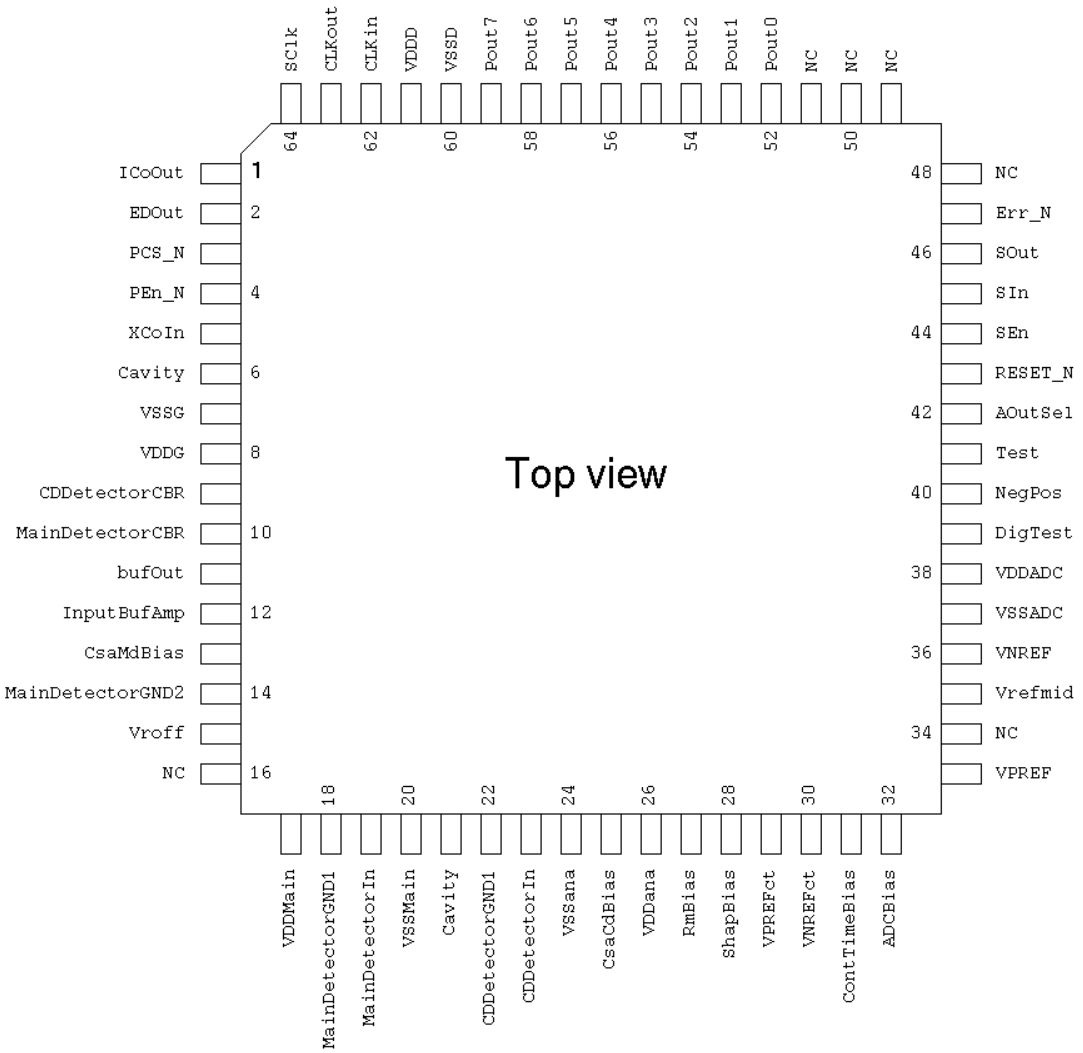
Layout

- Die size : 31 square mm



Package

- 64 pins Quad Flat Package
- 56 pins used



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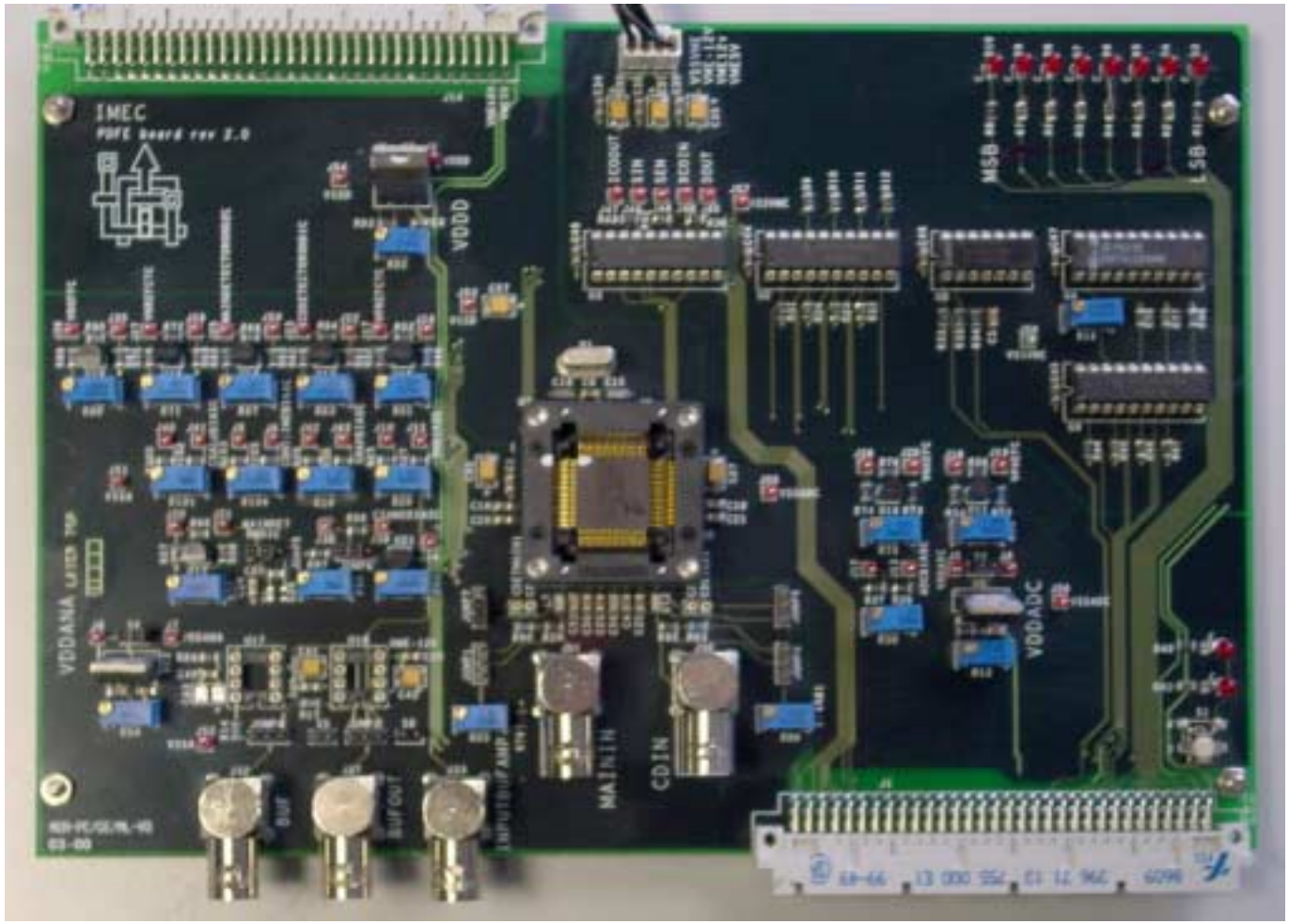
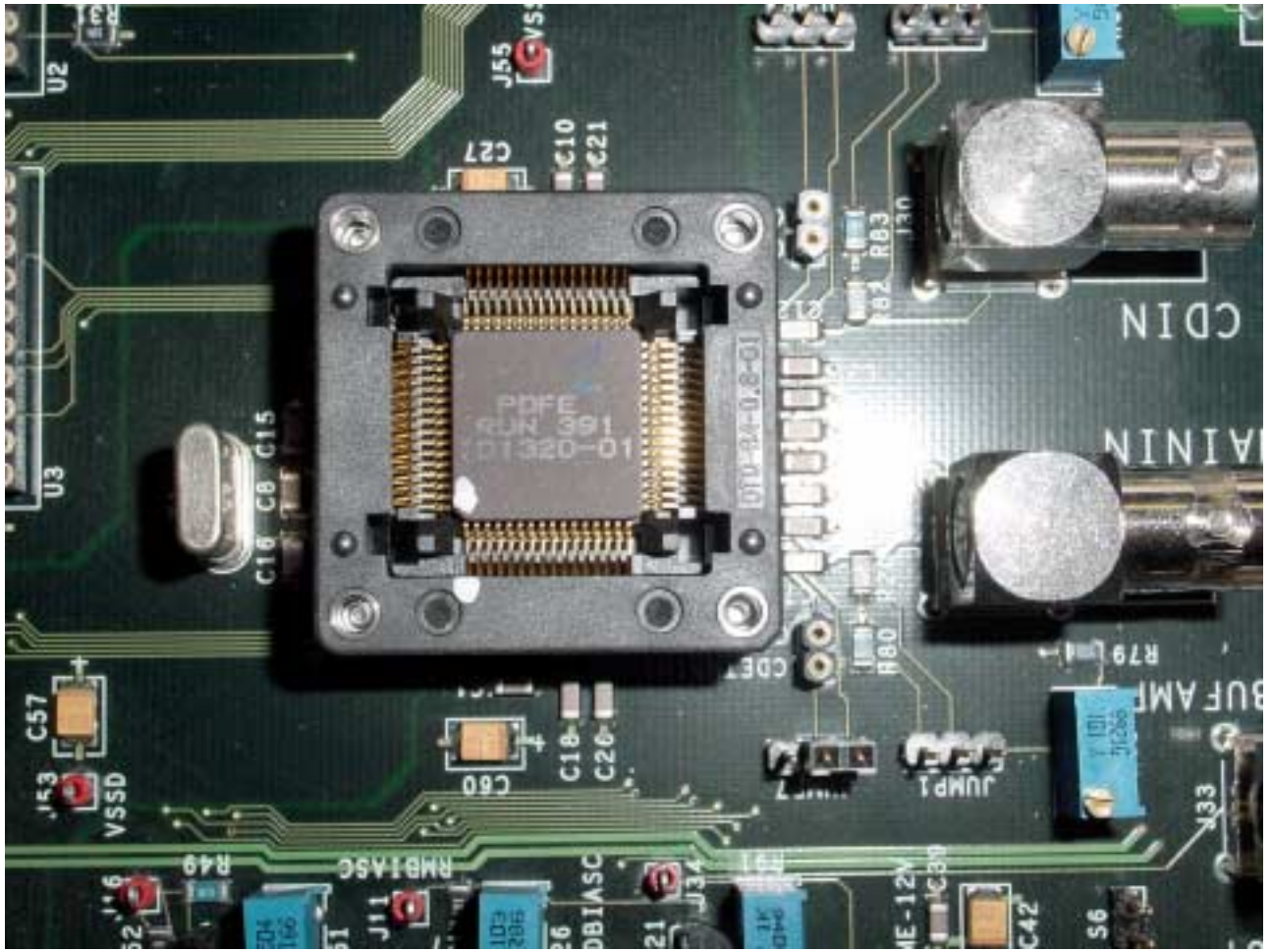
Debug PCB / 1

- VME board



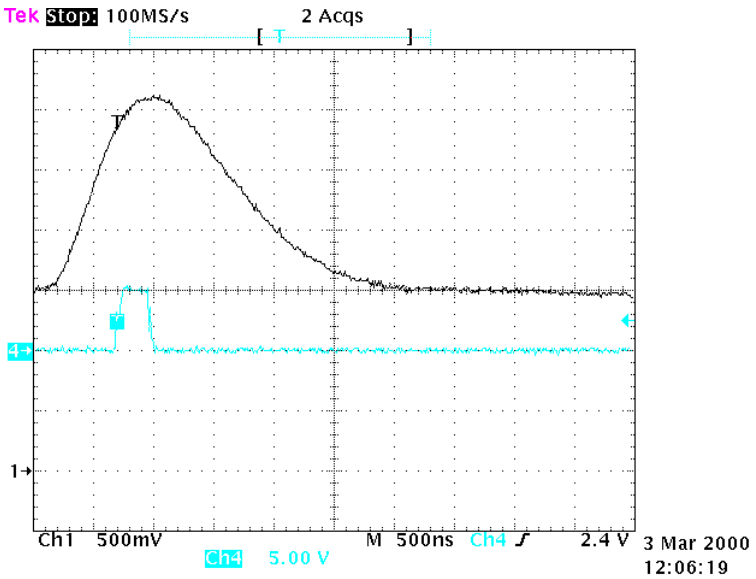
Debug PCB / 2

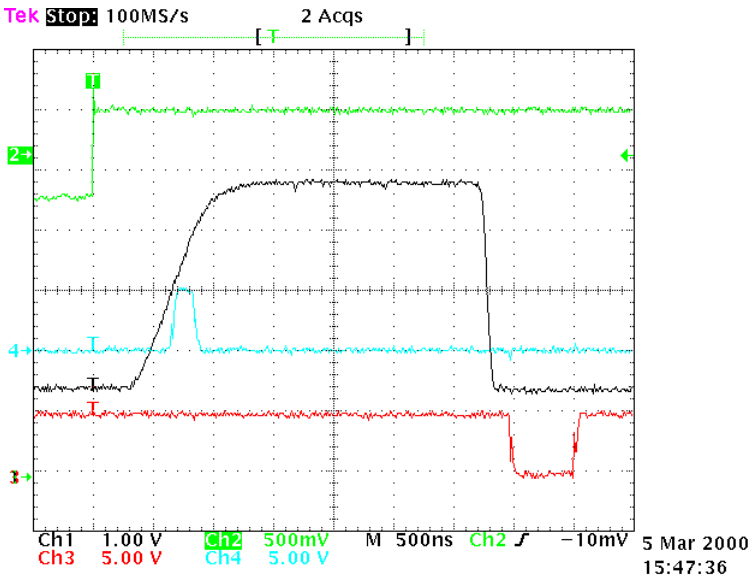
- The two inputs close to the asic



Analog pulses

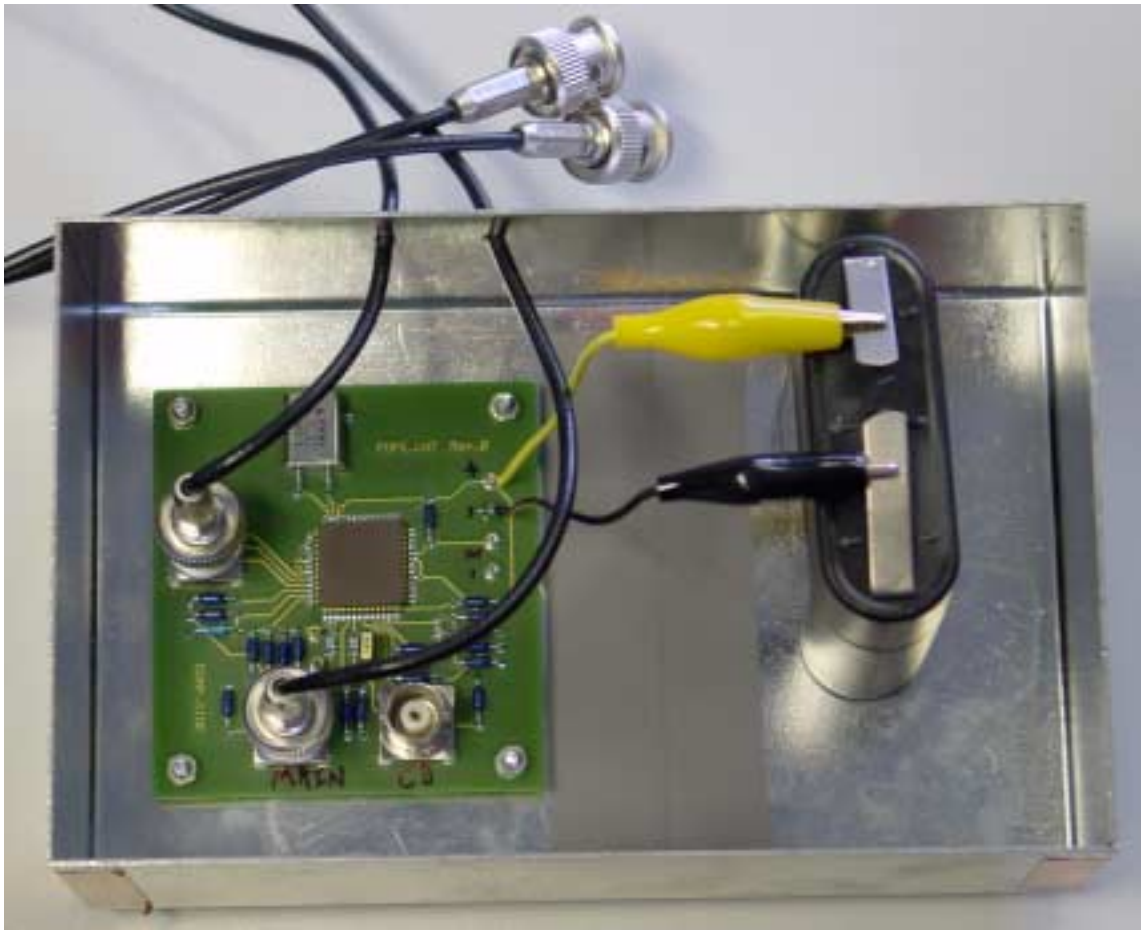
- Analog output mode
  - Semi-gaussian output pulse
  - Event detector out
- Digital output mode
  - Charge input (V-step on Cseries)
  - Peak detector output
  - Event detector out
  - End of A-to-D conversion





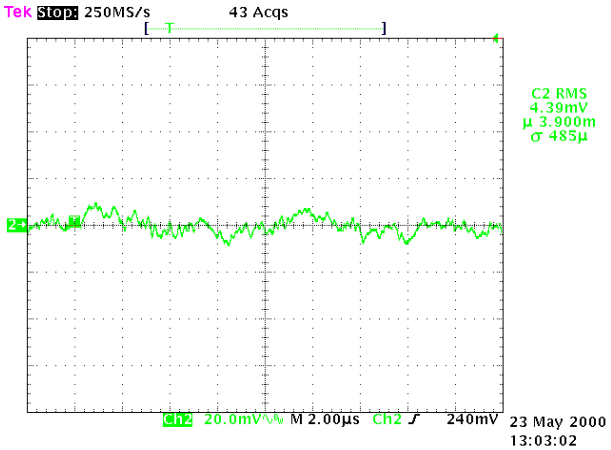
Low noise PCB / 1

- Only passive external components
- Battery-powered; faraday cage

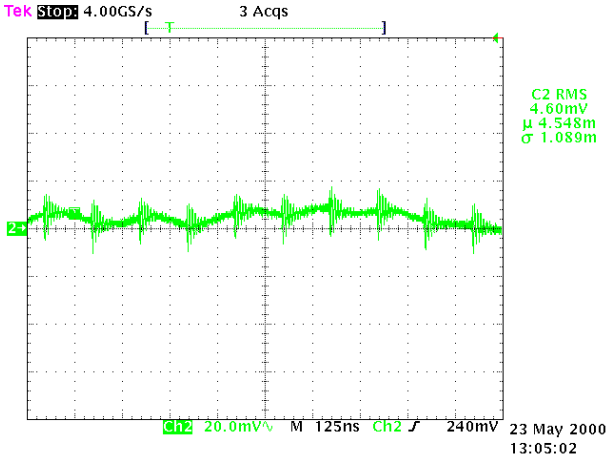


Low noise PCB / 2

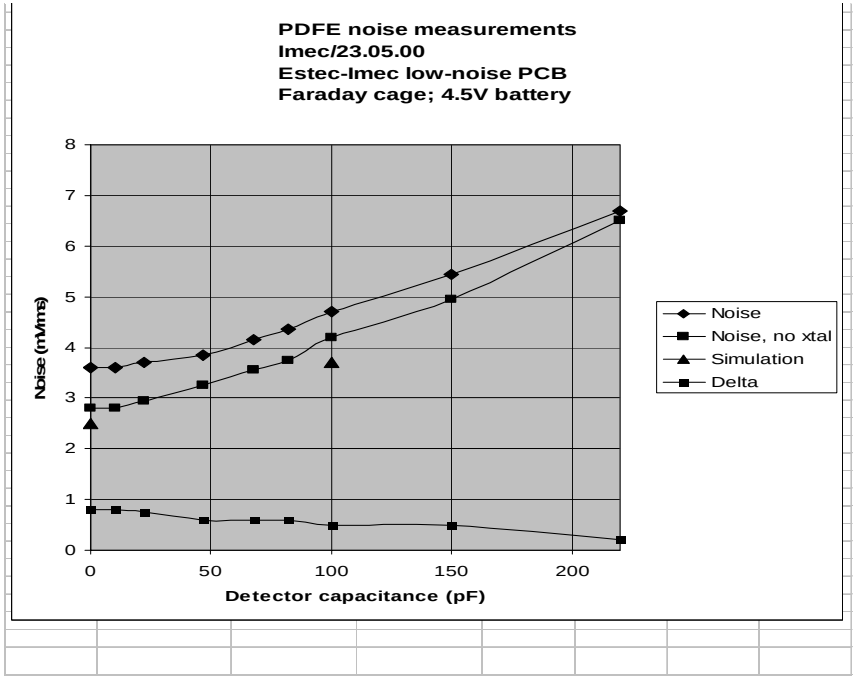
- Crystal (digital) *not* running



- Crystal (digital) running



- Noise(detector capacitance)
- With and without crystal running
- Measured with zero input signal
- 1mVrms corresponds to an ENC of 207electrons



imec

Status & conclusions

- A low power low noise PDFE is realized
- Implements all analog processing up to (& including) the ADC
- Mixed analog digital design
- High re-usability and scalability
- Samples available since 1 year
- Device is fully functional
- Evaluation board allows all kind of settings and measurements
- Low noise board for noise characterization
- Estec is building an instrument for STEREO, using PDFE

- Technical paper available, from the ESCCON 2000 conference
- Datasheet available

Application: NASA's STEREO mission

- Study of solar eruptions
- PDFE to be part of the SEPT experiment (IMPACT instrument)
- Launch: 2004
- http://stprobes.gsfc.nasa.gov/stereo.htm