ESA-ESTEC GSTP4 - Analog Silicon Compiler for Mixed Signal ASICs

PDFE: A *Particle Detector Front-End ASIC*
PDFE: collaborators

- PDFE is the result of a collaboration between:
  - ESA-Estec
    - S. Habinc, B. Johlander, T. Sanderson
  - KULeuven, ESAT-MICAS
    - G. Gielen, J. Vandenbussche, G. Van der Plas
  - IMEC, Invomec
    - C. Das, K. Marent, S. Redant, J. Wouters

- PDFE is designed by IMEC, Invomec
Presentation overview

- Basic functionality
- Concept
- PDFE characteristics:
  - functionalities
  - block diagram
  - specs
  - programmability
- Some analog cells
- Digital part
- Simulations
- Radiation hardness
- Evaluation PCB’s & some measurement results
- Status & Conclusions
Basic functionality

- CSA
- PSA
- Peak detection
- DAC and discriminator
- ADC
Basic functionality: 1 conversion cycle

- One full cycle takes 4μs

Diagram showing the main charge event and next main charge event with various voltage levels and timing details.
Concept

- Miniaturized Microcontroller based Read-out Electronics for Space Application (Energetic Particle Instrumentation)
- PDFE together with a 8052-based Microcontroller
- Architectural design drivers:
  - Low noise, low power
  - Low mass $\iff$ Low chip count
  - Single supply voltage $\iff$ simple power supply
  - Integrated ADC
  - Integrated standard space craft interface
  - Re-usability and scalability
    - because high NRE cost & long development time
  - Tolerance against single event effects and total ionizing dose
  - Mixed analog and digital signals
  - Testability and reliability (monolithic)
Main PDFE functionalities

- Main channel: charge amp, pulse shaping, baseline restorer, peak detector S/H
- (Anti-)coincidence channel
- Internal or external (anti-)coincidence gating
- Build-in 8-bit discriminators
- Gain adjustment (+/-5%)
- Linear 8-bit ADC, two-step flash
- Completely event driven
- Cascadable 32 bits serial control/status interface (scalability)
- 8-bit parallel output interface
- All internal registers SEU protected
- Low speed low amplitude digital I/O (to limit noise)
- Non-active blocks powered down
PDFE block diagram

Supply pins, voltage reference pins, analog ground pins and pins for external capacitors are not shown.

Powerdown signals: MainChPwr, CDChPwr, PDSHPath, BbPwr, ADCPwr, PDSHSelInt, bypassAAF
Main specifications

- Detector capa  100 pF
- Detector leakage  1 nA
- Full Scale input  0.1 pC
- Conversion gain  30 mV/fC
- Noise (ENC)  800 e⁻ rms (@ 100 pF)
- Peaking time  1 µs
- Counting rate  250 Ks/s @ 2.5 fC
  25 Ks/s @ 0.1 pC
- Baseline drift  15 mV
- Nonlinearity  1 LSB
- Number of channels  2
- ADC resolution  8 bit
- ADC INL and DNL  ½ LSB
- Power supply  5 V
- Power consumption  One channel: 15 mW
  ADC: 30 mW
  Total: 70 mW
- Ambient temperature  -40 to 65 °C
- Technology  0.7-µm CMOS, mixed-signal, Alcatel Microelectronics
- Package  64-pins quad flat pack
  56 pins used
Programmability

- Using the serial control/status interface
  - Coincidence channel enable/disable
  - Coincidence or anti-coincidence gating
  - Internal or external coincidence input
  - Discriminator levels (two 8-bit DACs)
  - Conversion gain adjustment (+/-5%)
  - ADC stand-alone
  - Power down

- Using digital pins (VSS - VDD strapped)
  - Charge sign
  - Analog or digital (ADC) output
  - Parallel output interface (ADC):
    internal or external control of the update
    (non-latching or latching mode; PROM or µP bus)
PDFE: An Instrument on a Chip
Analog circuits / 1

- **CSA**
  - Charge sensitive amplifier
  - Integrates a charge pulse, into a voltage step
  - Input transistor: minimum noise (1/f & thermal):
    - \( \frac{W}{L} = 10,000\mu \text{m}/0.9\mu \text{m} \)
    - \( I = 1.8\text{mA} \)

\[ \text{Delta} V_{out} = Q_{in} \cdot C_f \]
**Analog circuits / 2**

- **Shaper (PSA, Pulse Shaping Amplifier)**
  - Gm-C bandpass filter
    - Optimises noise performance and counting rate
      - first-order high pass (differentiation)
      - second-order low pass
  - Rpz: pole-zero cancellation
  - vOutDC: sets output DC level; used by the BaselineRestorer
Analog circuits / 3

- Channel
  - Input: charge pulse
  - Output: semi-gaussian pulse
  - Csa, shaper, baseline restorer

Cext: pin for external capacitor, 100nF.
1. to minimize the effect of the BR on pulses
2. to get a dominant (low frequent) pole

Also rail-clipping at the gm output
filters pulses (and passes DC);
non-linear filtering!
**DDA**

- Differential difference amplifier
- Used to levelshift and invert *without* resistors (hence low power)

\[ V_{out} = A_0 \left[ (V_{pp} - V_{pn}) - (V_{hp} - V_{hn}) \right] \]
**Peak Detector Sample&Hold**

- Current I: 30nA, to counter potential upward drift (fundamental for a PD)

I is switched off during ADC
 Comparator

- Very fast: 50ns @ 10mV differential input
  Because node b cannot move far

![Comparator schematic]
ClassAB opamp

- Only capacitive loads. Drives ADC and/or analog output.
- Output stage quiescent current is well controlled, for low power
- Standard cells: not OK:
  - (internal) slew rate too low
  - power too high
• Architecture:
  • Two-step flash
    4 MSB’s first; then 4 LSB’s
  • Two resistive ladders, 16 units each
    ■ coarse ladder low resistive
    ■ fine ladder high resistive
  • Comparators
    ■ CMOS : $V_{os} = 10$ mV (3-sigma)
    ■ $1$ LSB $= 11$ mV
    ■ $\iff$ auto-zeroing necessary
  • 250 K conversions/s
  • 30 mW
Clocked comparator

Auto-zeroing (or correlated double sampling) → Offset < 100μV
Only possible because no continuous operation

Residual offset = VosMain/AAux + DiffClockFeedThrough*AAux/AM
• Measurement results
  - LabVIEW / GPIB setup
  - ADC stand-alone
  - DNL = 0.32 LSB
  - INL = 0.34 LSB
Digital part

• Serial interface, 32 bits
  ○ Control (input)
    ▪ operating modes
    ▪ various controls (e.g. gain)
    ▪ discriminator levels
  ○ Status (output)
    ▪ voting & parity errors
    ▪ some pin settings
  ○ Cascadability (scalability)

• Parallel output (ADC). Latching or none-latching.
• 4 MHz clock, 1500 equivalent gates, VHDL, decoding&control
• To minimize disturbances of the analog
  ▪ event driven (PDFE quite, except some 30 FF’s, until peak latched)
  ▪ I/O: TLL, very long rise & fall times
## Mixed mode simulations / 1

### Table with main functional modes

<table>
<thead>
<tr>
<th>Description</th>
<th>Input signals</th>
<th>power up / signals</th>
<th>to ana</th>
<th>digital set</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coincidence detection mode; anti-coincidence mode; digital out</td>
<td>0 0 0 0 0 1 1 1 1 1 1</td>
<td>0 X 0 E N</td>
<td>0 0 0 0 0 0 1</td>
<td>Default mode 8</td>
</tr>
<tr>
<td>Coincidence detection mode; coincidence mode; digital out</td>
<td>0 0 0 0 0 1 1 1 1 1 1</td>
<td>0 X 0 E N</td>
<td>0 0 0 0 0 0 1</td>
<td>Default mode 1</td>
</tr>
<tr>
<td>Charge amplification mode; anti-coincidence mode; digital out</td>
<td>0 0 0 0 0 1 0 1 1 1 1</td>
<td>0 X 0 E N</td>
<td>0 0 0 0 0 0 1</td>
<td>Default mode 1</td>
</tr>
<tr>
<td>Charge amplification mode; coincidence mode; digital out; coin chan on, isolated</td>
<td>0 0 0 1 0 1 1 1 1 1 1</td>
<td>0 X 0 E N</td>
<td>0 0 0 0 0 0 0</td>
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<td>0 0 0 1 0 1 1 1 1 1 1</td>
<td>0 X 0 E N</td>
<td>0 0 0 0 0 0 1</td>
<td>Charge amplification mode; coincidence mode; digital out</td>
</tr>
<tr>
<td>Quiet mode (everything in power down, except crystal oscillator and part of ADC)</td>
<td>0 0 0 0 1 1 1 1 1 1 1</td>
<td>0 X 1 X X</td>
<td>0 0 0 0 0 0 NA</td>
<td>Default mode 1</td>
</tr>
<tr>
<td>Coincidence detection mode; analog out</td>
<td>0 1 0 1 0 0 1 0 1 0 1 0</td>
<td>0 X 0 X X</td>
<td>0 0 0 0 0 0 NA</td>
<td>Coincidence detection mode; analog out</td>
</tr>
<tr>
<td>Charge amplification mode; analog out</td>
<td>0 1 0 1 0 0 1 0 1 0 1 0</td>
<td>0 X 0 X X</td>
<td>0 0 0 0 0 0 NA</td>
<td>Charge amplification mode; analog out</td>
</tr>
<tr>
<td>Buffer-only mode (AAP bypassed); quasi-quiet mode (as quite mode, but buffer on)</td>
<td>0 1 0 0 1 X X X X X X</td>
<td>0 0 0 0 0 0 NA</td>
<td>0 0 0 0 1 0</td>
<td>Buffer-only mode (AAP bypassed); quasi-quiet mode (as quite mode, but buffer on)</td>
</tr>
<tr>
<td>Test mode: as 00000, but buffer to pin bufOut (to observe PDSH)</td>
<td>1 1 1 0 0 0 0 1 1 1 1 1 1</td>
<td>0 X 0 E N</td>
<td>0 0 0 0 0 0 1</td>
<td>Test mode: as 00000, but buffer to pin bufOut (to observe PDSH)</td>
</tr>
<tr>
<td>Test mode: PDSH and MDAC output direct to EDOout</td>
<td>1 1 1 0 1 X X X X X X</td>
<td>1 0 0 0 0 0 NA</td>
<td>0 0 0 1 1 1</td>
<td>Test mode: PDSH and MDAC output direct to EDOout</td>
</tr>
<tr>
<td>Test mode: as 00110, but MDAC output direct to pin EDOout</td>
<td>1 1 1 0 1 X X X X X X</td>
<td>1 0 0 0 0 0 NA</td>
<td>0 0 0 1 1 1</td>
<td>Test mode: as 00110, but MDAC output direct to pin EDOout</td>
</tr>
<tr>
<td>Test mode: MDAC output direct to PDSH</td>
<td>1 1 1 0 1 X X X X X X</td>
<td>1 0 0 0 0 0 NA</td>
<td>0 0 0 1 1 1</td>
<td>Test mode: MDAC output direct to PDSH</td>
</tr>
<tr>
<td>Test mode: MDAC output direct to EDOout</td>
<td>1 1 1 0 1 X X X X X X</td>
<td>1 0 0 0 0 0 NA</td>
<td>0 0 0 1 1 1</td>
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<td>1 1 1 0 1 X X X X X X</td>
<td>1 0 0 0 0 0 NA</td>
<td>0 0 0 1 1 1</td>
<td>Test mode: MDAC output direct to EDOout</td>
</tr>
<tr>
<td>Test mode: as 00110 (= ADC-only mode), but AAP bypassed</td>
<td>1 1 1 0 1 X X X X X X</td>
<td>1 0 0 0 0 0 NA</td>
<td>0 0 0 1 1 1</td>
<td>Test mode: as 00110 (= ADC-only mode), but AAP bypassed</td>
</tr>
<tr>
<td>Test mode: as 00101, but main channel off, external input to PDSH</td>
<td>1 1 1 0 1 X X X X X X</td>
<td>1 0 0 0 0 0 NA</td>
<td>0 0 0 1 1 1</td>
<td>Test mode: as 00101, but main channel off, external input to PDSH</td>
</tr>
<tr>
<td>Powerdown mode (everything in power down, except crystal oscillator and part of ADC)</td>
<td>0 X X X X X X X X X X X X</td>
<td>0 0 0 0 0 0 NA</td>
<td>0 0 0 0 0 0 NA</td>
<td>Powerdown mode (everything in power down, except crystal oscillator and part of ADC)</td>
</tr>
</tbody>
</table>
Mixed mode simulations / 2

- Chip + external components: simulation schematic
Chip: toplevel design schematic
- Co-simulation: spice - verilog
- Essential for PDFE:
  - Many operating modes
  - Complex interaction analog ↔ digital
    - event driven
    - asynchronous
    - loops
Nonlinearity

Simulation result
All circuits except ADC

Best Straight Line nonlinearity < 0.5 LSB
Errors somewhat proportional with signal
Radiation Hardness

- **Total Dose:** analog and digital part: good up to 12 krad.
  - Parasitic MOS transistor field-oxide leakage: gate-all-round layout for critical NMOS devices (determined by simulation)
  - Gate oxide threshold voltage drift: corner analysis, and assume that no Worst Case wafer (limited volume)

- **Single Event Upsets:** digital part
  - Cell level: foundry library screened for least sensitive cells
  - Rt (register transfer) level:
    - feedback avoided as much as possible (no FSM's)
    - parity bits
    - majority voting for critical registers (EDAC)

- **Single Event Latch-up**
  - Thin epi layer on top of a heavily doped and hence low impedance substrate intrinsically robust for latch-up. Latches up under Cf256.
Edgeless transistor layout

- Significantly increases the total dose immunity
- Applied in the peak detector’s anti-drift current source
• Die size: 31 square mm
- 64 pins Quad Flat Package
- 56 pins used
- VME board
The two inputs close to theasic
**Analog pulses**

- **Analog output mode**
  - Semi-gaussian output pulse
  - Event detector out

- **Digital output mode**
  - Charge input (V-step on Cseries)
  - Peak detector output
  - Event detector out
  - End of A-to-D conversion
Low noise PCB / 1

- Only passive external components
- Battery-powered; faraday cage
Low noise PCB / 2

- Crystal (digital) *not* running
- Noise (detector capacitance)
- With and without crystal running
- Measured with zero input signal
- 1mVrms corresponds to an ENC of 207 electrons

- Crystal (digital) running

![Graphs showing noise measurements](image)
Status & conclusions

- A low power low noise PDFE is realized
- Implements all analog processing up to (& including) the ADC
- Mixed analog digital design
- High re-usability and scalability
- Samples available since 1 year
- Device is fully functional
- Evaluation board allows all kind of settings and measurements
- Low noise board for noise characterization
- Estec is building an instrument for STEREO, using PDFE

- Technical paper available, from the ESCCON 2000 conference
- Datasheet available
Application: NASA's STEREO mission

- Study of solar eruptions
- PDFE to be part of the SEPT experiment (IMPACT instrument)
- Launch: 2004
- http://stprobes.gsfc.nasa.gov/stereo.htm