Active Pixel Sensor CMOS Image Array for Optical Inter-Satellite Links (OISL)

Final Presentation

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Presentation outline

- Introduction
  Project motivation, objective, scope, base line
- Activities
- Technical part
  - Image sensor outline
  - Specifications
  - Test & Measurement
  - Demo system features
- Conclusions

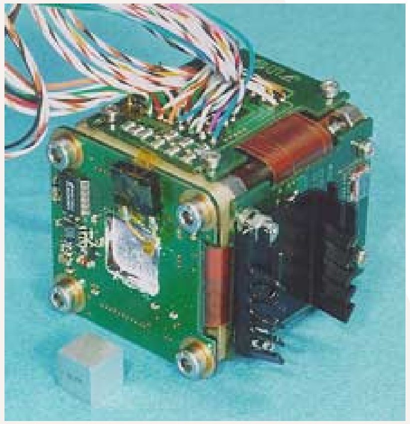
Introduction

Project motivation:

- The growing market of satellite telecom constellations (early 2000) asked for a cost-effective beam-tracking device that could withstand the radiation load encountered in low orbit.
- APS can offer benefits in terms of system-level cost-effectiveness, weight and volume.
- Start from the experience gained with ASCoSS design

Introduction

Attitude Sensor Concepts for Small Satellites (ASCoSS)



Co-operation with SIRA electro-optics, Contraves and IMT (1997-1999)

Project objective:

Design a star tracker using novel technologies
APS, MCM, Diffractive optics, …

- » FOV 20° x 20°
- » Update rate 10Hz
- » NEA 1arc minute (2σ)
- » Dim star limit: 5 m_v

Image sensor properties:

- » 512 by 512 format , 25 μm pitch CMOS Active Pixel Sensor (APS)
- » ALCATEL Micro-Electronics 0.7 Analogue CMOS process
- » Patented N-well pixel structure results in high fill factor
- » On-chip 8-bit ADC

Introduction

ASCoSS:

Corrigible items

- Design flaws in output amplifier
- Ghost image due to cross-talk
- Low MTF due to epi-layer thickness
- Pixel-to pixel non-uniformity
- Low radiation tolerance

Conclusion of SIRA:

"The overall conclusion is that a sensor has been designed and breadboarded which could meet the target specification."

- Positive: noise behavior
- Precludes: low MTF, non-uniformity requires on-flight calibration, poor radiation tolerance.

Introduction

Objective:

Design a next-generation CMOS Active Pixel image Sensor (APS), capable of tracking a laser beam beacon in Low Earth Orbit.

- Start from ASCoSS specifications:
  - » Format: 512 by 512, 25 µm pixel pitch
  - » Equal or better noise performance
- Enhancements over ASCoSS:
  - » Enhanced radiation tolerance
  - » Enhanced ADC resolution
  - » Improved MTF
  - » Improved Infra-red response
  - » Addressable shift registers

Envisage broader field of applications:

- Low- to medium accuracy star tracking
- Sun sensing

Introduction

Scope

- Design and fabrication of the image sensor
- Electro-optical and limited radiation tolerance evaluation
- Delivery of a limited number of samples
- Construction and delivery of evaluation system

Not included:

Complete qualification testing :

environmental, life time, extended radiation testing, …

Introduction

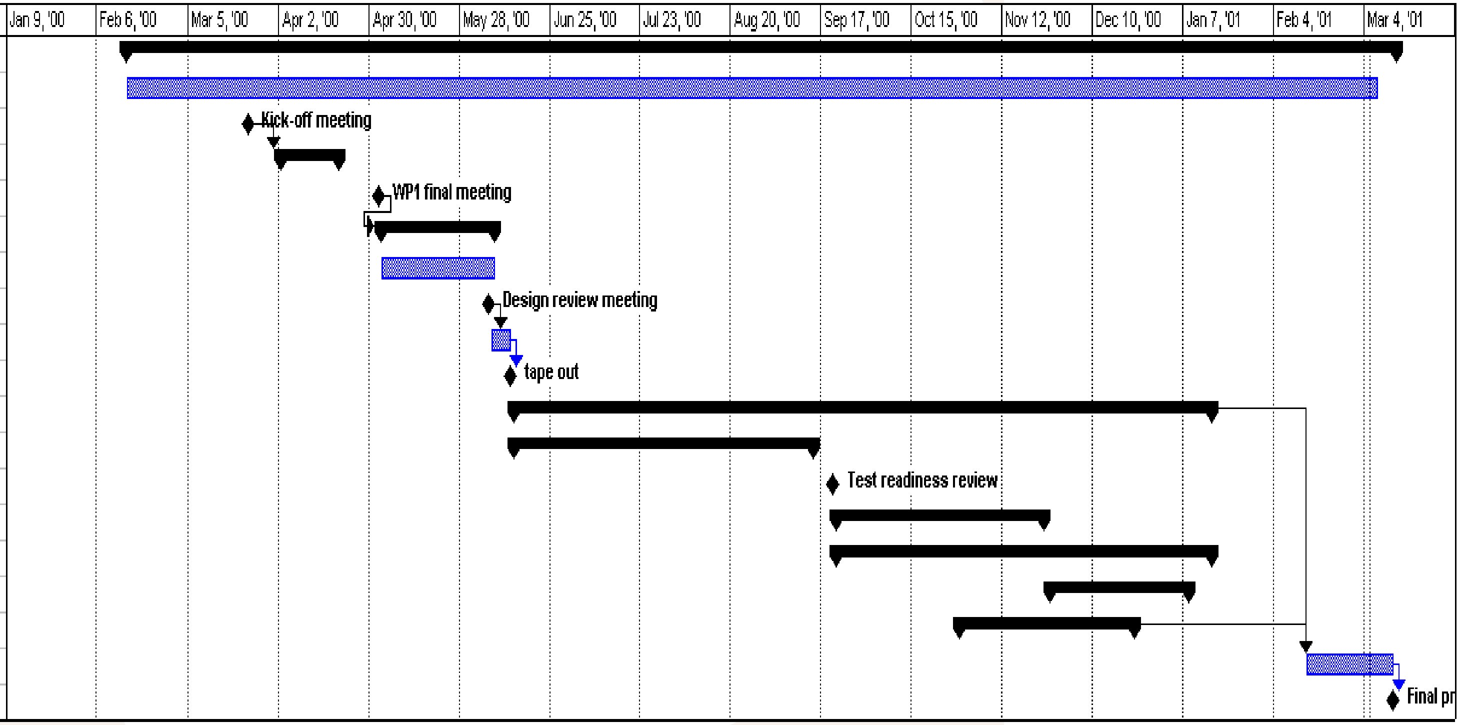
Design base line:

- CMOS Active Pixel Sensor (APS) with 4 diodes per pixel
- Format 512 by 512 pixels
- On-chip Fixed Pattern Noise (FPN) correction
- Programmable gain output amplifier
- 10-bit ADC
- Programmable windowing
- Radiation tolerant design technique (first time !)

Activities

Study logic, project timing

ID	Task Name
1	**OISL development**
2	WP0: general project management (IMEC)
3	Kick-off meeting
4	**WP1: Conceptual design (FF)**
6	WP1 final meeting
7	**WP2: Detailed design (FF)**
8	Detailed design
9	Design review meeting
10	Post layout design review at ESA
11	tape out
12	**WP3: Production**
13	**WP 3.1: Fabrication (FF)**
26	Test readiness review
27	**WP 3.2: Electro-optical evaluation (FF)**
30	**WP 3.3: Radiation test (IMEC)**
41	**WP 3.4: Delivery of 40 samples (FF)**
45	**WP4: Demonstration system (IMEC)**
53	Final documentation
54	Final project meeting



Activities

Design activities:

Preliminary design (WP1):

- Architectural design: first-cut specification targets and floorplan
- Simulations of pixels, shift registers, output amplifier
- Design of pixel, shift register cell, ADC basic cell
- Selection of foundry

Detailed design (WP2):

- Full custom IC layout with Cadence Virtuoso layout editor
- Drawing of about 100 basic unit cells
- Hierarchical design, based on parametric cells
- Start from scratch (first radiation tolerant design)

Activities

Production and testing (WP3):

- Production at ALCATEL Micro-Electronics (WP 3.1)
- Electro-optical evaluation (WP 3.2)
  - Confirmation of design target specifications
  - Spectral response, photo response, MTF, noise, dark current , …
- Radiation testing (WP 3.3)
  - Only total dose test up to 230 Krad (device can probably sustain much higher levels)
- Delivery of 40 samples to the agency (WP3.4)
  - Functional testing of all produced devices on wafer
  - Packaging and re-testing selected devices for delivery
- Construction of demo system (WP 3.5)

Technical part

Outline

- Image sensor description
- Specifications
- Test & Measurement
- Packaging
- Demo system

Image sensor description

Features

- Integrating APS in 0.5 µm CMOS technology
- 512 by 512 pixels on 25 µm pitch
- 4 diodes per pixel for improved MTF and PRNU
- Radiation tolerant design
- On-chip double sampling circuit to cancel Fixed Pattern Noise
- Electronic shutter capability
- Readout rate: up to 30 full frames per second
- Fast windowing through pre-settable start point of read-out
- On-chip 10-bit ADC
- Ceramic JLCC-84 package

Image sensor description

Image sensor outline

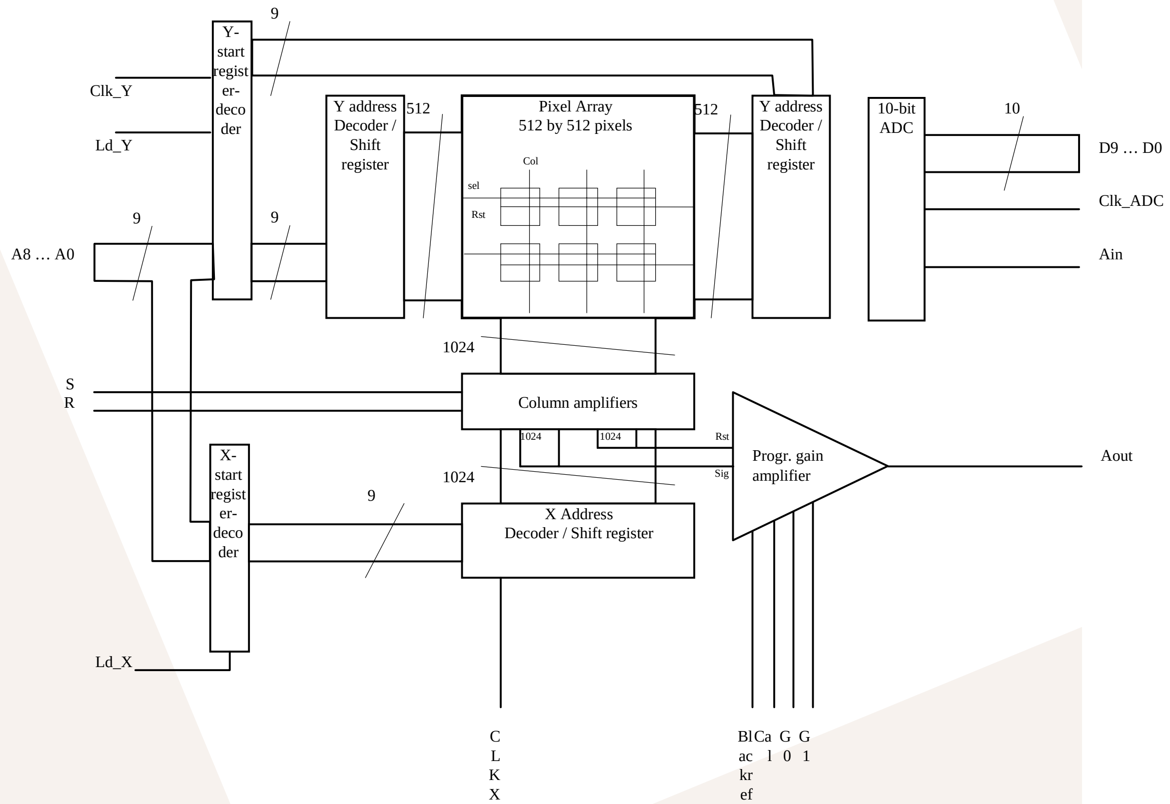


Image sensor description

Lay-out view

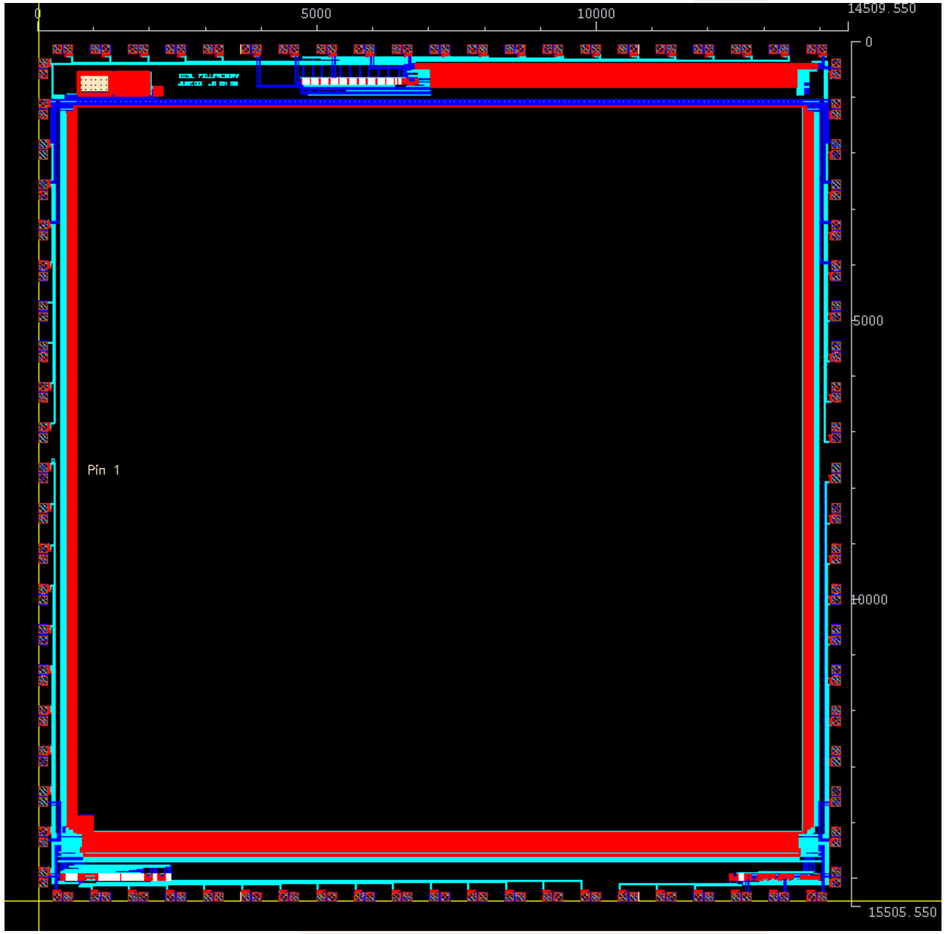


Image sensor description

Pixel design

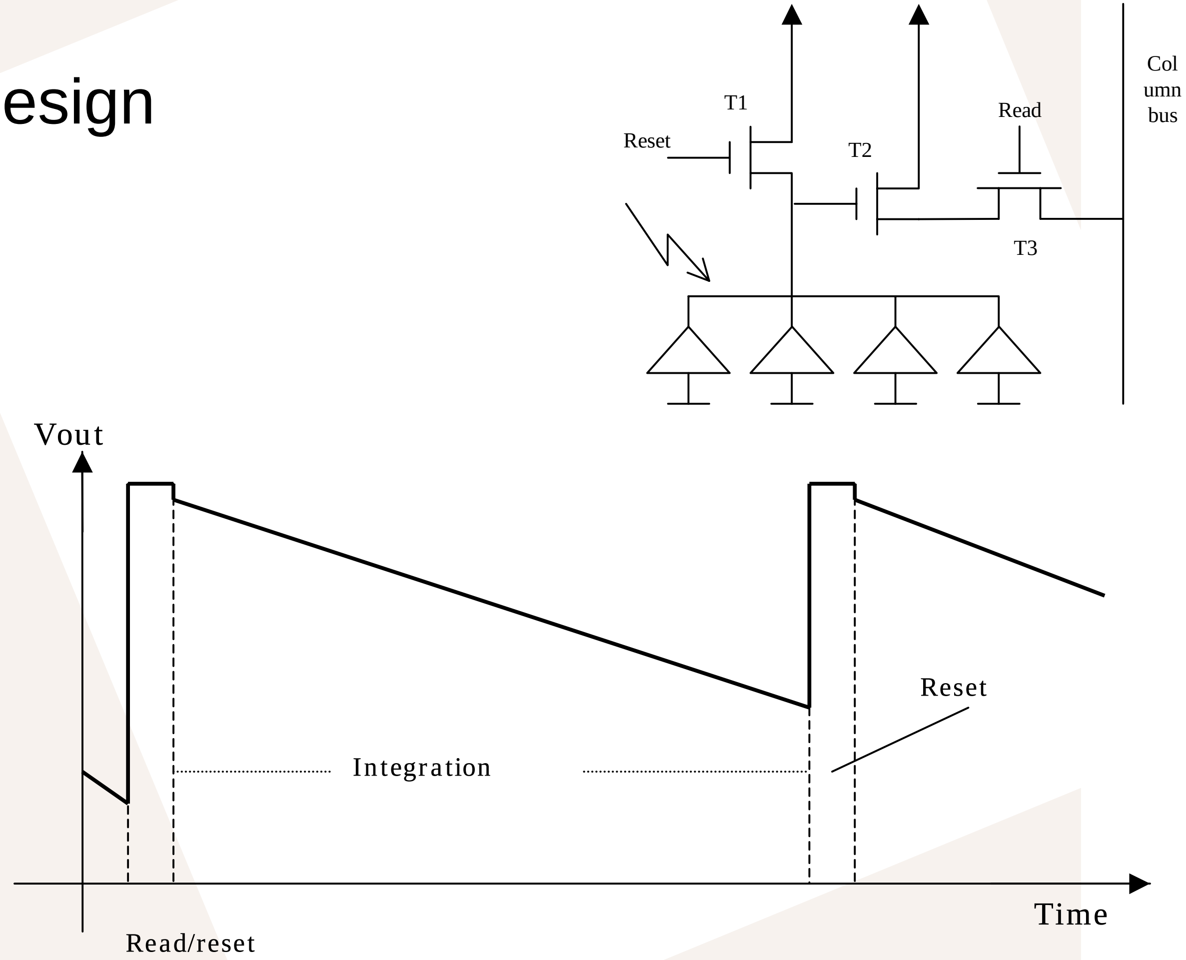
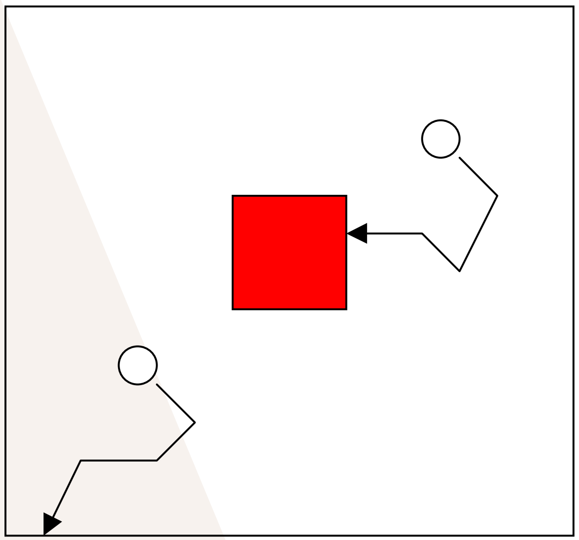


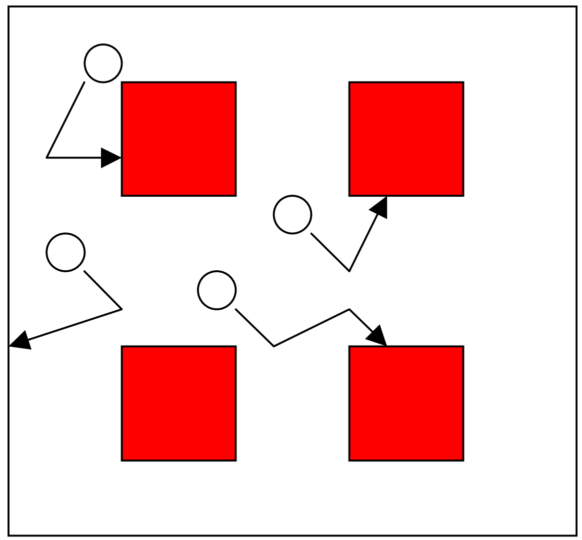
Image sensor description

Pixel design

4 photodiodes



4 photodiodes



Charges can diffuse to neighboring pixels

Cross talk : 20%

MTF: 0.27

Almost all charges will be collected within the pixel

Cross talk : 8%

MTF: 0.4

Image sensor description

Image sensor description

Column amplifiers

Optimization (compared to ASCOSS):

- Less sensitivity to Vth variations (radiation!)
- Better fixed pattern noise
- Less power dissipation
- Simpler timing diagram

Output amplifier

Designed for 12.5 MHz & 40 pF load

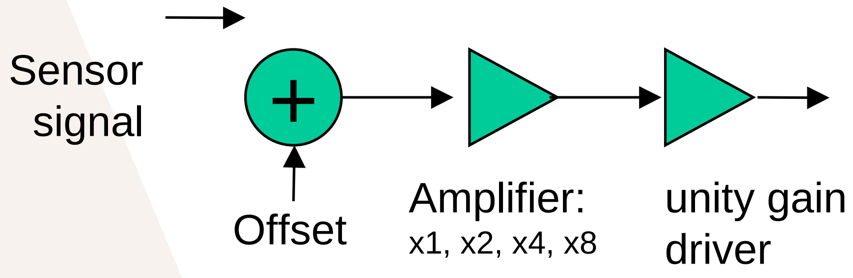


Image sensor description

ADC

- 12.5 Msamples/s
- 10 bit ADC
- Radiation-soft version used on ibis 4 & ...
- Radiation tolerant layout
  - Size has increased slightly due to radiation tolerant design

Image sensor description

Fabrication

Fabrication at ALCATEL Micro-Electronics as prototype run

- 2 wafers + 2 wafers for digital sun sensor project
- 54 devices per wafer

Process:

- Alcatel Microelectronics 0.5 µm analogue-signal CMOS, 5 µm epi-layer
- Analogue cores: full-custom, manual layout
- I/O pads and power pads: manual layout

Electro-optical specifications

Parameter	Specification
Spectral range	400 – 1000 nm
Quantum Efficiency x Fill Factor	Max. 35%
Full Well capacity	311K electrons
Linear range within ± 1%	128K electrons
Output signal swing	1.68 V
Conversion gain	5.7 µV/e-
kTC noise	76 e-
Dynamic Range	74 dB (5000:1)
Fixed Pattern Noise	1σ < 0.1% of full well
Photo Response Non-uniformity at Qsat/2	Local: 1σ < 0.39% of signal Global: 1σ < 1.3% of signal
Average dark current signal	4750 e- / s
MTF	Horizontal: 0.36 Vertical: 0.39
Anti-blooming capacity	x 1000 to x 100 000
ADC	10 bit
ADC linearity	± 3.5 counts
Missing codes	none
ADC setup time	310 ns to error <1% (large signal)
ADC delay time	125 ns
Power Dissipation	< 350 mW

Test & Measurement

Outline

- Packaging, operation and bias conditions
- Electro-optical evaluation
- Radiation testing
- Functional testing of delivery samples

Test & Measurement

Packaging, Operation and Bias conditions

- Package devices from one wafer in 84 pin J-lead with glass cover
- Operate one device in test system
- Establish bias conditions: voltage and timing, resulting in datasheet
- Verify bias conditions on 5 devices

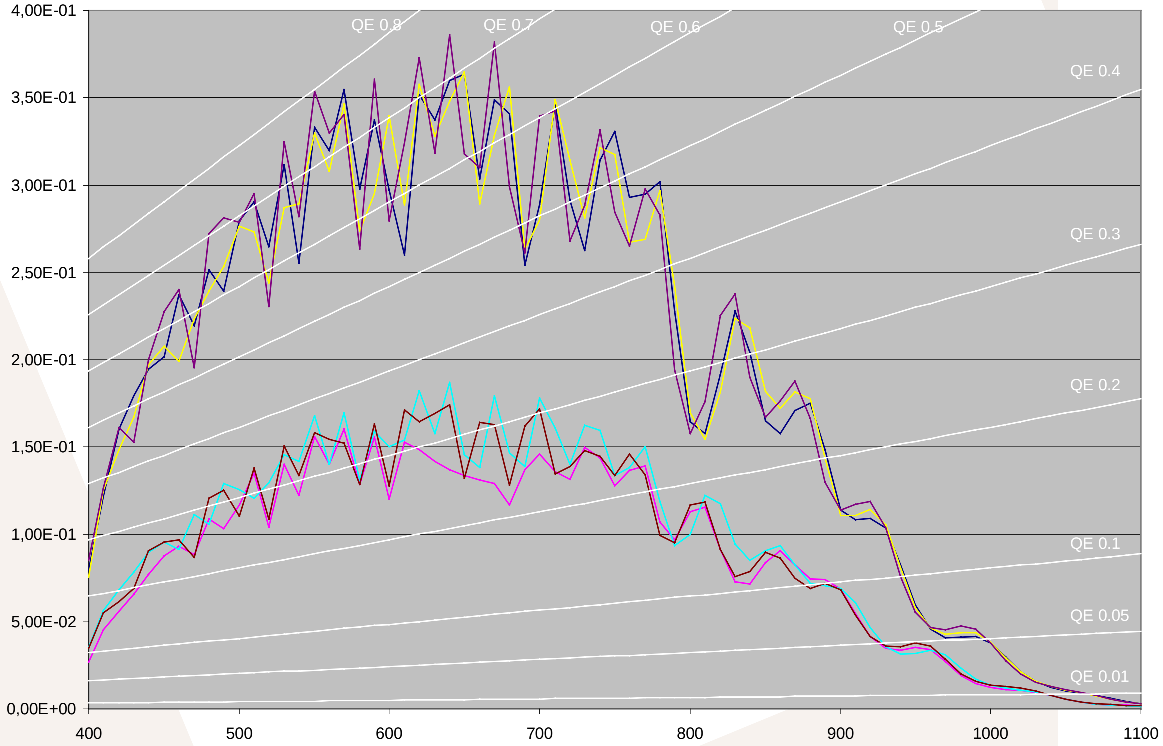
Test & Measurement

Electro-optical evaluation: overview

Measurement	Test sample
Spectral response	On test structure on 3 samples
Photo-voltaic response	On 3 pixel on 3 devices each at different gain settings
Pixel profile	On 3 pixel on 3 devices in both horizontal and vertical direction
Dark current	On 5 pixels on 5 devices
FPN	On 50% of the pixels of 5 devices
PRNU	On 50% of the pixels of 5 devices
Noise	On 5 pixels on 5 devices
Power	On 5 devices
Output amplifier DC response	On 3 devices
Output amplifier gain/phase diagram	On 3 devices
ADC minimum set-up time	On 3 devices
ADC missing codes	On 3 devices
ADC linearity	On 3 devices

Test & Measurement

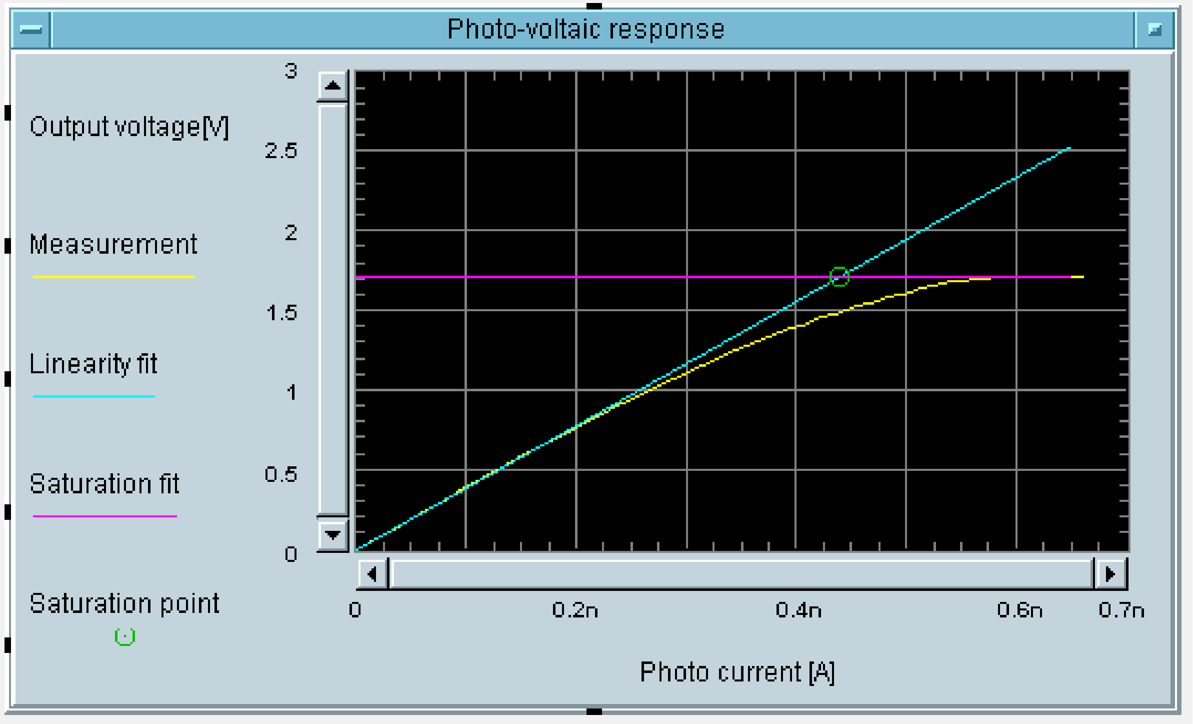
Spectral response and quantum efficiency



Test & Measurement

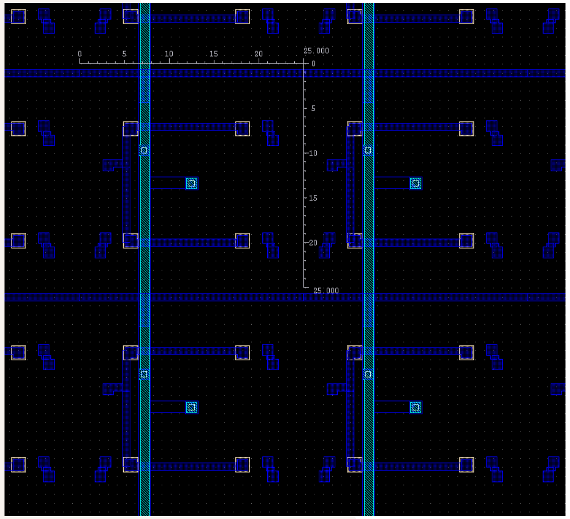
Photo-voltaic response

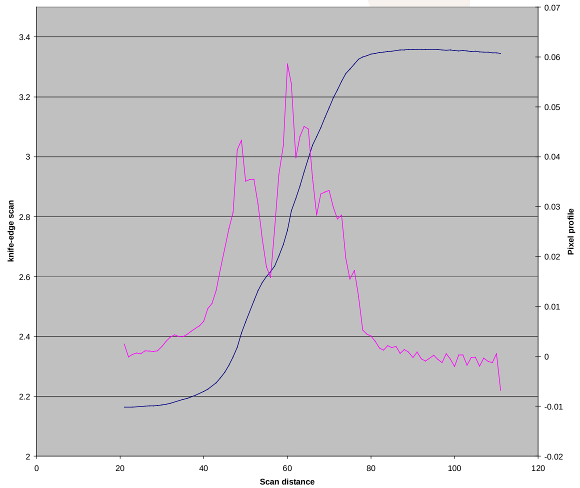
Allows to calculate saturation charge, linear region and conversion factor.



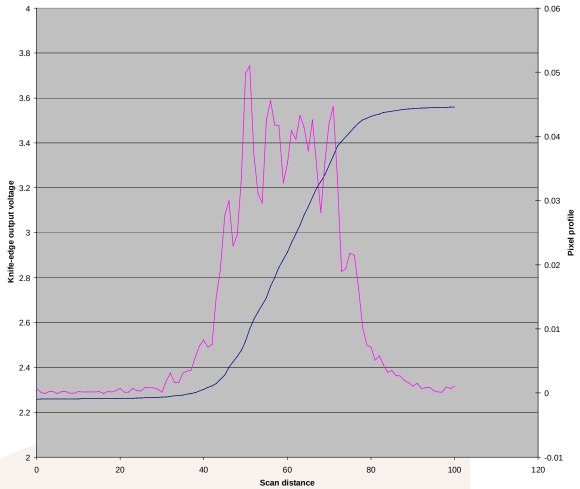
Test & Measurement

Pixel profile





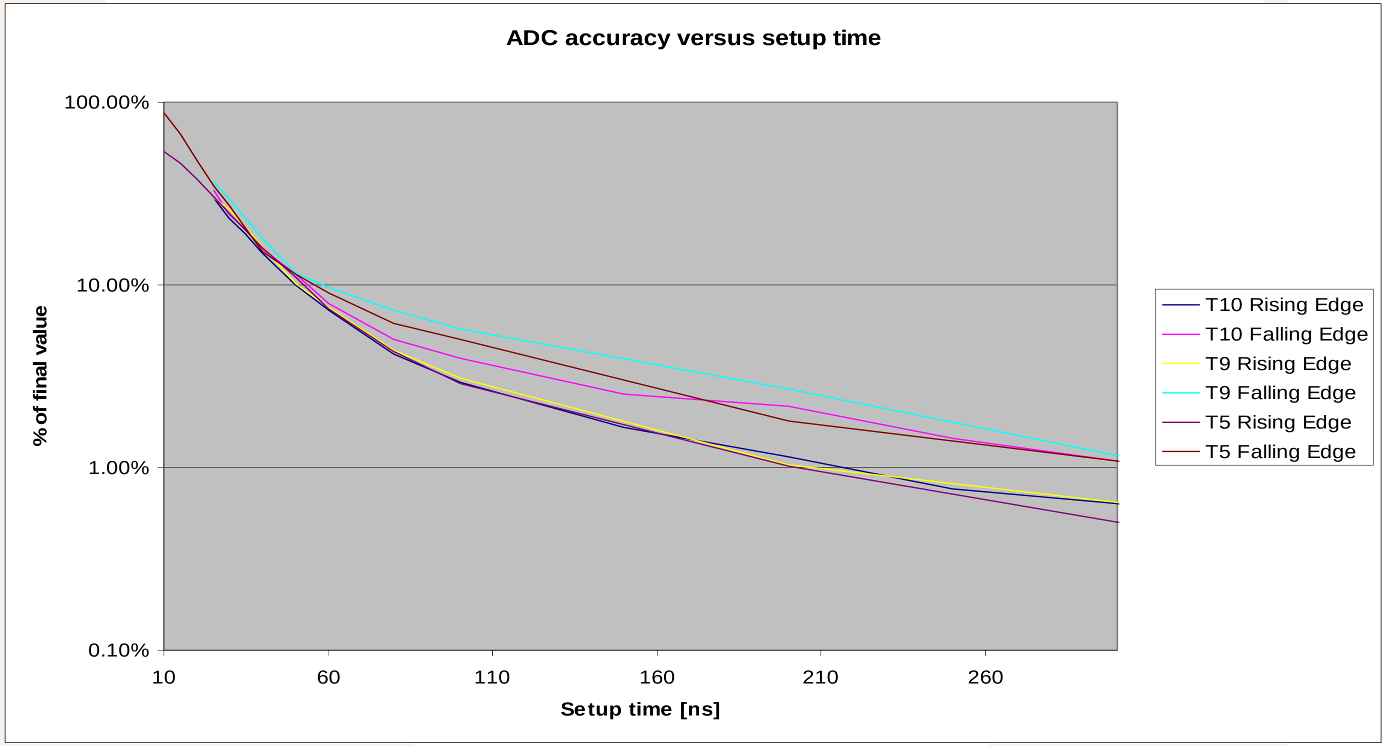
Horizontal



Vertical

Test & Measurement

ADC set up time



Test & Measurement

Radiation testing

Pre- and post- irradiation tests:

- Functional test
- Power consumption: functional and under DC bias
- Dark current on 5 pixels
- Fixed Pattern Noise (FPN) on 50% central area
- Photo Response Non Uniformity (PRNU) on 50% central area

Total dose irradiation (CO 60) of 10 samples with varying dose

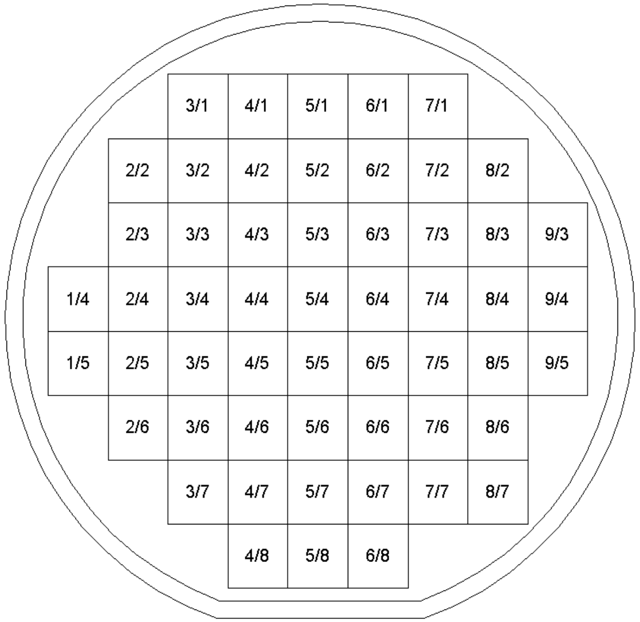
- Total dose: 230 Krad
- Dose rate: 5 Krad/hr
- DC bias, no clocking

Approximate insertion time	**Sample ID**	**Total dose**
T0	S1, S2	230 Krad
T0 + 24 hr.	S3, S4	110 Krad
T0 + 38 hr	S5, S6	40 Krad
T0 + 42 hr	S7, S8	20 Krad
T0 + 44 hr	S9, S10	10 Krad
T0 + 46 hr	End of irradiation	

Test & Measurement

Functional testing on wafer

- High yield: 50% of the devices have less than 10 isolated defect pixels.
- Functional test on wafer:
  - At 50% uniform illumination
  - Power consumption
  - Average gray value and standard deviation
  - Number of bad pixels (bright/dark)
  - Number of bad pixels with bad neighbor (bright/dark)
  - Number of bad columns/rows based upon average column/row value and u standard deviation
- Select 40 best devices
- Packaging in 84 J-lead package with glass window
- Visual inspection of images from packaged devices at 50% uniform illumination

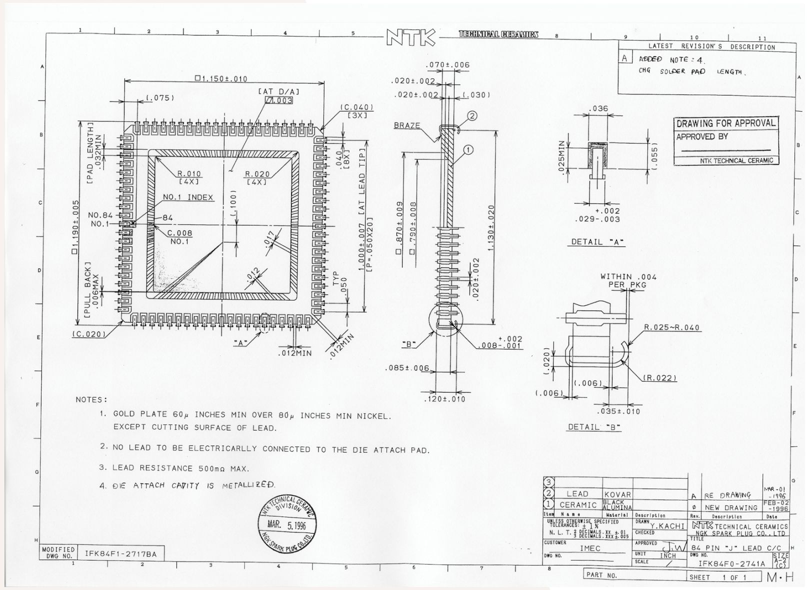


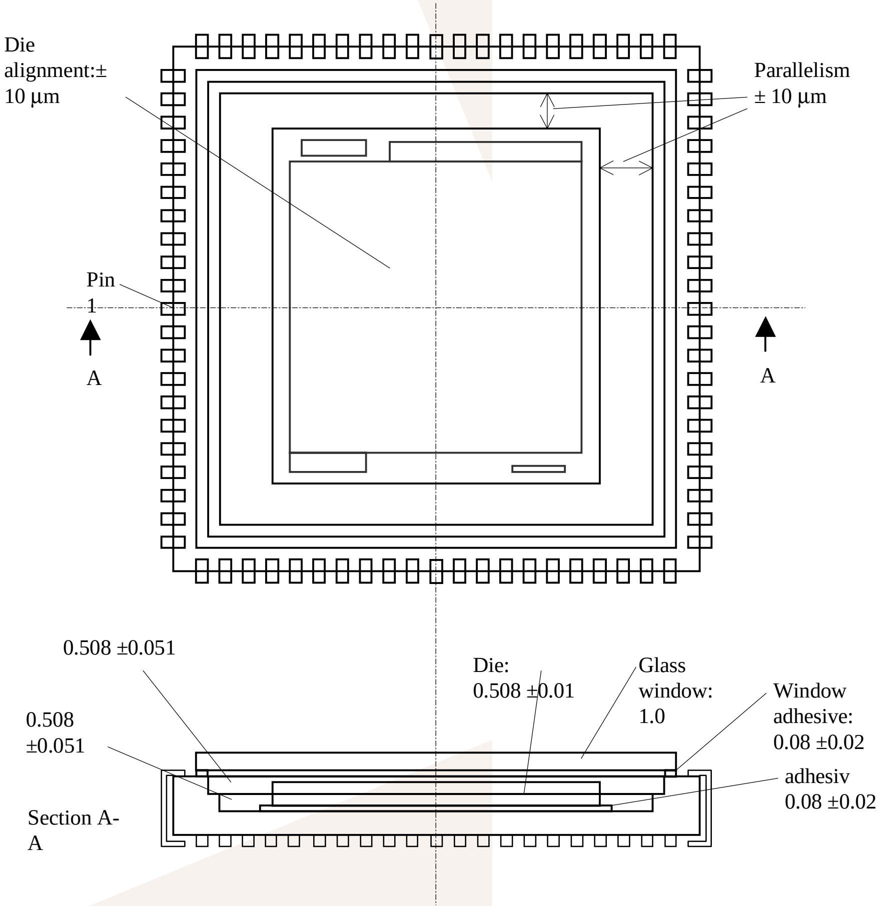
Packaging

84-J-leaded package

- Ceramic package (black alumina), gold leads
- Custom designed for Fillfactory to contain large-area image sensors

Position of die in package within known tolerances





Drawing not to scale

Demo system

Main demo system features:

- Apply power, logic signals and DC bias to OISL image sensor for proper read-out at nominal or at reduced speed
- Control sensor properties:
  - Integration time (setting by line or by frame)
  - Windowing
  - Gain setting
- Capture one frame in memory buffer at nominal read-out speed
- Transfer image to PC via printer port and display on PC screen
- Store image in different file formats:
  - nip (16 bit), PGM, BMP, tab-separated text

Continuation

Other projects, based upon OISL were started:

Application in ISLFE breadboard

- Breadboard for optical link
- SIRA Electro-optics and Contraves

Low cost digital sun sensor

- Funded By ESA
- 2 consortia:
  - » TNO-TPD, Sodern, Fillfactory: use OISL sensor as is
  - » Officine Galileo: 1024 x 1024 format, 1 diode pixel (15 µm)

Atmospheric Chemistry Experiment (ACE)

- Canadian Space Agency, ABB Bomem (Quebec)
- Sensor development funded by the Belgian government through Prodex
- 256 x 256, 4-diode pixel (25 µm), with black reference pixels
- Flight qualification, launch: July 2002

Interest from industry

- Large pixel format
- Large area
- High uniformity

Conclusions

OISL is the first complete image sensor that was designed with the novel radiation-tolerant design technique.

The design was successful: the device is operational and meets all predicted specifications except ADC speed.

Design target	Comment
512 by 512, 25 μm pixel pitch	By design
Equal or better noise performance	Better noise performance through better amplifier design
Enhanced radiation tolerance	Novel design technique successfully applied
Enhanced ADC resolution	10 bit, radiation tolerant
Improved MTF	4-diode pixel has very high MTF
Improved Infra-red response	Not improved over ASCoSS, but uncommitted
Windowing	Successful implementation of addressable shift registers

Demo

Demo