ESA 13345 : Building Blocks for System on a chip contract
ESA 13345/#1 : Design of a VME Interface (EVI32)
Final Presentation

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THE OBJECTIVES OF EVI32 CONTRACT

Contract history

- **EVI32 was developed in the frame of ESA 13345 contract called “Building Blocks for System on a Chip”.**

- **ESA 13345 contract is managed by Sandi Habinc at ESTEC. It includes :**
  - **#1 : development and Industrialization of an ERC32 VMEbus Interface Device**
  - **#2 : Initial Analysis of the Development of a System-On-a-Chip device**
  - **#3 : Development of a System-On-a-Chip device**

- **It was initially foreseen to use a VME interface within System-On-a-Chip but this interface has been replaced by a PCI interface. Thus only the design of a packaged component remains from the initial project.**

Management objective of the study

- Design and manufacture a first-time-right radiation tolerant ERC32 VMEbus Interface for on-board application
- Ensure that the device is unrestrictedly available from the design house to European industry at fair and reasonable pricing
- Ensure that the manufacturing foundry makes available and supports the developed EVI32 device as an ASSP with a comprehensive data sheet
- Preferably use a European technology for foundry, with a process having been approved or being considered for ESA/SCC Capability Approval
- EVI32 shall be based on the VHDL code provided by ESA
- ESA shall have full ownership of the updated VHDL code
- No validation of EVI32 at board level is performed in this study.

Technical objective of the study

- EVI32 shall fully adhere to IEEE 1014-1987 VMEbus standard
  - A32/A24/D32/D16/D8 master interface;
  - A24/D32/D16/D8 slave interface;
  - Interrupt handler;
  - Interrupter;
  - Single level arbiter (SGL);
  - VME bus timer;
  - Optimised D16 interface;
  - Four mailboxes for multi-processor communication;
  - On-chip error-detection.
- EVI32 shall be made compatible with :
  - ATMEL ERC32 3 chip microprocessor (TSC691E, TSC692E, TSC693E)
  - ATMEL ERC32 single chip microprocessor (TSC695E)
  - ATMEL 21020 DSP (TSC21020E)
- Radiation Tolerance shall be greater that 50 krads TD with a good immunity to SEU

BRIEF DESCRIPTION OF EVI32

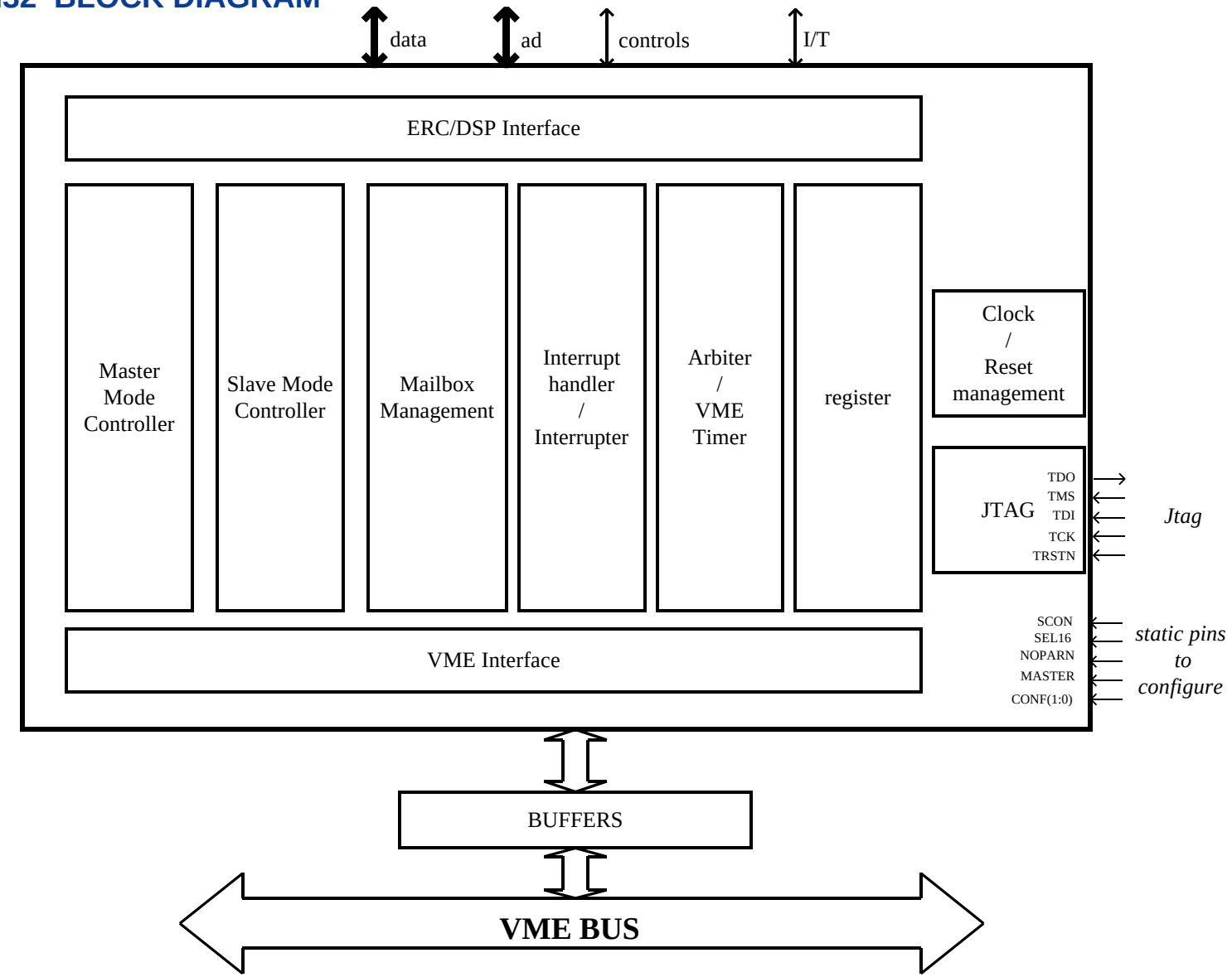
Technical solutions for process/matrix

- MG2RTP process of ATMEL was selected
- MG2RTP-142 matrix used - MQFPF 256 package
  - 23138 gates used for 122128 available gates = 16.28 %
  - 256 pin used for 256 available pins
  - 224 signals, 4 power pins for core, 28 power pins for buffers

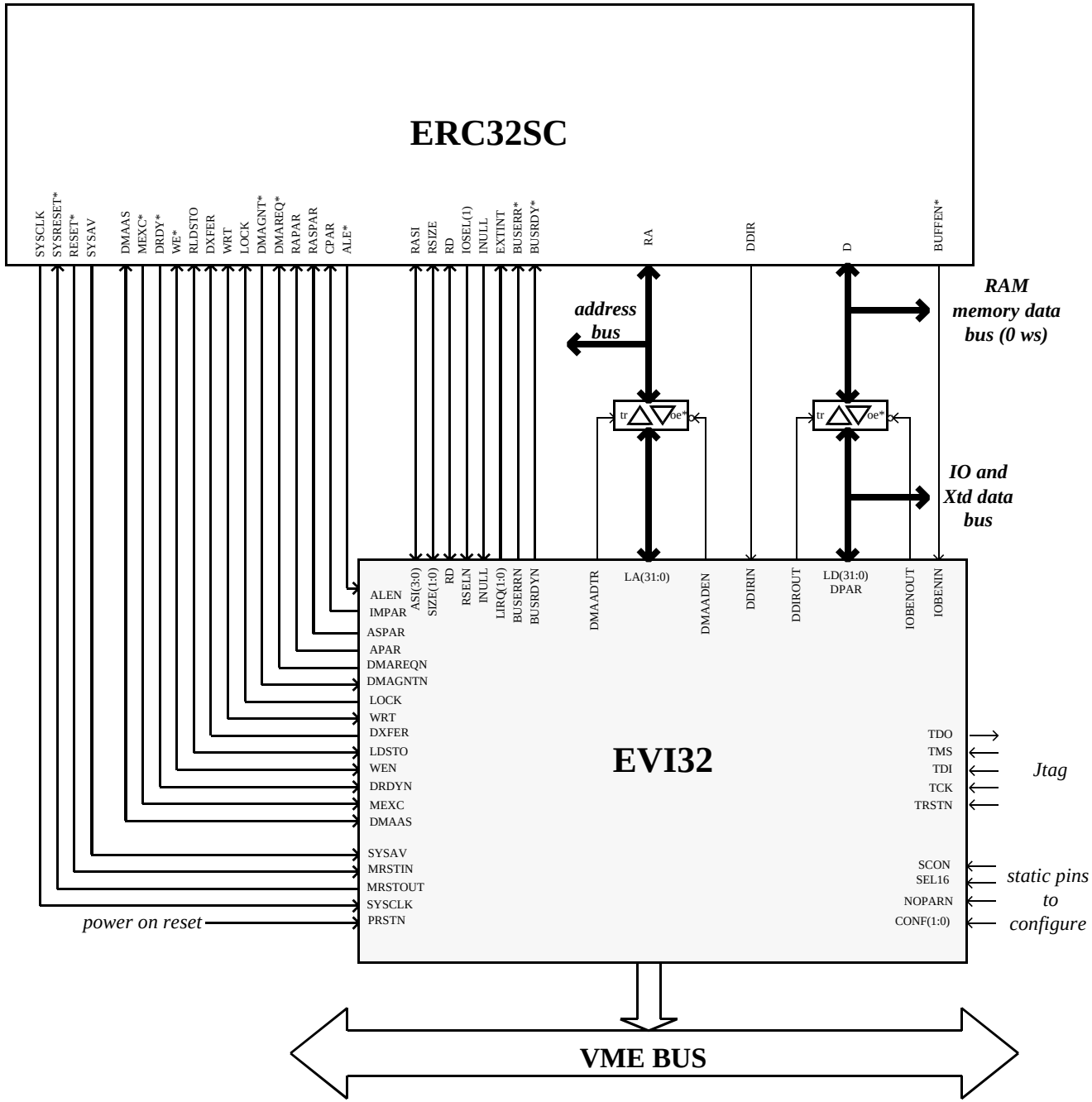
- All the functional D flip-flop are HDFF “SEU hardened D flip-flop”
- Total Dose tolerance of EVI32 is over 100 krads and SEU immunity very high

- No scan used, functional vectors + random vectors allows a fault coverage over 100 %.
- JTAG Boundary Scan is implemented for board level testing

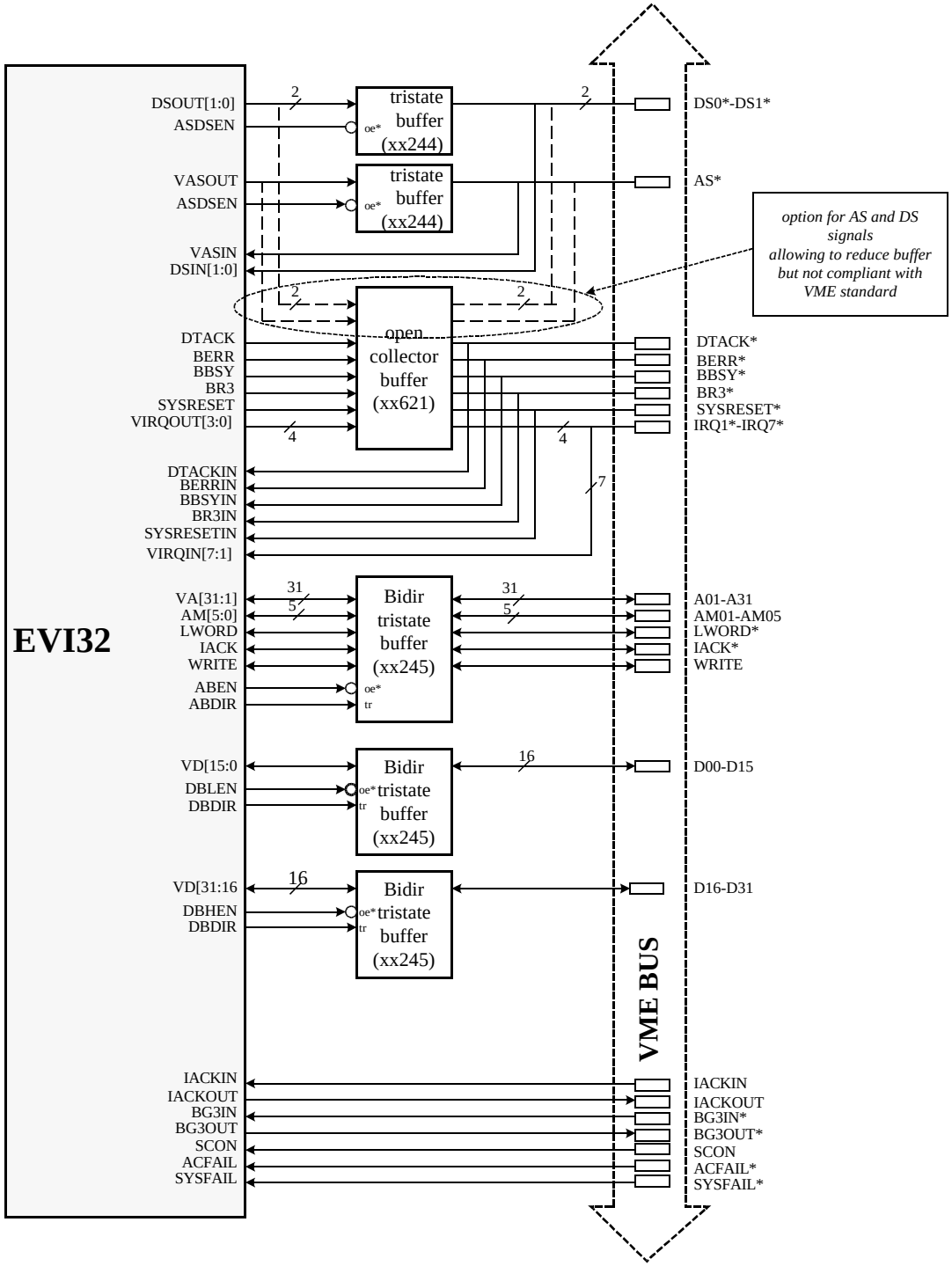
EVI32 BLOCK DIAGRAM



EVI32 ERC SC INTERFACE



EVI32 VME INTERFACE



DSP Interface

- EVI32 can interface TSC21020 DSP
- DSP concept does not fit very well with VME :
  - Byte or 16 bit accesses are not implemented in DSP
  - Data bus are 40 bit or 48 bit wide
  - Address bus are only 25 bit wide for data and 20 bit wide for address
  - Instructions and data paths are separated
- Limitations to VME interface have been performed in DSP mode :
  - In A32 and A24 addressing modes MSB bits are generated by EVI registers
  - D8 and D16 accesses are controlled by decoding DMA[|21:19] and IOSEL_N
  - Master accesses are mapped in DSP Data Space
  - Slave accesses are mapped in Program Data Space

EVI32 timing performances

- in ERC32 3C mode, EVI32 speed is limited only by the speed of the uP (about 15 MHz)

- in ERC32 3C mode :
  - in master mode EVI32 runs at 25 MHz
  - in slave mode EVI32 runs at about 20 MHz. Critical paths comes from the DMAAS signal that has the following characteristics :
  - Setup time min 12 ns – setup time max ½ SYSCLK Period

- in DSP mode EVI32 runs at 15 MHz.

EVI32 DEVELOPMENT SPECIFICITIES

EVI32 development specificities

- EVI32 development was based on ESA provided VHDL core
- EVI32 development method based on ESA requirement, but modified to take into account that the core of the development was not performed by Astrium.

Obviously this is not a recommended design flow

=> Astrium put a large effort on model verification

EVI32 Verification of the model

- An analysis of the code provided was done
  - By reading the VHDL model
  - By running checkers (as DC compiler, Prime Time, Star) on the synthetized netlist to analyze paths between IO and registers, between IO and IO, and between registers, or design rule violations
- Comments were asked to ESA concerning specification and coding of EVI32
- A writing of the Architectural report from the VHDL code was made
- Improvement of the model was made concerning VHDL coding rules, and then modification of the model done.

EVI32 Verification by Simulation (I)

- A test plan was derived from EVI32 specification, VME standard, and previous FPGA developed by ASTRIUM.
- A very large number of case has to be taken into account for the 3 configurations :
  - EVI32 master / slave
  - A32/A24/D32/D16/D8 type of exchange
  - Block transfer activated/or not
  - D16 interface activated / not
  - EVI32 interrupter / interrupt handler
  - EVI32 Arbiter / not
  - EVI32 in charge of VME timer function/ or not
  - EVI32 in slot1 , intermediate slot , end slot
  - plus error cases : non-response...

EVI32 Verification by Simulation (II)

- For each of the 3 configurations (ERC 3C, ERC SC, DSP) EVI32 was simulated with accurate models of the processors :
  - ERC32 3 chip VHDL RTL model
  - ERC32 SC gate level model with its associated SDF file
  - TSC21020 gate level model and DPC companion ASIC VHDL model
- a VME checker written in VHDL and issued from our previous FPGA allows to check violations of the VME standard on the bus
- a VME spy written in VHDL allow to monitor trafic on the bus during simulations
- a VME remote slave written in VHDL is used to dialog with EVI32 in master mode
- a VME remote master written in VHDL is used to dialog with EVI32 in slave mode

EVI32 Verification by Simulation (III)

- 3 different configurations for ERC were coded in VHDL (in addition to ESA provided testbench) :
- Conf M :
  - Slot 1 : ERC 3C or SC, RAM, ROM… + EVI32 acting mainly as master
  - Slot2 : VHDL remote slave
  - VME bus : VME checker, VME spy
- Conf S :
  - Slot 1 : ERC 3C or SC, RAM, ROM… + EVI32 acting mainly as slave
  - Slot2 : VHDL remote master
  - VME bus : VME checker, VME spy
- Conf 4EVI : test of IACK and Arbitration daisy chains
  - - Slot 1 : ERC 3C, RAM, ROM, + EVI32
  - - Slot 2 : ERC 3C, RAM, ROM, + EVI32
  - - Slot 3 : ERC 3C, RAM, ROM, + EVI32
  - - Slot 4 : ERC 3C, RAM, ROM, + EVI32

EVI32 Verification by Simulation (IV)

- About 12 complex sequences have been coded to test each mode. Each sequence is composed of an Assembly program for ERC32 (or a C program for DSP) and in case of slave test of a command file for the remote master.

- Testbench includes auto-check functions that verifies automatically most of the functionality of EVI32

- Modelsim VHDL coverage tool was used to ensure that 100% of the model instructions are tested

EVI32 simulation with ERC32 SC model

- Thanks to ATMEL Nantes a model of ERC32 SC has been delivered to Astrium to allow simulation. This model is a gate level model associated with its SDF file. It is compiled with a -nodebug option for Modelsim.
- ERC32SC model is very accurate, but long to simulate. Internal registers of EVI32 cannot be viewed during simulation.
- ERC32SC model generate a continuous flow of messages related to internal violations in the model. These messages have to be filtered before checking Modelsim outputs.
- EVI32 functionality was first debugged with ERC32 3C model, and then tested with ERC32 SC model in order to save time

EVI32 DELIVERABLE STATUS

EVI32 board simulation model

- Timing have been added to EVI32 model following ESA recommendation
- EVI32 board level model has the same functionality as the component (except JTAG that is not included in the VHDL model), but has a limited accuracy in terms of timing
- A board level model of EVI32 is available upon request from ESA
- Warning : ERC32 SC model is delivered by ATMEL under specific conditions

EVI32 delivery schedule

- Delivery of prototypes planned for week 10
- Delivery of 5 EM planned in week 18
- Draft data sheet available from Astrium, will be put into ATMEL format
- Model available from ESA

Conclusion

- **EVI32 is manufactured, and will be available from ATMEL-WM**
- **EVI32 validation at board level has still to be made**

- **EVI32 study put in evidence the difficulty to base a space ASIC design on a code that has not been designed by the company.**
- **The ASIC methodology has to be modified and focused on verification :**
  - Specification review
  - VHDL code analysis : by reading , with CAD tools
  - Extraction of the Architecture from the VHDL code and analysis
  - Generation of a simulation plan
  - Simulation , code coverage
  - Etc…