32 bit Embedded Real-time computing Core
Single Chip Development
(ERC32SC/TSC695)

Contract 12598/FM (SC)

T. Corbiere, J. Tellier, C. LeGargasson, B. Mouchel, S. Vandepeute, ATMEL WM, France
A. Pouponnot, J. Gailser, ESTEC, Netherlands
ERC32 Single Chip development

Agenda

- Objectives of the contract
- Tentative specification
- Added / Removed functionality
- Electrical characterization
- Radiation test results
- Evaluation Board
- On Chip Debugger
- Part numbering
- Conclusions
- References
Program objectives

- 18 months overall program
- Monolithic version of the existing ERC32 chip set
- Identical set of net-lists with minimum changes
- Upward software functionality
- Improved functionality, speed, radiation hardness, “user friendly”
- 5V and 3V tolerant functionality
- Basic “foundry” functional validation
New Features

• General Purpose Interface (µcontr. Functions)
  ✓ 8-bit parallel I/O port bit per bit configurable
  ✓ Edge detection on GPI inputs => External interrupt

• FLASH compatibility

• Selectable NMI or Watchdog

• High Drive Capability
  ✓ Up to 400 pF for Address buffers
  ✓ Address latches included
  ✓ Up to 150 pF for Data, Controls & Clock buffers

• On-Chip Debugger for J TAG Emulator with
  Read/Write access for all Registers and I/Os
No longer supported

- Master/checker mode *(Never used by customers)*
- Program flow control *(Not supported by compilers)*
- 601/602 modes *(Internal parities always checking)*
- Coprocessor capability *(Never used, embedded processor)*
ERC32 Single Chip development

Atmel Wireless & Microcontrollers

ESTEC, Noordwijk, The Netherlands

Final Presentation days, March 6-7, 2001

Typical Application

TSC695

Mandatory

Boot PROM

Xtd PROM

Xchg Mem

Xtd RAM

I/O 0
to
I/O 3

Xtd I/O

Xtd general

Optional

Mandatory

RAM Memory

(0 ws)

User Application

Mandatory
# Contractual specification

<table>
<thead>
<tr>
<th>Power supply (V)</th>
<th>Speed (MHz)</th>
<th>MIPS</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Committed</strong></td>
<td>5.00 ± 10%</td>
<td>20</td>
<td>&lt; 1.5</td>
</tr>
<tr>
<td><strong>ATMEL objectives</strong></td>
<td>35</td>
<td>25</td>
<td>&lt;1.5</td>
</tr>
<tr>
<td><strong>Committed</strong></td>
<td>3.00 ± 10%</td>
<td>12</td>
<td>&lt; 0.4</td>
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<tr>
<td><strong>ATMEL objectives</strong></td>
<td>20</td>
<td>14</td>
<td>&lt; 1.0</td>
</tr>
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</table>
ERC32 Single Chip development

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OCD

FPU

MEC

IU

Table:

<table>
<thead>
<tr>
<th>A</th>
<th>W min</th>
<th>W max</th>
<th>H min</th>
<th>H max</th>
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<tr>
<td>C</td>
<td>0.10</td>
<td>0.20</td>
<td>0.19</td>
<td>0.29</td>
</tr>
<tr>
<td>D</td>
<td>0.50</td>
<td>1.25</td>
<td>2.00</td>
<td>2.50</td>
</tr>
<tr>
<td>E1</td>
<td>0.50</td>
<td>1.25</td>
<td>2.00</td>
<td>2.50</td>
</tr>
<tr>
<td>E2</td>
<td>0.50</td>
<td>1.25</td>
<td>2.00</td>
<td>2.50</td>
</tr>
<tr>
<td>e</td>
<td>0.300</td>
<td>0.350</td>
<td>0.300</td>
<td>0.350</td>
</tr>
<tr>
<td>f</td>
<td>0.15</td>
<td>0.20</td>
<td>0.15</td>
<td>0.20</td>
</tr>
<tr>
<td>A1</td>
<td>2.06</td>
<td>2.56</td>
<td>1.80</td>
<td>2.30</td>
</tr>
<tr>
<td>A2</td>
<td>0.35</td>
<td>0.58</td>
<td>0.32</td>
<td>0.54</td>
</tr>
<tr>
<td>L</td>
<td>0.20</td>
<td>0.20</td>
<td>0.123</td>
<td>0.166</td>
</tr>
<tr>
<td>N1</td>
<td>64</td>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N2</td>
<td>64</td>
<td>64</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Dimensions:
Functional Validation

• Validation plan rev 1.0 Feb 1999
• Current status:

<table>
<thead>
<tr>
<th>Bloc</th>
<th>Status</th>
<th>Comment</th>
</tr>
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<tbody>
<tr>
<td>System startup control</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>Integer Unit</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>Floating Point Unit</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>Access controller</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>Timers</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>UARTs</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>Wait-states and Time-out</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>Interrupt Ctrl</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>General Purpose Interface</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>EDAC / Parity</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>Direct Memory Access</td>
<td>Done</td>
<td>OK</td>
</tr>
<tr>
<td>Test Access Port</td>
<td>Done</td>
<td>OK</td>
</tr>
</tbody>
</table>
Electrical Characterization

- Covers from 2.7V up to 6.0V, from -55°C to +125°C
- Functional verification (all patterns at V and Temp)
- Dynamic/static measurements (example given for initial rev.)

<table>
<thead>
<tr>
<th>Timing</th>
<th>Worst case (5.0V range)</th>
<th>Comment for 30MHz speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>t5</td>
<td>10.8 nS</td>
<td>Critical / to improve</td>
</tr>
<tr>
<td>t8</td>
<td>35.6 nS</td>
<td>Critical / to improve</td>
</tr>
<tr>
<td>t9_D</td>
<td>16.5 nS</td>
<td>Critical / to improve</td>
</tr>
<tr>
<td>t13</td>
<td>18.3 nS</td>
<td>Critical / few nS to get</td>
</tr>
<tr>
<td>t15</td>
<td>35.6 nS</td>
<td>Critical / to improve</td>
</tr>
<tr>
<td>t7</td>
<td>33.0 nS</td>
<td>OK. No change requested</td>
</tr>
<tr>
<td>t9_CB</td>
<td>7.6 nS</td>
<td>OK. No change requested</td>
</tr>
<tr>
<td>t12</td>
<td>20.2 nS</td>
<td>OK. No change requested</td>
</tr>
<tr>
<td>t14</td>
<td>12.0 nS</td>
<td>Spec. to be changed</td>
</tr>
<tr>
<td>t57</td>
<td>13.7 nS</td>
<td>Change to t15 will make t57 better</td>
</tr>
</tbody>
</table>
Power Dissipation

![Graph showing power consumption versus frequency for Specification and Typical cases.](image)

**Specification**
- 20 mA/MHz

**Typical**
- 12 mA/MHz

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Tolerance to Total Dose

TSC695E vs Total Dose 5.5V

Annealing 5.5V

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Heavy ions test results

- 2 parts @ 4.5V & 2 parts @ 2.7V
- Test at Berkeley, CA
- eVAB-695, evaluation board used
- LATCH-UP detection
  - by external current threshold
  - In case of functional failure, no POWER-DOWN to not remove possible permanent LATCH-UP
- UPSET detection
  - By means of similar to what was used during the ERC chip set test
  - Internal registers then PARANOIA tests
  - Test status reporting via UART to monitor
  - In case of functional crash, RESET is sent to the eVAB-695.
# Response to Heavy ions

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>LET Threshold (MeV/mg/cm²)</th>
<th>Cross Section (cm²)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.5</td>
<td>&gt; 109.7</td>
<td>&lt; 2.0E-07</td>
<td>No Upset. No event in space</td>
</tr>
</tbody>
</table>
| 2.7         | 20                          | 2.2E-07             | Functional (*)  
3.3E-7 Error/device/day |

(*) The board used for test is not equipped with 3V tolerant products. Results assume errors are generated by the TSC695
SEU sensitivity @ 2.70V

\[ \tau = f(LET) \ (3\text{V}) \]

Cross section (cm$^2$)

LET (MeV/mg/cm$^2$)

0.0 20.0 40.0 60.0 80.0 100.0


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New revisions

- Improved memory interface / signals
- Corrected internal parity generation & checks
- Minor timing improvements
- Same die from 2.7V to 5.5V, Mil temp.
  - Speed: 25MHz @ 5V ±10%
  - 0.9W typ. @ 25MHz & 5.0V
- One single package: 256-pins MQFP (>70% space saved)
- Internal qualification pronounced as early as September 1999
- Changed to Rev.F to correct internal parity check deviations
- Space evaluation started (CNES contract)
JTAG On-Chip Debugger Features

- **Reset / Run / Stop**
- **Breakpoints**
  - 3 hardware breakpoints for program execution
  - 1 hardware breakpoint data memory access
  - ‘n ’ software breakpoints using trap patch mechanism
- **Step-in, Step-out, Step-over**
  - Assembly level
  - High language Level
- **Examination and Modification of Registers, Memory or I/O's**
- **Code Download, Inline Assembly for Local Patches**
Development tools

- Ada Cross compiler system
- Hard real-time tools, target simulator
- JTAG based TSC695 target emulator (*)
- VxWorks real-time operating system
- Rational/Verdix ADA cross-compiler Corp.
- RTEMS real-time kernel
- ADA95/C/C++ cross compiler system, simulator
- TLA 700 Logic analyser disassembler
- ADA95 compiler, based on GNAT
- ...

(*) Non intrusive breakpoint detection in executed instruction
References

- All major European space actors
- Selected for various Space applications:
  - Smart-1, Beagle 2, PHARAO, Ariane V, Radarsat, SAC-C ...
  - Generic Processor Units,
  - High reliability spacecraft buses,
  - Star trackers
  - Charge Particle Telescope (ESA experiment)
  - ...
- First QML-Q and QML-V parts delivered
  - SMD number: 5962-00540
Literature

- TSC695 user’s manual
- TSC695 data sheet
- eVAB695 user’s manual
- TSC695E errata sheet

- at www.atmel-wm.com
## Part Numbers

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Lead-times</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSC695F-25MA-E</td>
<td>On stock</td>
</tr>
<tr>
<td>TSC695F-25MA</td>
<td>6 Weeks</td>
</tr>
<tr>
<td>TSC695F-25MA/883</td>
<td>22 Weeks</td>
</tr>
<tr>
<td>5962-0054001QXC</td>
<td>20 Weeks</td>
</tr>
<tr>
<td>TSC695F-25SASB</td>
<td>35 Weeks</td>
</tr>
<tr>
<td>5962-0054001VXC</td>
<td>30 Weeks</td>
</tr>
<tr>
<td>TSC695-SKIT</td>
<td>On stock</td>
</tr>
</tbody>
</table>
Conclusions

- Fast & Successful transfer of the 3 ERC32 Chip set net-lists
- Dramatically improved performances:
  - Speed
  - Radiation Hardness
  - Power Consumption
  - Space / Weight
- Additional features while overall compatibility
- Enhanced development tools:
  - Support from ESTEC and European industry
  - Starter kit / Development board / Compiled model for hardware simulation
  - ATMEL-wm Semiconductors hot line