32 bit Embedded Real-time computing Core Single Chip Development
(ERC32SC/TSC695)

Contract 12598/FM (SC)

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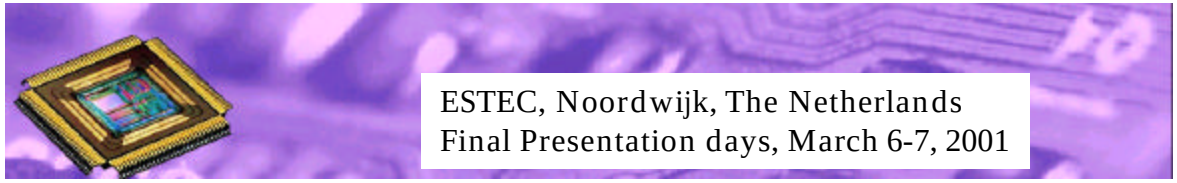


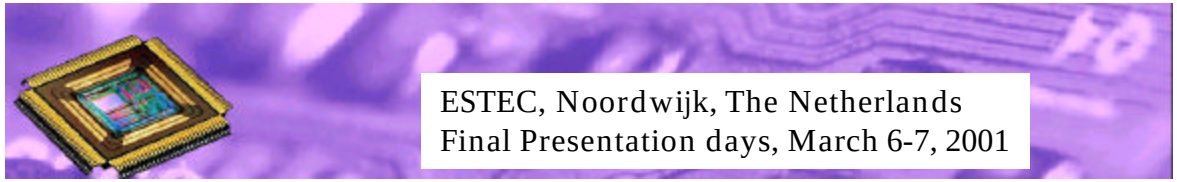
ESTEC, Noordwijk, The Netherlands
Final Presentation days, March 6-7, 2001

Agenda

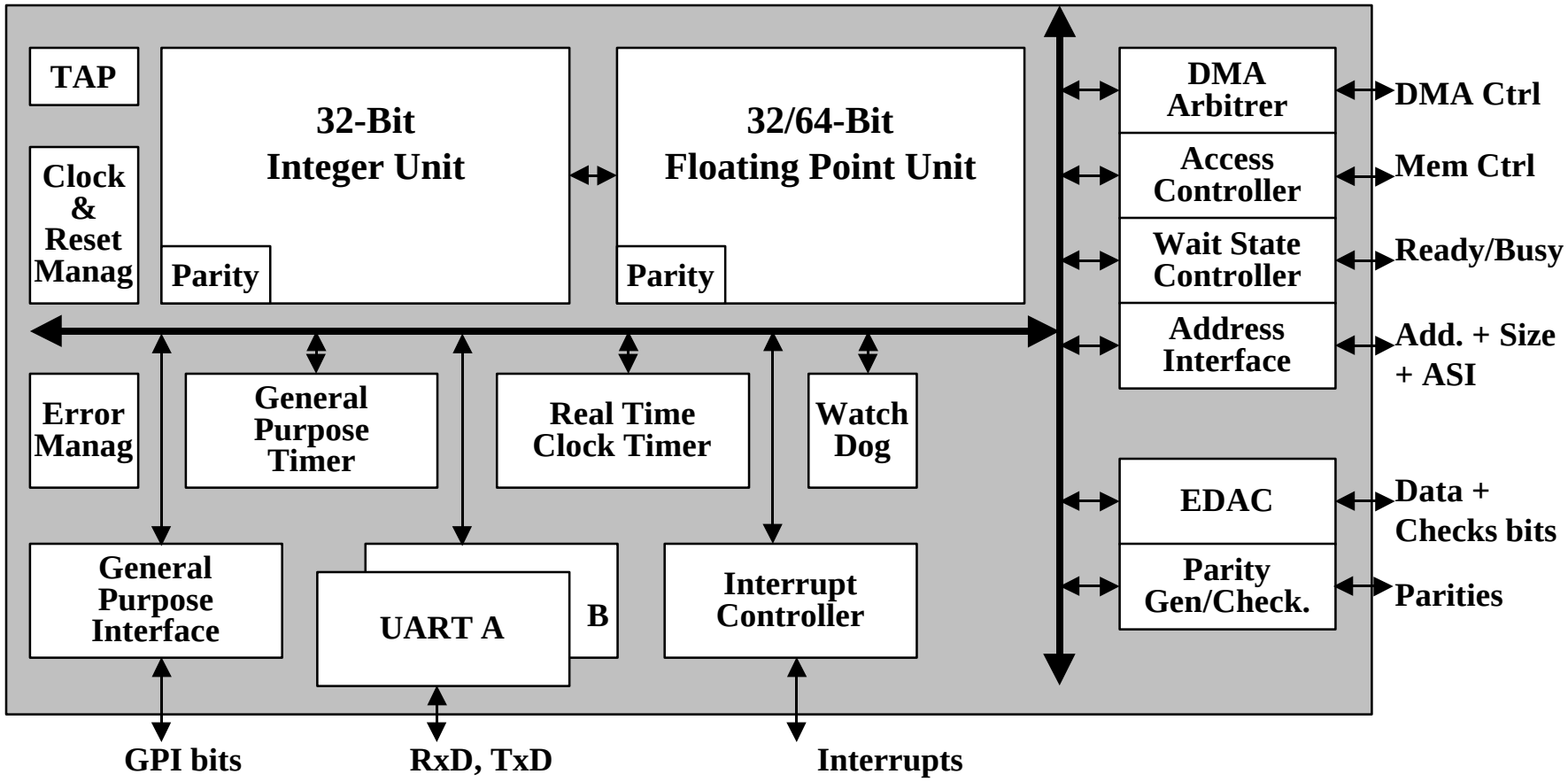
- Objectives of the contract
- Tentative specification
- Added / Removed functionality
- Electrical characterization
- Radiation test results
- Evaluation Board
- On Chip Debugger
- Part numbering
- Conclusions
- References

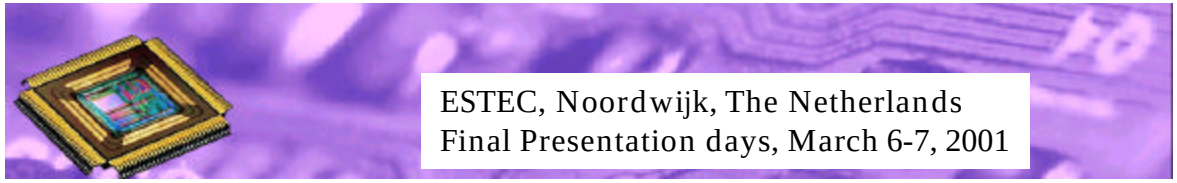
Program objectives

- 18 months overall program
- Monolithic version of the existing ERC32 chip set
- Identical set of net-lists with minimum changes
- Upward software functionality
- Improved functionality, speed, radiation hardness, “user friendly”
- 5V and 3V tolerant functionality
- Basic “foundry” functional validation



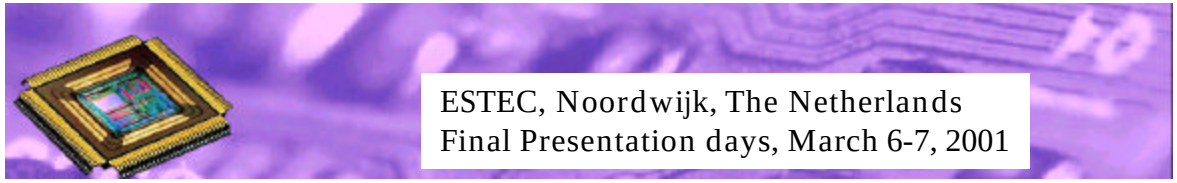
Block Diagram





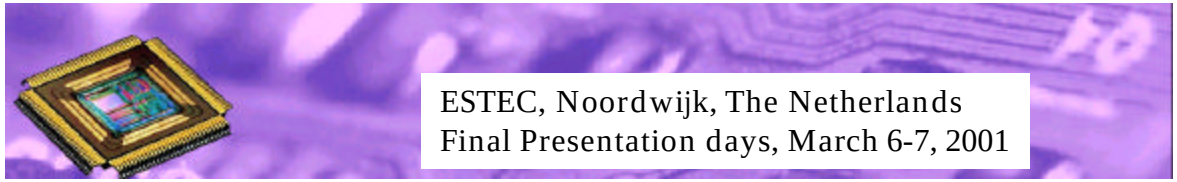
New Features

- **General Purpose Interface (µcontr. Functions)**
  - ✓ 8-bit parallel I/O port bit per bit configurable
  - ✓ Edge detection on GPI inputs => External interrupt
- **FLASH compatibility**
- **Selectable NMI or Watchdog**
- **High Drive Capability**
  - ✓ Up to 400 pF for Address buffers
  - ✓ Address latches included
  - ✓ Up to 150 pF for Data, Controls & Clock buffers
- **On-Chip Debugger for JTAG Emulator with Read/Write access for all Registers and I/Os**

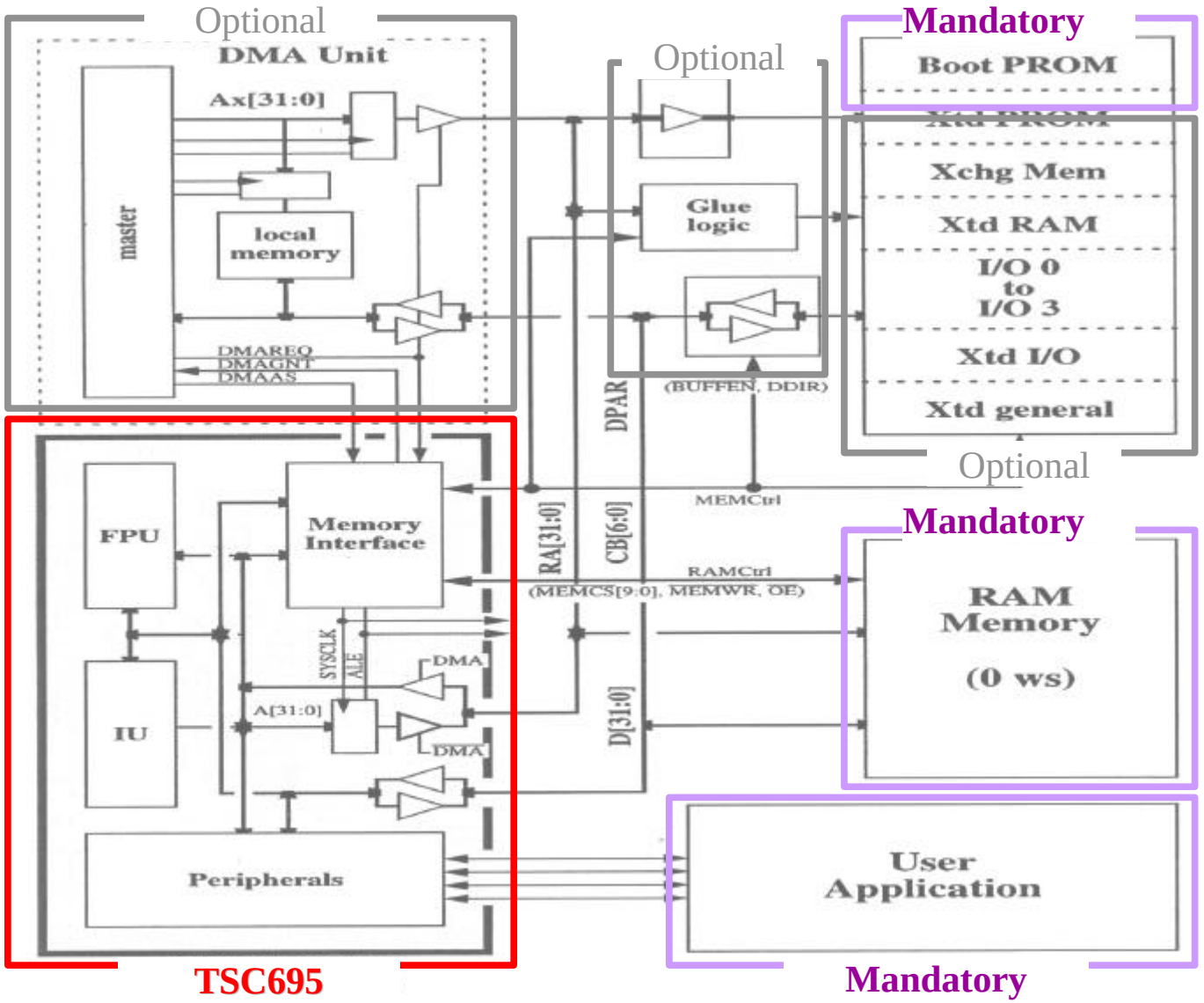


No longer supported

- **Master/checker mode *(Never used by customers)***
- **Program flow control *(Not supported by compilers)***
- **601/602 modes *(Internal parities always checking)***
- **Coprocessor capability *(Never used, embedded processor)***

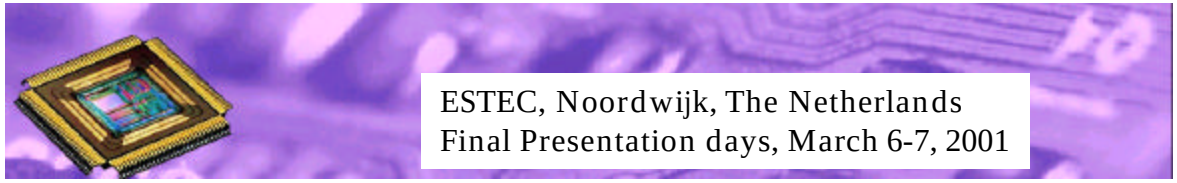


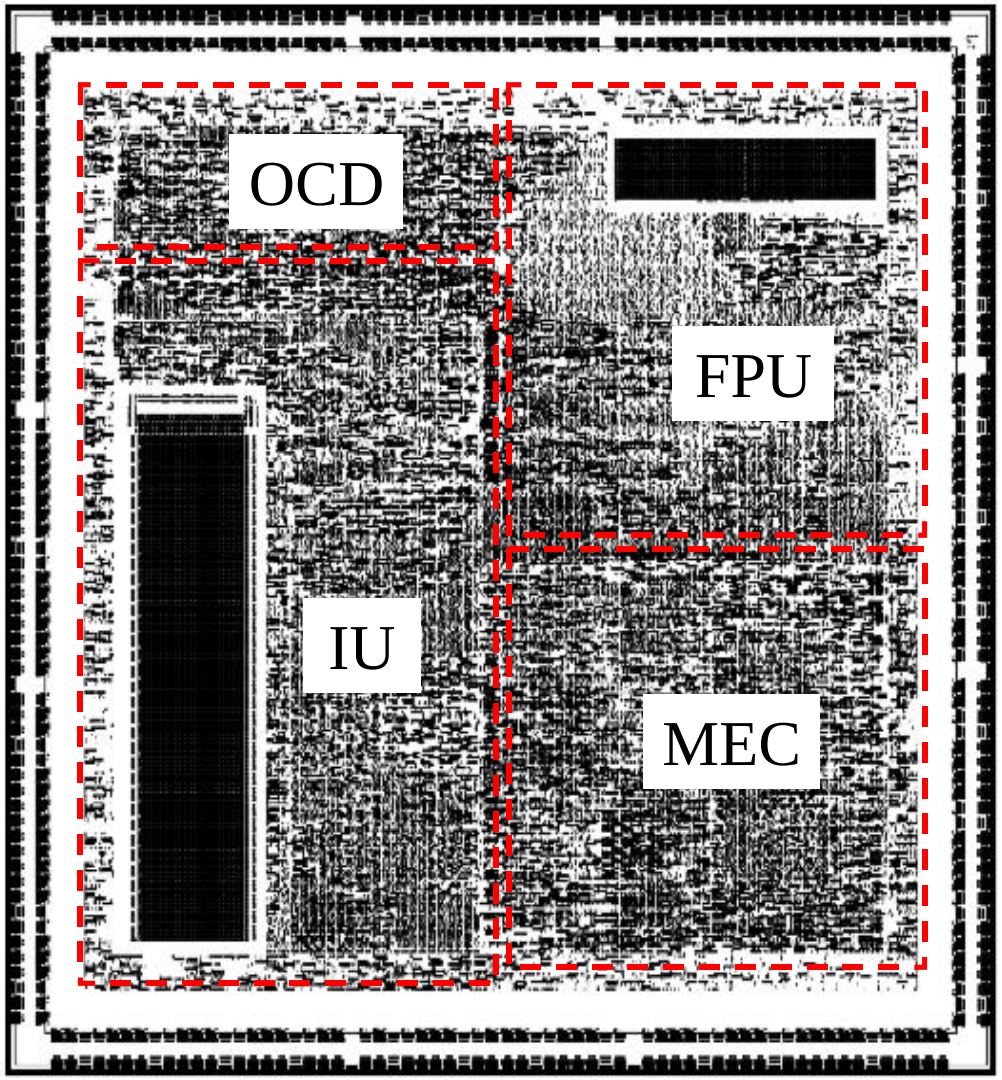
Typical Application



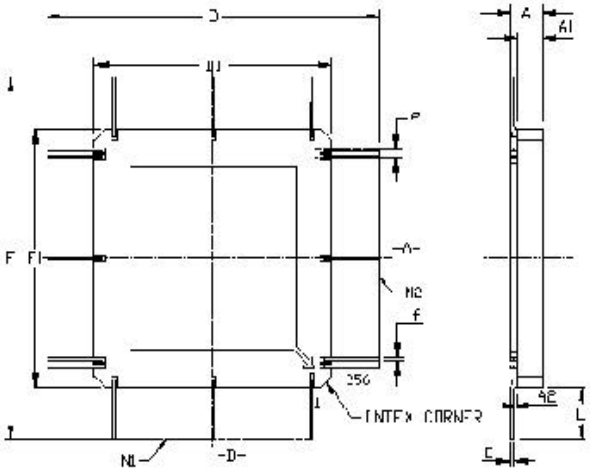
Contractual specification

	Power supply (V)	Speed (MHz)	MIPS	Power (W)
Committed	5.00 ± 10%	20	14	< 1.5
ATMEL objectives		35	25	<1.5
Committed	3.00 ± 10%	12	8	< 0.4
ATMEL objectives		20	14	< 1.0





256 LEAD MQFP_F

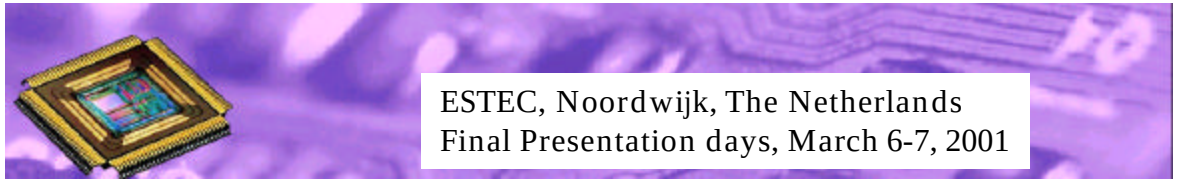


	mm		mils	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
C	0.10	0.20	.004	.008
D	53.23	55.74	2.095	2.195
D1	36.83	37.34	1.450	1.470
E	53.23	55.74	2.095	2.195
E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
f	0.15	0.25	.006	.010
A1	2.06	2.56	.081	.101
A2	0.05	0.36	.002	.014
L	8.20	9.20	.323	.362
N1	64		64	
N2	64		64	

Functional Validation

- Validation plan rev 1.0 Feb 1999
- Current status:

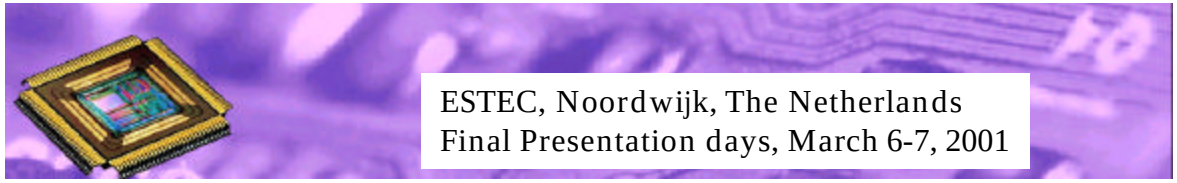
Bloc	Status	Comment
System startup control	Done	OK
Integer Unit	Done	OK
Floating Point Unit	Done	OK
Access controller	Done	OK
Timers	Done	OK
UARTs	Done	OK
Wait-states and Time-out	Done	OK
Interrupt Ctrl	Done	OK
General Purpose Interface	Done	OK
EDAC / Parity	Done	OK
Direct Memory Access	Done	OK
Test Access Port	Done	OK



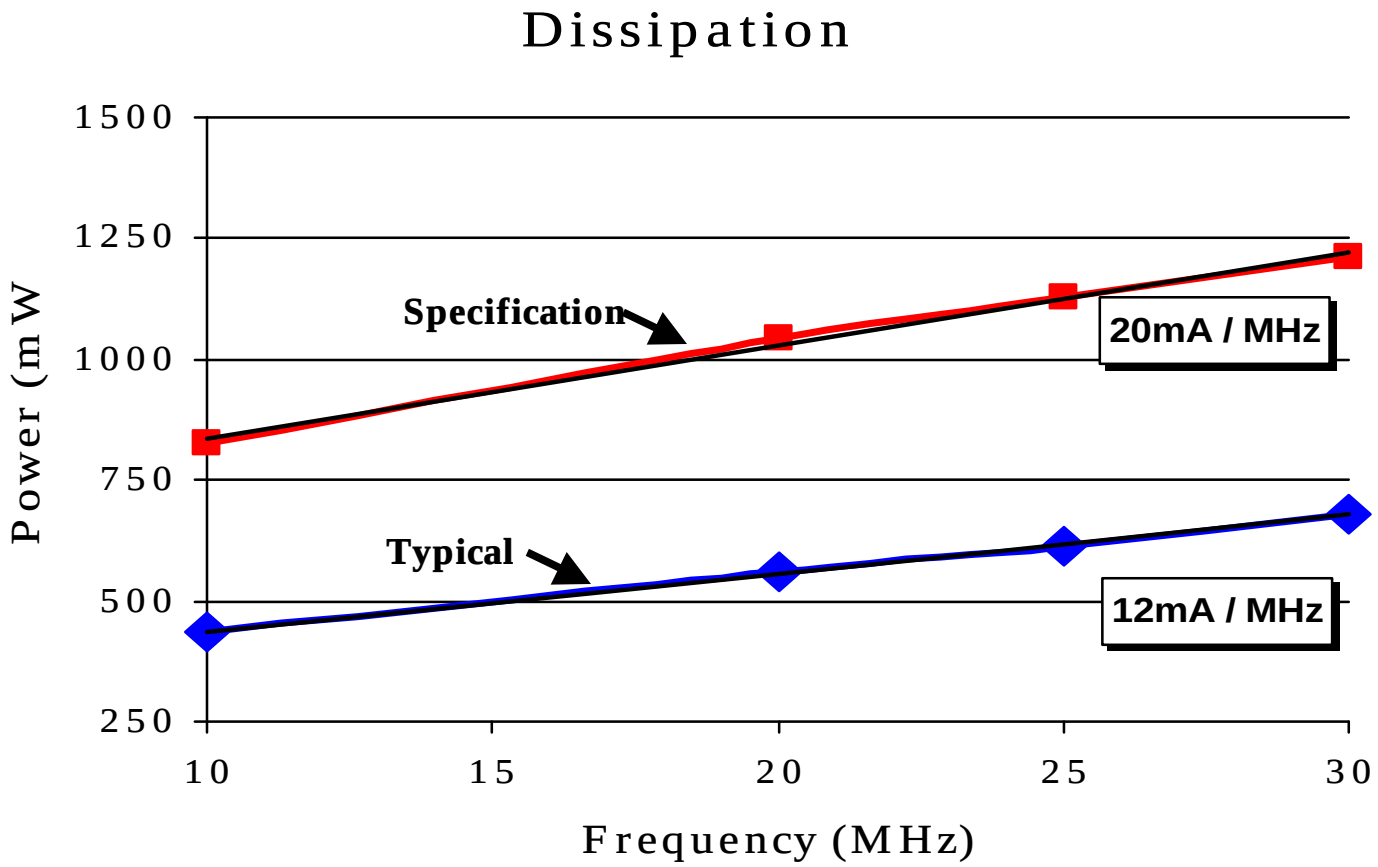
Electrical Characterization

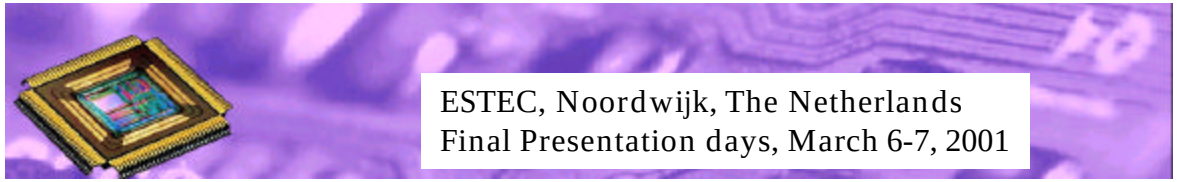
- **Covers from 2.7V up to 6.0V, from -55°C to +125°C**
- **Functional verification (all patterns at V and Temp)**
- **Dynamic/static measurements** ***(example given for initial rev.)***

Timing	Worst case (5.0V range)	Comment for 30MHz speed
t5	10.8 nS	Critical / to improve
t8	35.6 nS	Critical / to improve
t9_D	16.5 nS	Critical / to improve
t13	18.3 nS	Critical / few nS to get
t15	35.6 nS	Critical / to improve
t7	33.0 nS	OK. No change requested
t9_CB	7.6 nS	OK. No change requested
t12	20.2 nS	OK. No change requested
t14	12.0 nS	Spec. to be changed
t57	13.7 nS	Change to t15 will make t57 better



Power


Dissipation
1500
1250
1000
750
500
250
Power (mW
Specification
20mA / MHz
Typical
12mA / MHz
10
15
20
25
30
Frequency (MHz)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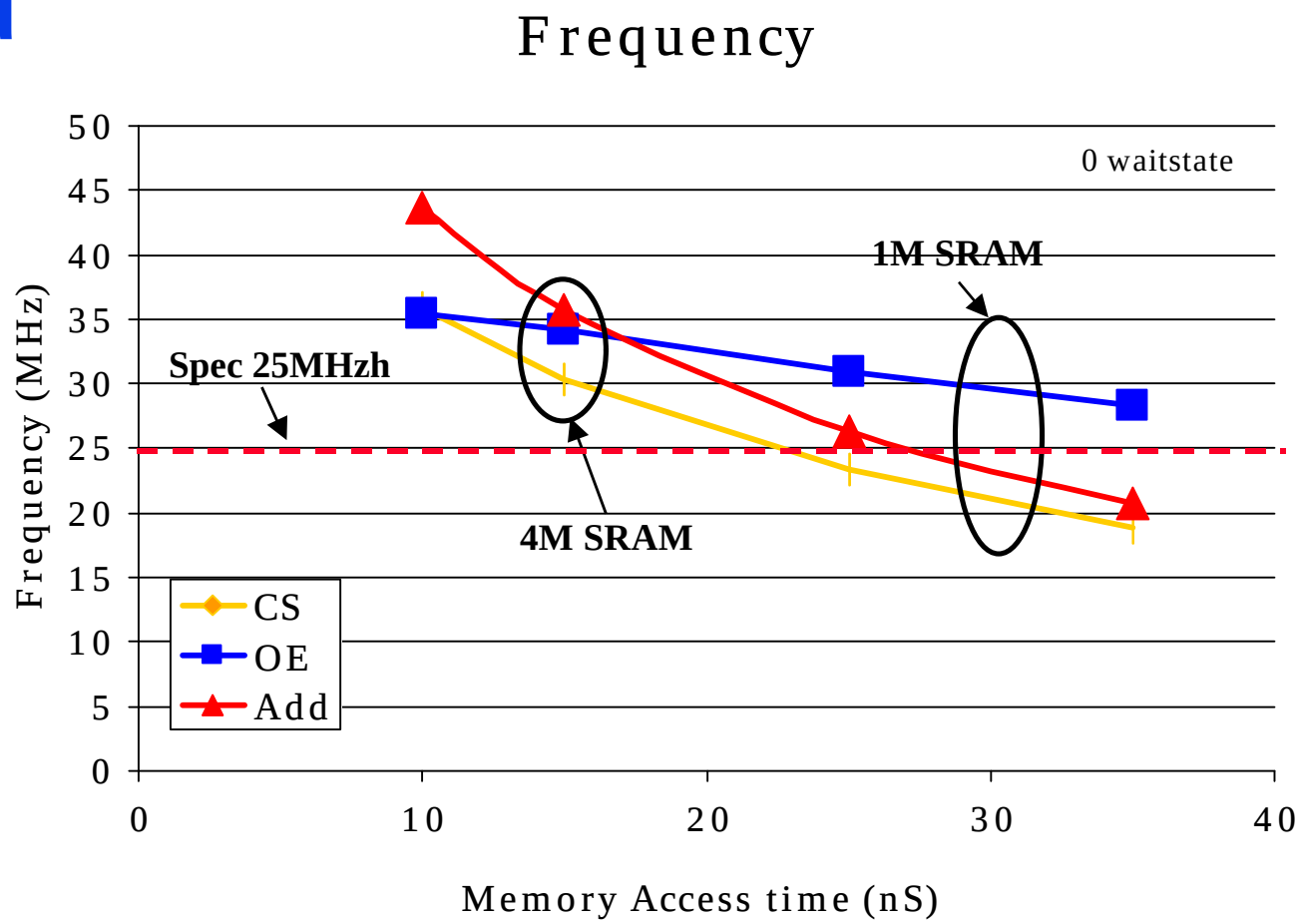
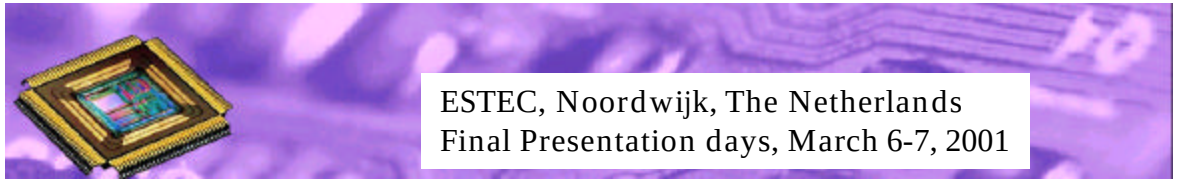
Speed


Frequency
0 waitstate
1M SRAM
Spec 25MHzh
4M SRAM
CS
OE
Add
Frequency (MHz)
Memory Access time (nS)
0
5
10
15
20
25
30
35
40
45
50
0
10
20
30
40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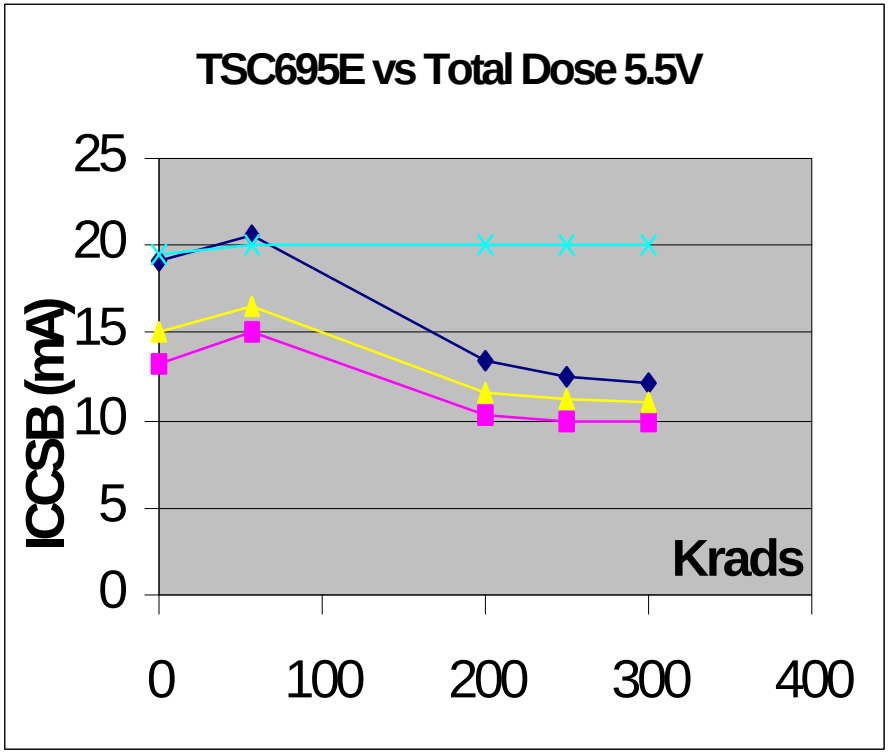
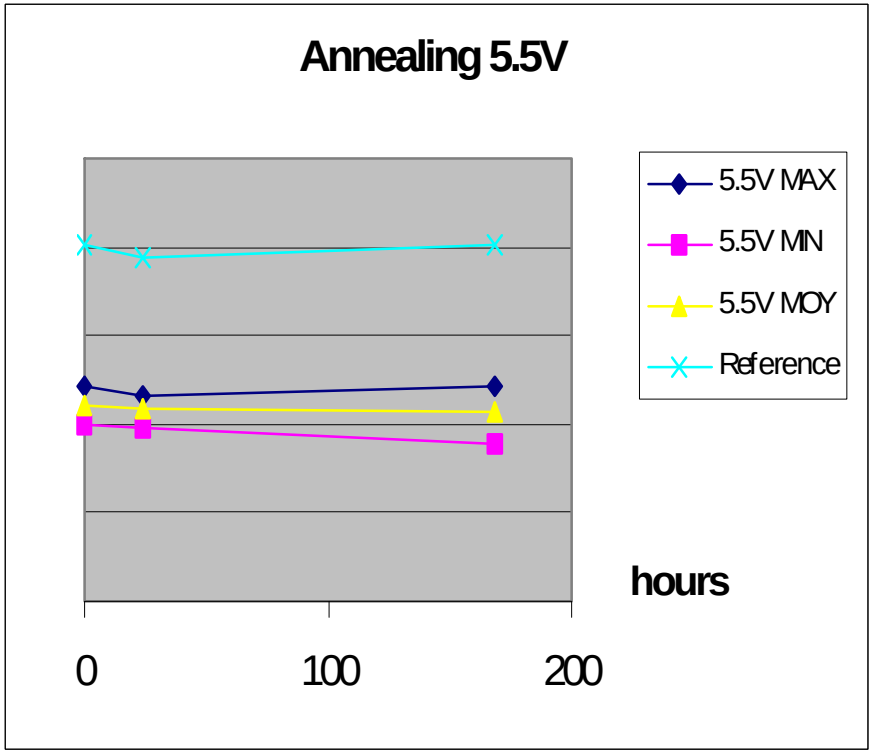
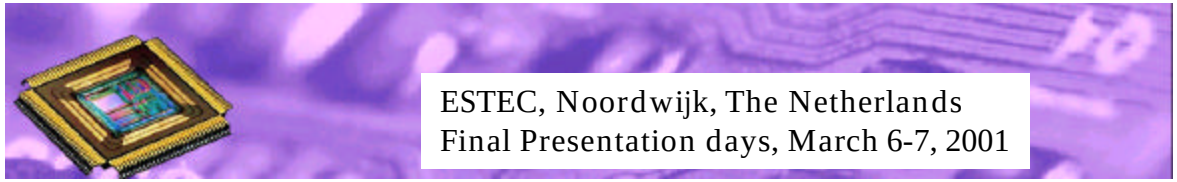
Tolerance to Total Dose

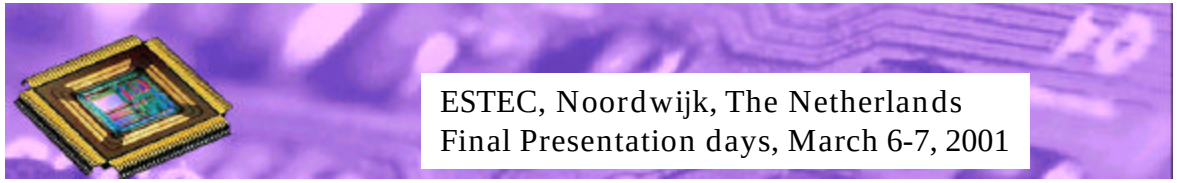






Heavy ions test results

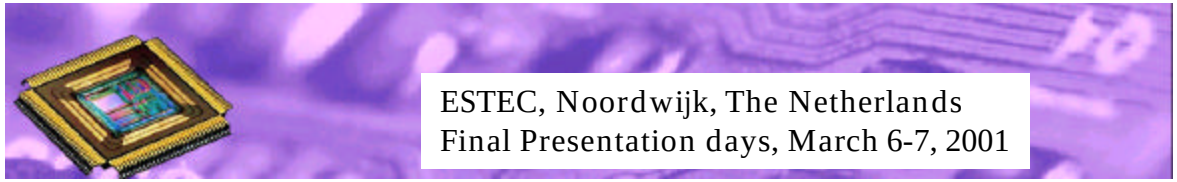
- 2 parts @ 4.5V & 2 parts @ 2.7V
- Test at Berkeley, CA
- eVAB-695, evaluation board used
- LATCH-UP detection
  - ✓ by external current threshold
  - ✓ In case of functional failure, no POWER-DOWN to not remove possible permanent LATCH-UP
- UPSET detection
  - ✓ By means of similar to what was used during the ERC chip set test
  - ✓ Internal registers then PARANOIA tests
  - ✓ Test status reporting via UART to monitor
  - ✓ In case of functional crash, RESET is sent to the eVAB-695.



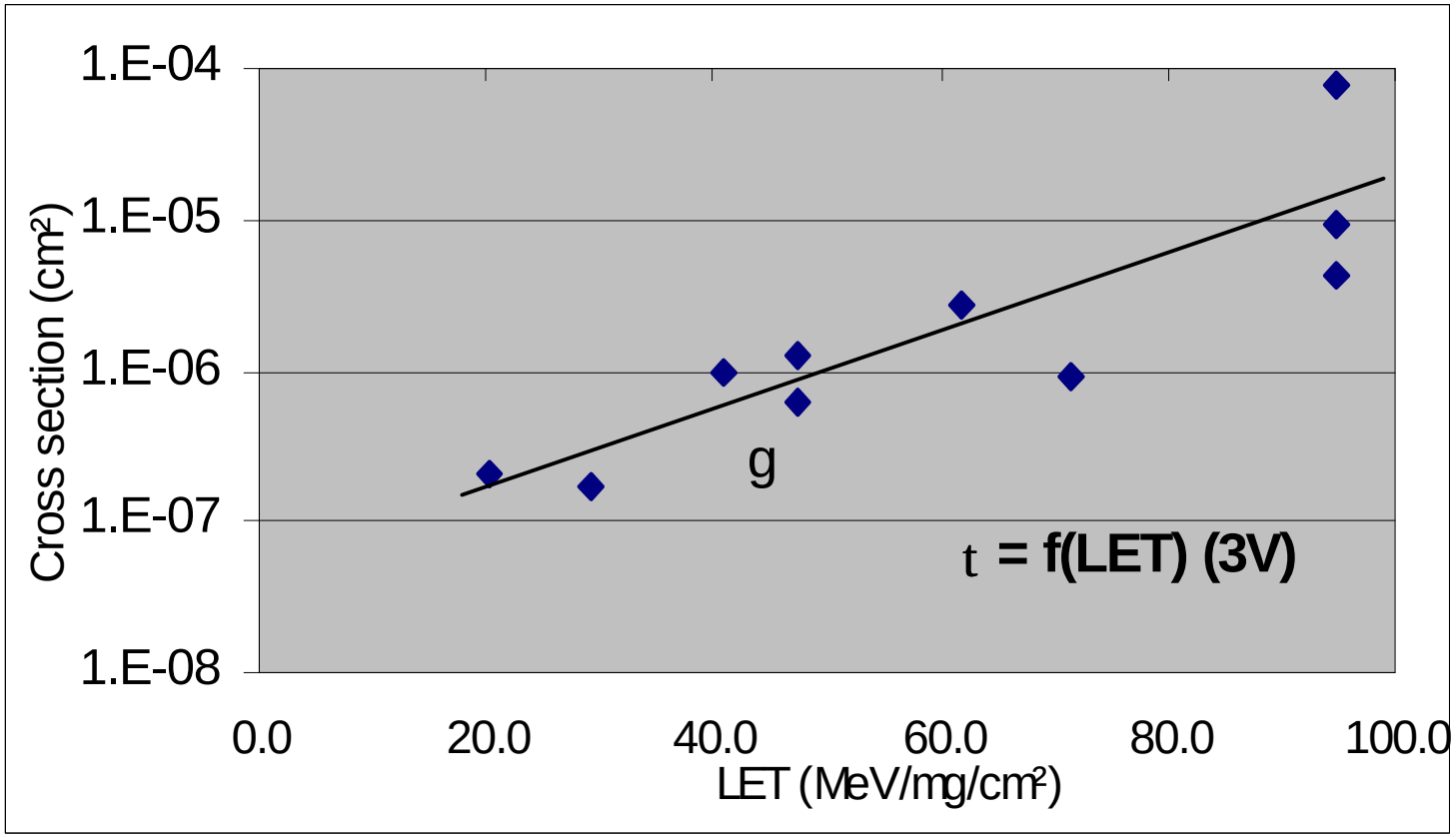
Response to Heavy ions

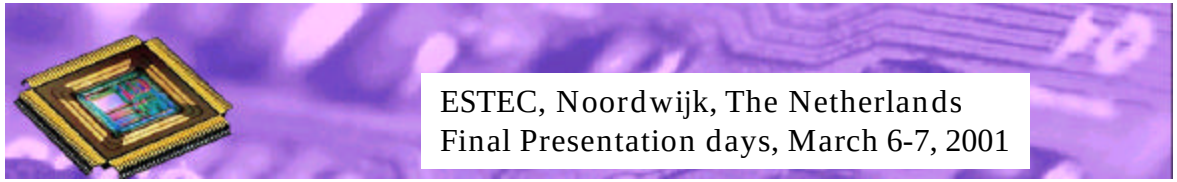
Voltage (V)	LET Threshold (MeV/mg/cm²)	Cross Section (cm²)	Comments
4.5	> 109.7	< 2.0E-07	No Upset. No event in space
2.7	20	2.2E-07	Functional (*) 3.3E-7 Error/device/day

(*) The board used for test is not equipped with 3V tolerant products. Results assume errors are generated by the TSC695



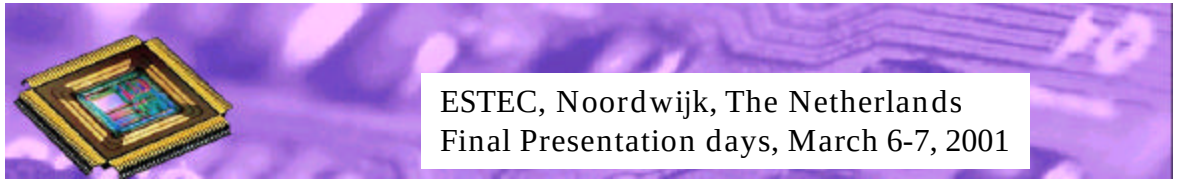
SEU sensitivity @ 2.70V





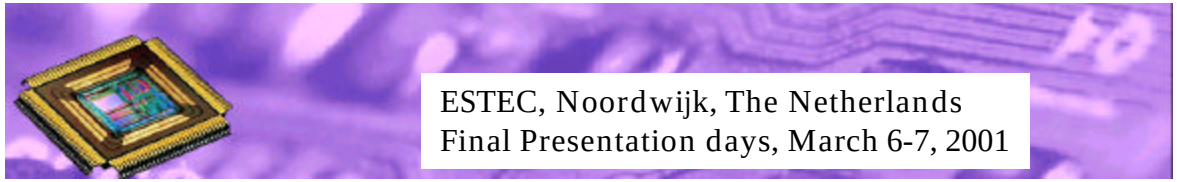
New revisions

- Improved memory interface / signals
- Corrected internal parity generation & checks
- Minor timing improvements
- Same die from 2.7V to 5.5V, Mil temp.
  - Speed: 25MHz @ 5V ±10%
  - 0.9W typ. @ 25MHz & 5.0V
- One single package: 256-pins MQFP (>70% space saved)
- Internal qualification pronounced as early as September 1999
- Changed to Rev.F to correct internal parity check deviations
- Space evaluation started (CNES contract)



JTAG On-Chip Debugger Features

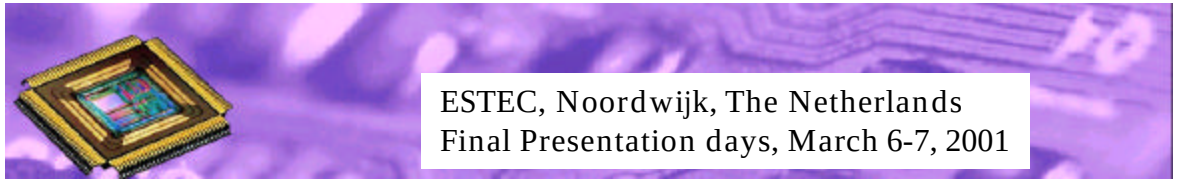
- **Reset / Run / Stop**
- **Breakpoints**
  - ✓ **3 hardware breakpoints for program execution**
  - ✓ **1 hardware breakpoint data memory access**
  - ✓ **‘n ’ software breakpoints using trap patch mechanism**
- **Step-in, Step-out, Step-over**
  - ✓ **Assembly level**
  - ✓ **High language Level**
- **Examination and Modification of Registers, Memory or I/O's**
- **Code Download, Inline Assembly for Local Patches**



Development tools

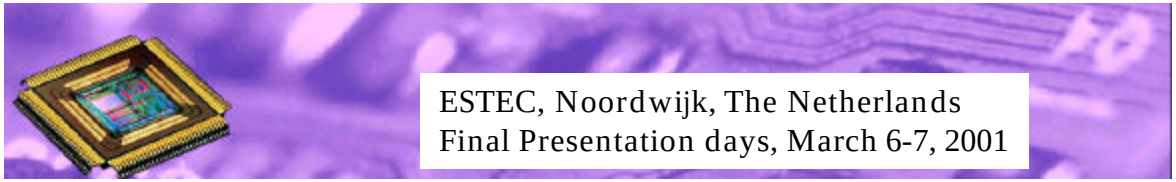
• Ada Cross compiler system	Aonix
• Hard real-time tools, target simulator	Spacebel
• JTAG based TSC695 target emulator (*)	Spacebel
• VxWorks real-time operating system	Wind River Syst. Inc.
• Rational/Verdix ADA cross-compiler	Rational Software Corp.
• RTEMS real-time kernel	OAR
• ADA95/C/C++ cross compiler system, simulator	ESA/ESTEC
• TLA 700 Logic analyser disassembler	Tektronix
• ADA95 compiler, based on GNAT	ADA Core Technologies
• …	

(*) Non intrusive breakpoint detection in executed instruction



References

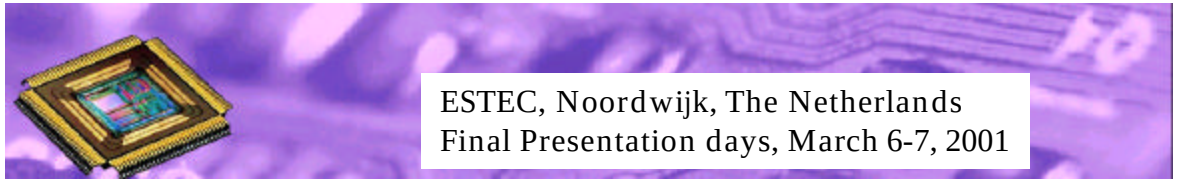
- All major European space actors
- Selected for various Space applications:
  - Smart-1, Beagle 2, PHARAO, Ariane V, Radarsat, SAC-C ...
  - Generic Processor Units,
  - High reliability spacecraft buses,
  - Star trackers
  - Charge Particle Telescope (ESA experiment)
  - …
- First QML-Q and QML-V parts delivered
  - SMD number: 5962-00540



Literature

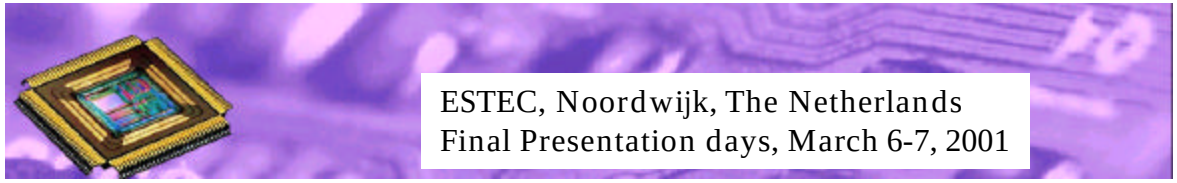
- TSC695 user's manual
- TSC695 data sheet
- eVAB695 user's manual
- TSC695E errata sheet

- at www.atmel-wm.com

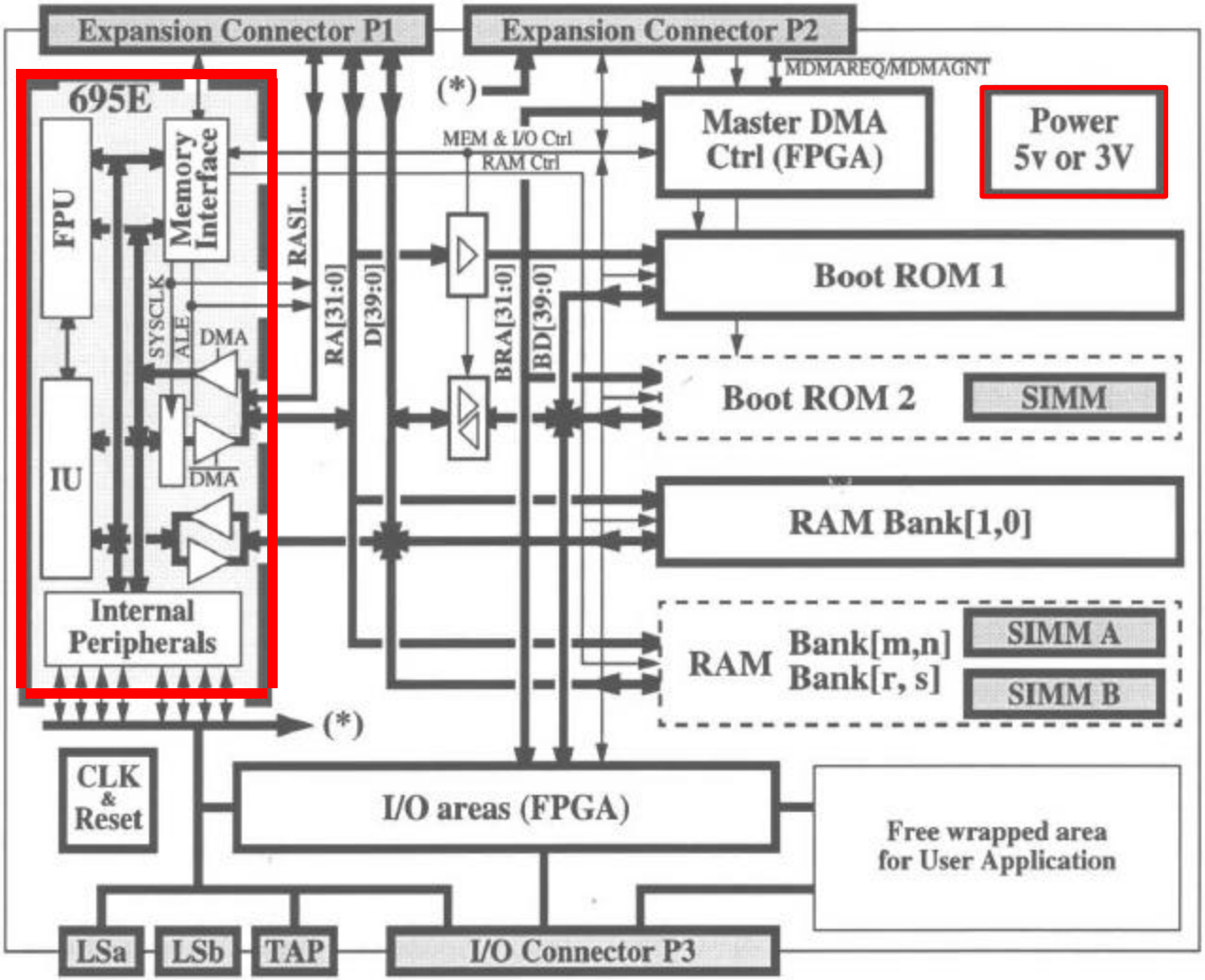


Part Numbers

Part Number	Lead-times
• TSC695F-25MA-E	On stock
• TSC695F-25MA	6 Weeks
• TSC695F-25MA/883	22 Weeks
• 5962-0054001QXC	20 Weeks
• TSC695F-25SASB	35 Weeks
• 5962-0054001VXC	30 Weeks
• TSC695-SKIT	On stock



eVAB-695


Expansion Connector P1
Expansion Connector P2
695E
FPU
Memory Interface
IU
Internal Peripherals
SYSCLK
ALE
DMA
DMA
RASL..
RA[31:0]
D[39:0]
(*)
MEM & I/O Ctrl
RAM Ctrl
BRA[31:0]
BD[39:0]
MDMAREQ/MDMAGNT
Master DMA Ctrl (FPGA)
Power 5v or 3V
Boot ROM 1
Boot ROM 2
SIMM
RAM Bank[1,0]
RAM
Bank[m,n]
Bank[r, s]
SIMM A
SIMM B
(*)
CLK & Reset
I/O areas (FPGA)
Free wrapped area for User Application
LSa
LSb
TAP
I/O Connector P3

Conclusions

- **Fast & Successful transfer of the 3 ERC32 Chip set net-lists**
- **Dramatically improved performances :**
  - **Speed**
  - **Radiation Hardness**
  - **Power Consumption**
  - **Space / Weight**
- **Additional features while overall compatibility**
- **Enhanced development tools :**
  - **Support from ESTEC and European industry**
  - **Starter kit / Development board / Compiled model for hardware simulation**
  - **ATMEL-wm Semiconductors hot line**