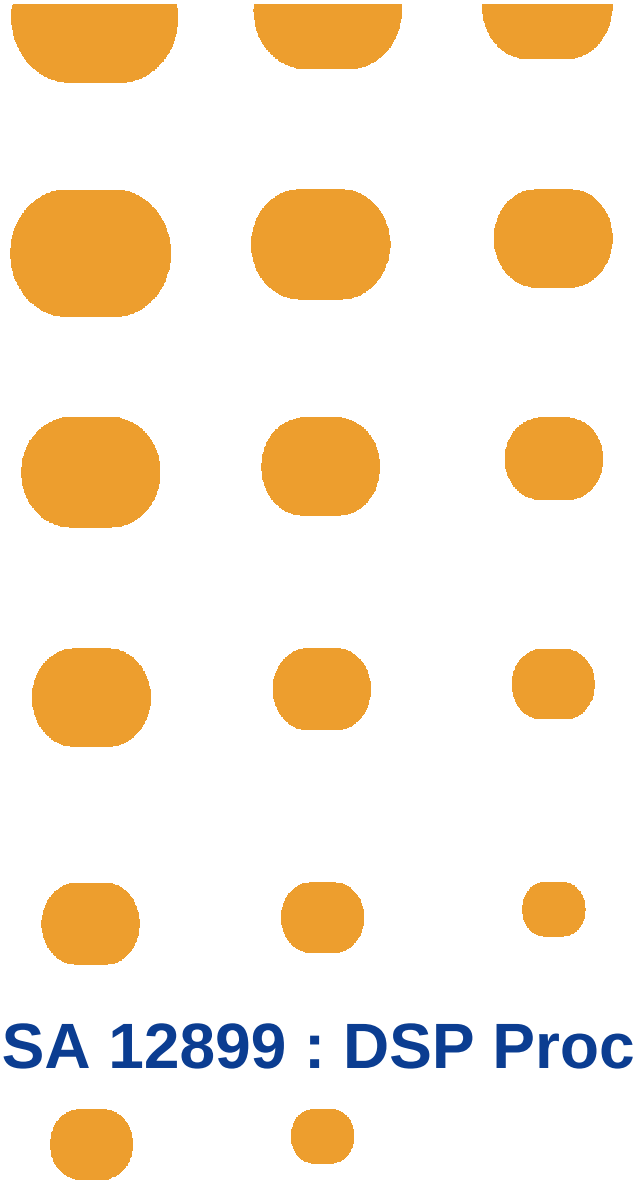

ESA 12899 : DSP Processor Peripheral Controller (DSP/T7904E)

Microelectronics Final Presentation Days,
Room Fresnel, ESTEC, Noordwijk, The Netherlands, March 6th

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Summary

- Contract history / background
- Objectives of the study
- DPC ASIC Environment, Functionality and Main technical features
- DPC ASIC development specificity and validation approach
- Technical solutions for process/matrix
- Encountered difficulties / lessons learned
- DPC ASIC test board features and validation results
- Application : MCM DSP Implementation
- MCM DSP Functionality and Main technical features
- MCM DSP test board features and validation results
- DPC ASIC and MCM DSP assessment and availability
- User base and applications
- Conclusion

Contract history / background (1/3)

- **The Processing Units trends for Space Applications are :**
  - **Computing Performances : 5 MIPS to 100 MIPS**
  - **Very strong Real Time constraints**
  - **Centralised or distributed architecture**

➲ **ADSP-21020 from Analog Devices has been transfered to the european foundry ATMEL Wireless & µC under the reference TSC21020F in the frame of an ESA contract in 1998.**

Contract history / background (2/3)

- Signal Processing Applications require additional efficient support for :
  - Initialisation of Program Memory
  - Memory type Compatibility (SRAM/DRAM) and Protection management
  - Interfacing with data handling systems, instruments and other processors in case of parallel processing extensions

➲ Possible implementation using discrete logic or FPGA results in larger board designs, lower performance and reliability and is not suitable for large number board manufacturing.

➲ ESA 12899 contract is managed by Sandi Habinc at ESTEC to develop a generic support device suitable for on-board applications based on the ADSP-21020 and the TSC21020E processors

➲ ASTRIUM was selected as prime contractor for this activity

➲ Atmel Wireless & µC was selected for the ASIC fundry activities

Contract history / background (3/3)

- Space Application requires also :
  - Very high integration level (weight and volume reduction)
  - Adaptation to critical environments (thermal, mechanical, EMC, pressure, radiation)
  - Compatibility with the Space qualification needs
  - Procurement cost reduction

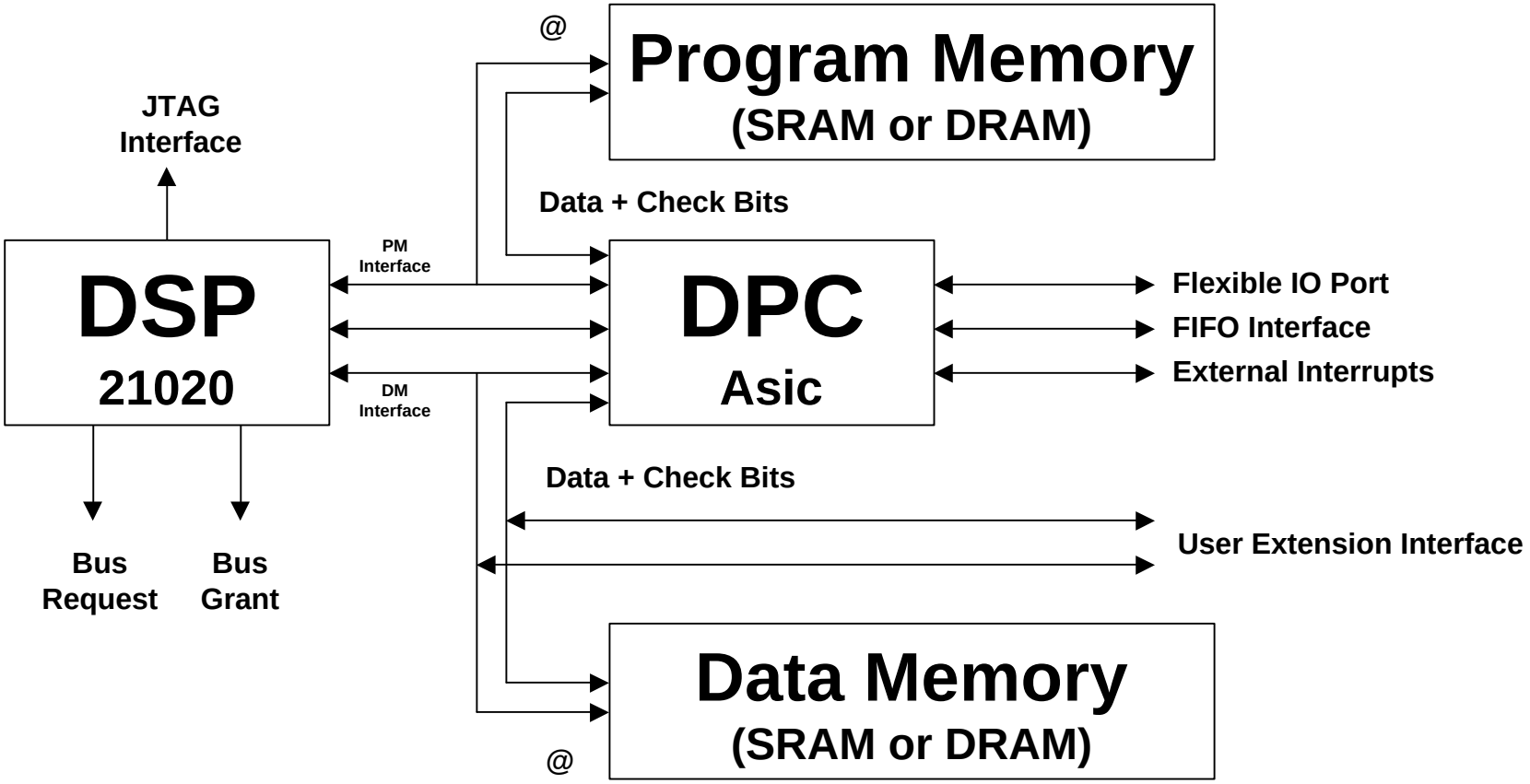
➲ New packaging solution requirement to fit these needs and to be compatible with the increasing number of devices I/Os

➲ In 1998, ASTRIUM started in parallel the development of the MCM DSP implementing one DSP System based on the DP21020F and the DSP Peripheral Controller in a single package.

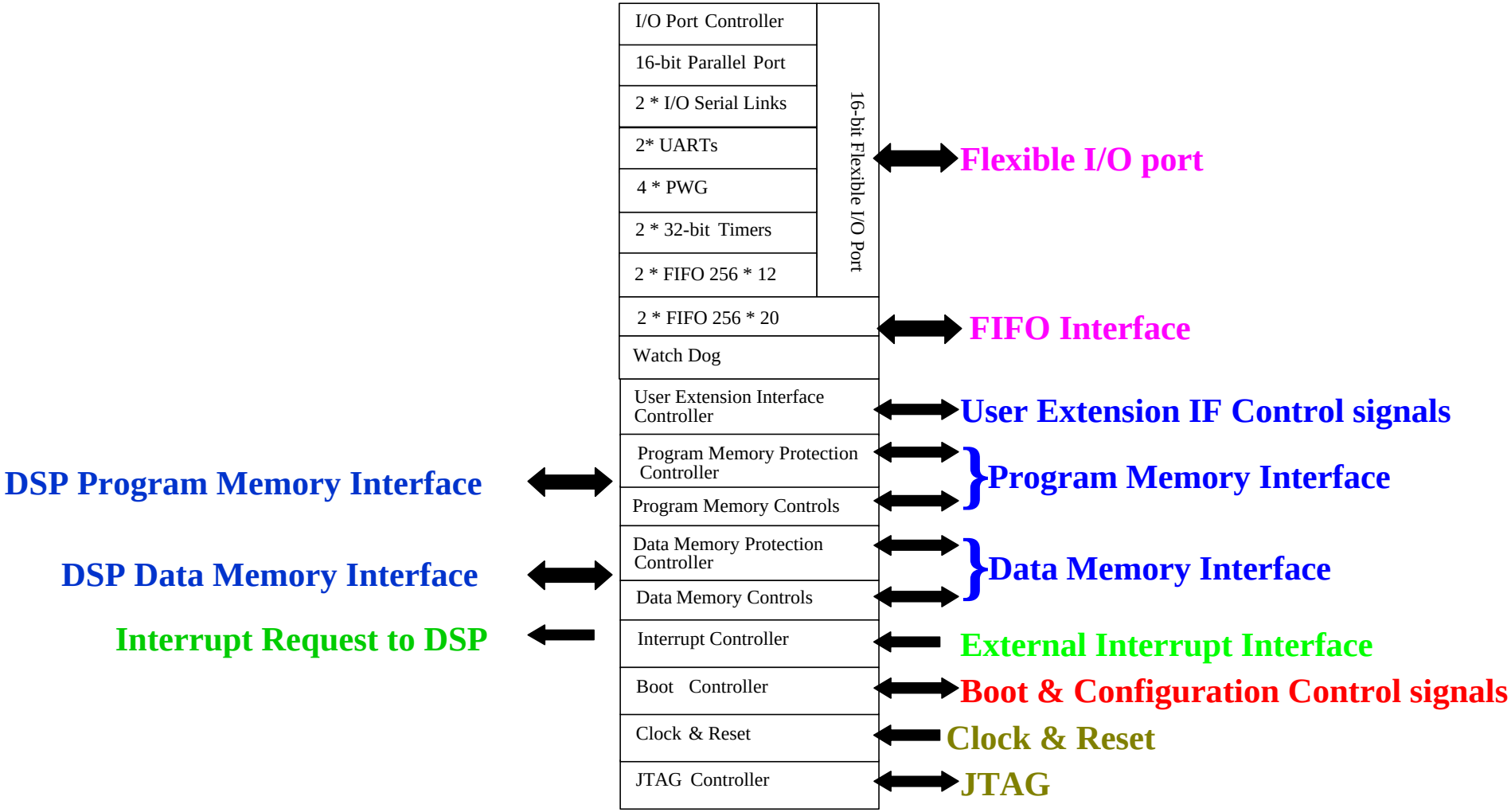
Objectives of the study

- Design and manufacture a first-time-right generic support device suitable for on-board applications based on the ADSP-21020 and the TSC21020E processors
- Validate the functionality of the developed device with a board featuring the device and the target processors
- Ensure that the developed device is unrestrictedly available from and supported by the manufacturing foundry as an ASSP with a comprehensive data sheet
- Ensure the availability of the device in both die and packaged form
- Develop and manufacture an integrated MCM DSP system using the DPC ASIC
- Ensure the availability of the MCM DSP for the space industry

DPC ASIC Environment



DPC ASIC Functionality



DPC ASIC Main technical features (1/2)

- The DPC ASIC provides the following functions :
  - DSP21020F Access management
  - Up to 4 MWords SRAM and DRAM Memory management support on both Program and Data Buses
  - Program and Data Memory EDAC (die only) and Parity Protection
  - Various System Boot options
  - External interrupt management
  - User Interface with various facilities management (full duplex UARTS, PWG, cascadable timers, watch dog timer, ...)

DPC ASIC Main technical features (2/2)

- **Performances :**
  - Intrinsic Performance : 20 MHz
  - Voltage range : 4.5 to 5.5 V
  - Temperature range : -55 to +125 °C
  - Power consumption : < 2 W
- **Technology :**
  - Total dose radiation tolerance : 100 Krads
  - Latch-Up immunity better than 100 Mev
  - SEU LET threshold better than 25 Mev/cm²/mg
- **Packaging :**
  - Ceramic 256 FQFP F and Bare Die

DPC ASIC development specificity

- DSP21020 interface
  - Difficult to meet => use of internal quicker clock
  - Phase between DPC clock and DSP clock
- PLL or external oscillator
- Atmel MG2RT development flow and library validation
- Two different versions with some different functionnalities : 256 QFP package and die (for MCM DSP integration)

DPC ASIC Validation Approach (1/2)

- **Simulations are done at DPC level and at Board level with test benches**

- **DPC Level :**
  - **Use of emulators (generation and check) for all the interfaces (Serial Link, UART, Memory,…), and also for the DSP (Read/Write model only)**
  - **Exhaustive simulations of the whole functions**

DPC ASIC Validation Approach (2/2)

- **Simulations are also done at Board level with test benches**
- **Board level :**
  - **Use of the DSP netlist (Gate Level VHDL delivered by ATMEL) for performing simulations with the best possible accuracy**
  - **Use of emulators (generation and check) for the others interfaces**
  - **Intensive simulations of nominal and special cases such as**
    - Boot procedure, Reset phase, and DSP start
    - Memory Access : nominal, aborted (with particular branch execution), extended (with different Wait States configurations), and interrupted (validation of the interrupt process influence)
    - Memory Protection : EDAC, Parity and No protection executed on all the previous DSP memory accesses

Technical solutions for process/matrix

- MG2RT process of ATMEL was selected
- Internal parity protection against SEU
- Total Dose tolerance of DPC is over 50 krads
- JTAG Boundary Scan is implemented for board level testing
- Functional vectors and Scan used. 97 % fault coverage
- MG2265E matrix used (MG2RT) - MQFP256 (package or die)
  - 185791 gates used for 264375 available gates = 70.28 %
  - Die version : 362 pads used for 362 available pads.
    324 signals, 6 power pins for core, 32 power pins for buffers
  - Package version : 243 pins used for 256 available pins
    200 signals, 6 power pins for core, 32 power pins for buffers, 5 pins for PLL

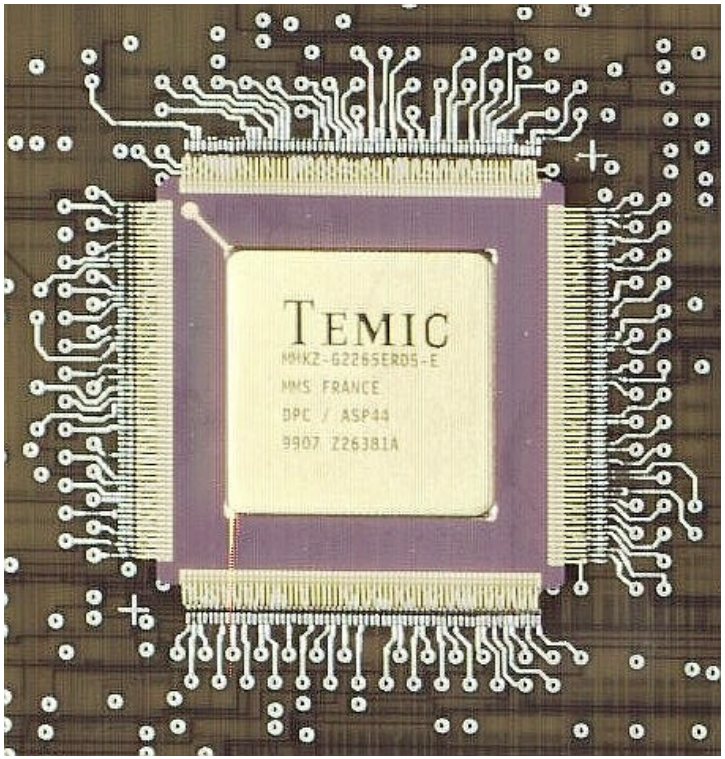
Encountered difficulties / lessons learned

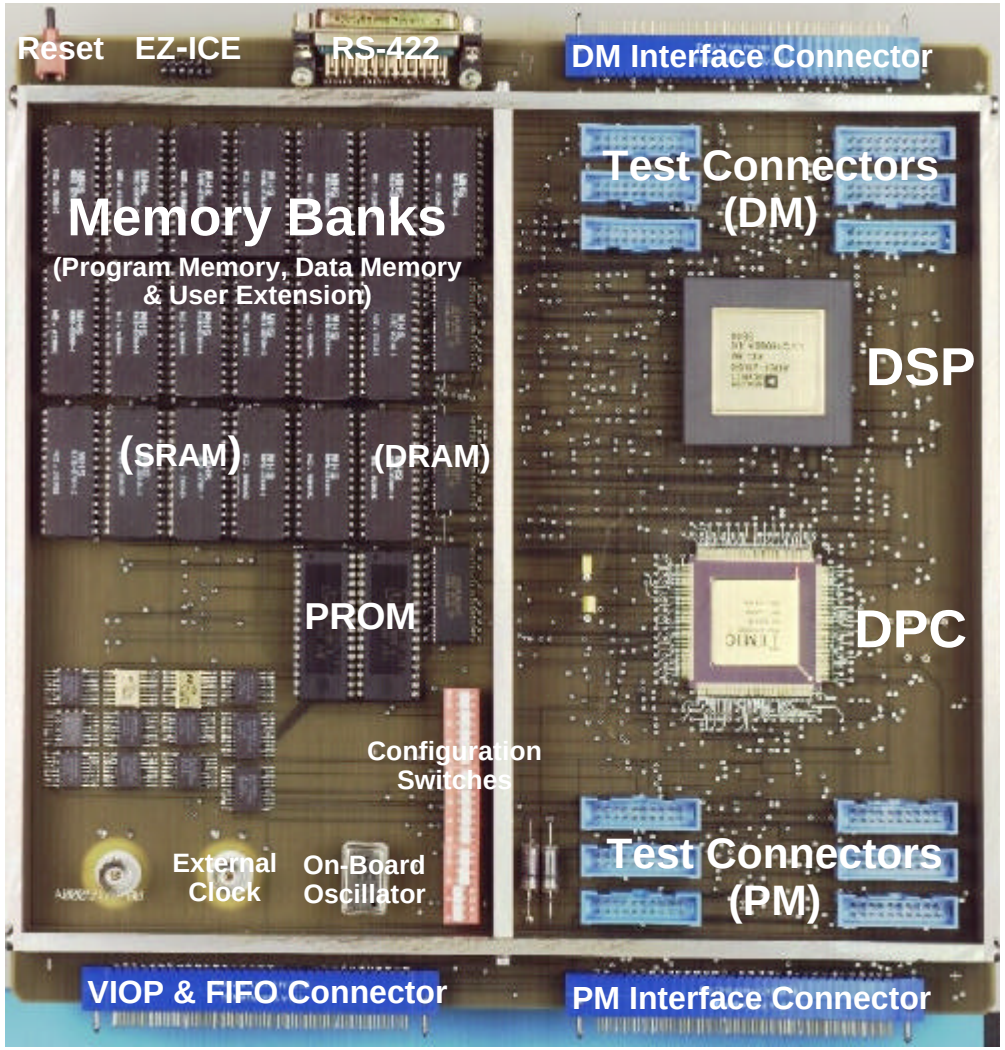
- Place: high cell density, new FIFO cells designed
- Routing : latches setup and hold and fine adjustment between internal clock and DSP clock made by hand.
- Static tests : Static consumption => FIFOs cells problem (pull-up)
- Debug :
  - system Resets due to FIFOs errors during read accesses => no sufficient test coverage with galopping 0 and 1
  - PLL => jitter not OK with design environment => not usable

DPC Test board features

- A DPC Test board has been developped for :
  - Rapid prototyping
  - DPC evaluation
  - Software development
- The DPC board implements :
  - The DPC Asic
  - The DSP 21020
  - SRAM and DRAM Memory (Program, Data and User)
  - The EZ-ICE interface for software development
  - Test points for complete observation
  - IO connectors (RS422, FIFO, etc…)

DPC Test board





Validation results (1/2)

Functional Limitations

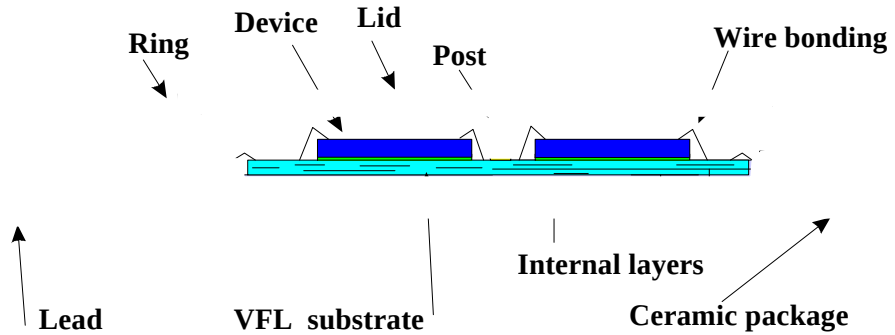
- Serial Input Link 0 frequency must be comprised between f and f/2 (f is the ClkOut Clock frequency). No work around. DPC specification modification
- For Serial Output Link frequency definition, either Scaler or Prescaler may be used (with the other programmed to 1) but not both. So frequency may be comprised between f and f/256. No work around. DPC specification modification
- EDAC and parity protection can not be mixed on Data Memory Interface. A hardware work around exists
- DR flag can not be reset in UARTStatusReg as specified. A work around exists. DPC specification modification
- The PLL is not usable. It is necessary to use external oscillators with high frequency (x4). This decreases a bit the system performance and imposes a load capacitors comprised between 50 (recommended) and 100 pF on ClkOut output pin

Validation results (2/2)

- Characterisation results
  - 20 MHz with DRAM (room temperature and nominal voltage)
  - 20 MHz with SRAM (room temperature and nominal voltage)
  - 14 MHz with DRAM (extreme temperature and voltage)
  - 14 MHz with SRAM (extreme temperature and voltage)
- Power consumption
  - 1.6 W

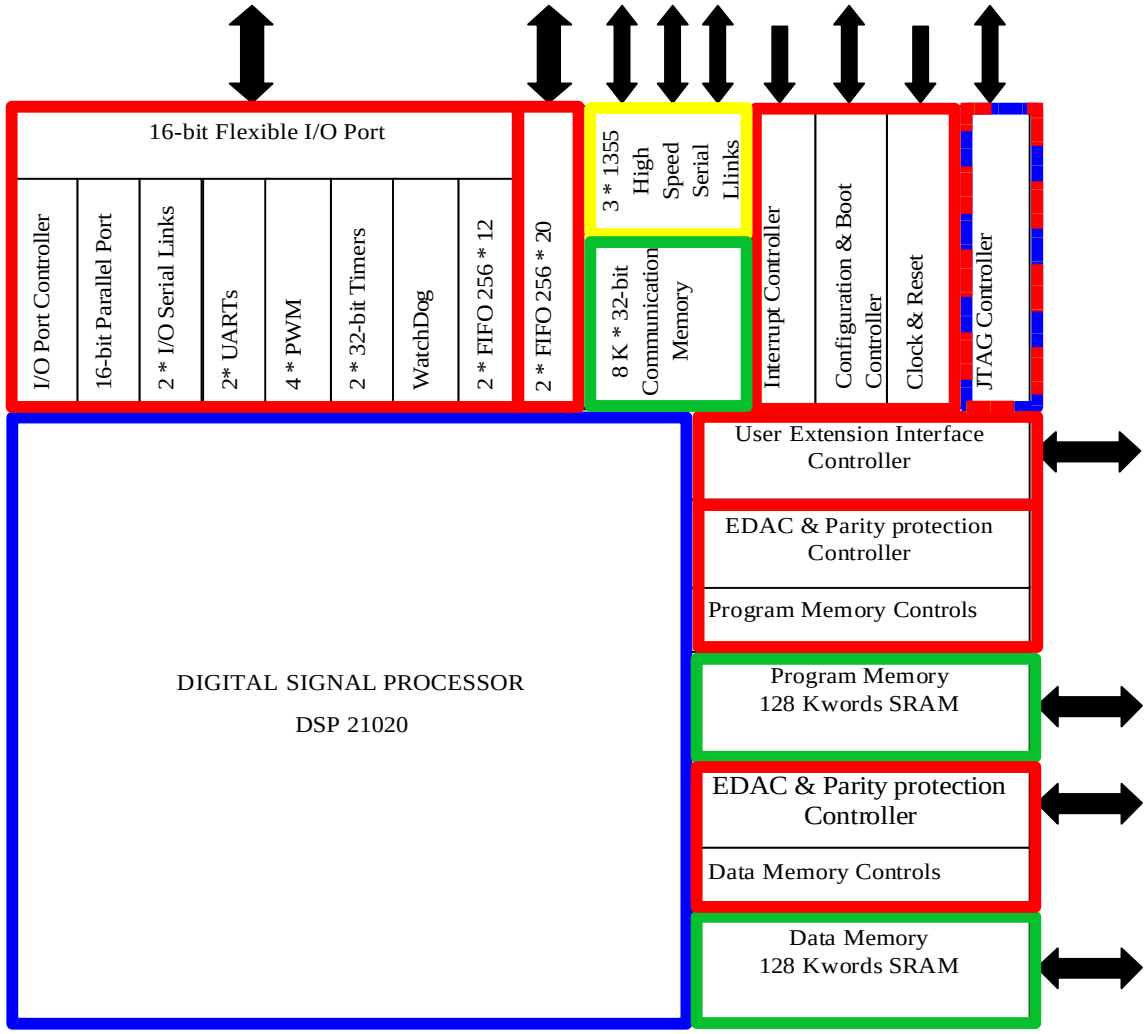
Application : MCM DSP (Multi Chip Module)

- **Space Application requires :**
  - Very high integration level (weight and volume reduction)
  - Adaptation to critical environments (thermal, mechanical, EMC, pressure, radiation)
  - Compatibility with the Space qualification needs
  - Procurement cost reduction



- **The Multi Chip Module (MCM) Concept**
  - A **substrate** allowing heterogeneous dices assembly and high speed interconnection
  - A **package** protecting the micro electronic function and giving the interconnection with the external environment (PCB,…)
  - A **lid** which hermetically seals the package to avoid the on-earth pollution
  - Enhanced function reliability and optimized electrical performances

MCM DSP Functional Block Diagram



MCM DSP Main technical features (1/2)

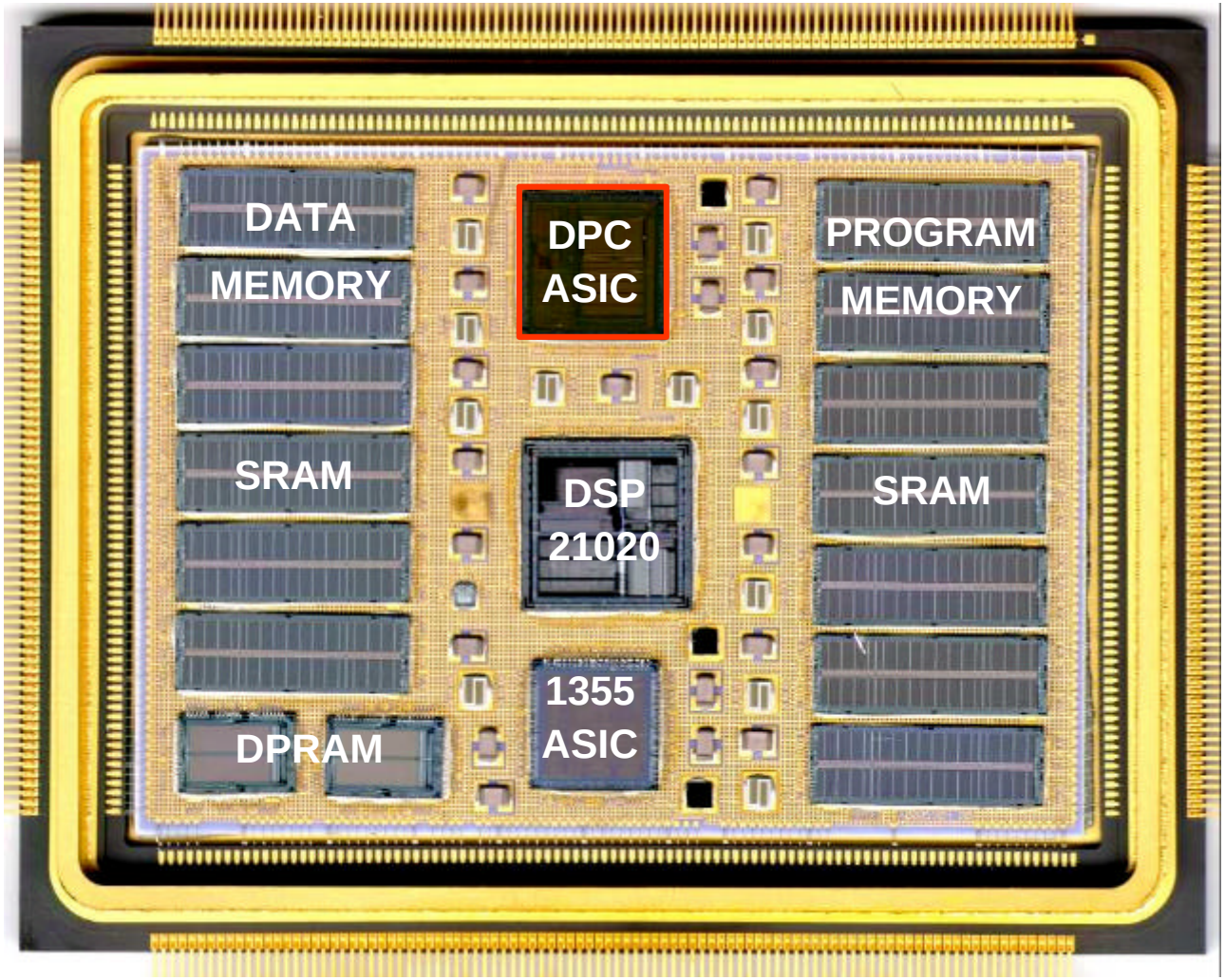
- **The MCM DSP provides the following features :**
  - 128K Words On-module SRAM for both Program and Data Memory
  - SEC/DED EDAC Memory Protection *(*)*
  - Open architecture (User Extension Interface, Versatile I/O port) *(*)*
  - 3 IEEE 1355 High Speed serial links
  - JTAG Interface for Boundary Scan Test
  - JTAG Interface for EZ-ICE In-Circuit emulator connection
  - User Interface providing powerful facilities management (full duplex UARTS, PWG, cascadable timers, watch dog, serial communication links, FIFO, ...) *(*)*
  - Single and multi-processor application programming supported by the VIRTUOSO Real Time Operating System with a standard C environment

(*) DPC features

MCM DSP Main technical features (2/2)

- **Performances :**
  - Performance : 15 MHz / 30 MFLOPS (0 WS) with EDAC protected memories
  - Voltage range : 4.5 to 5.5 V
  - Temperature range : -55 to +125 °C
  - Power consumption : 6 W typical
  - Reliability better than 100 FITs
- **Technology :**
  - Radiation tolerance better than 50 Krads (SI)
  - Latch-Up immunity better than 100 Mev
  - SEU LET threshold better than 25 Mev/cm²/mg
  - Implementation through the MCM-C/D technology

MCM DSP Product Implementation

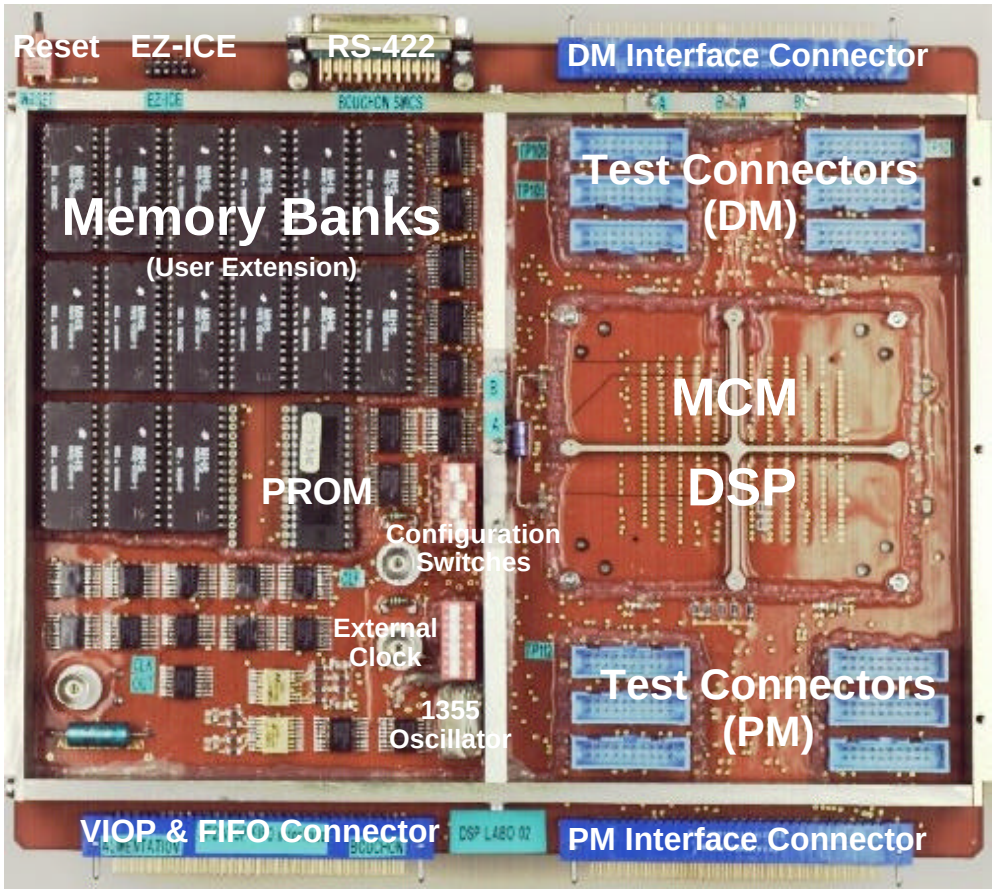


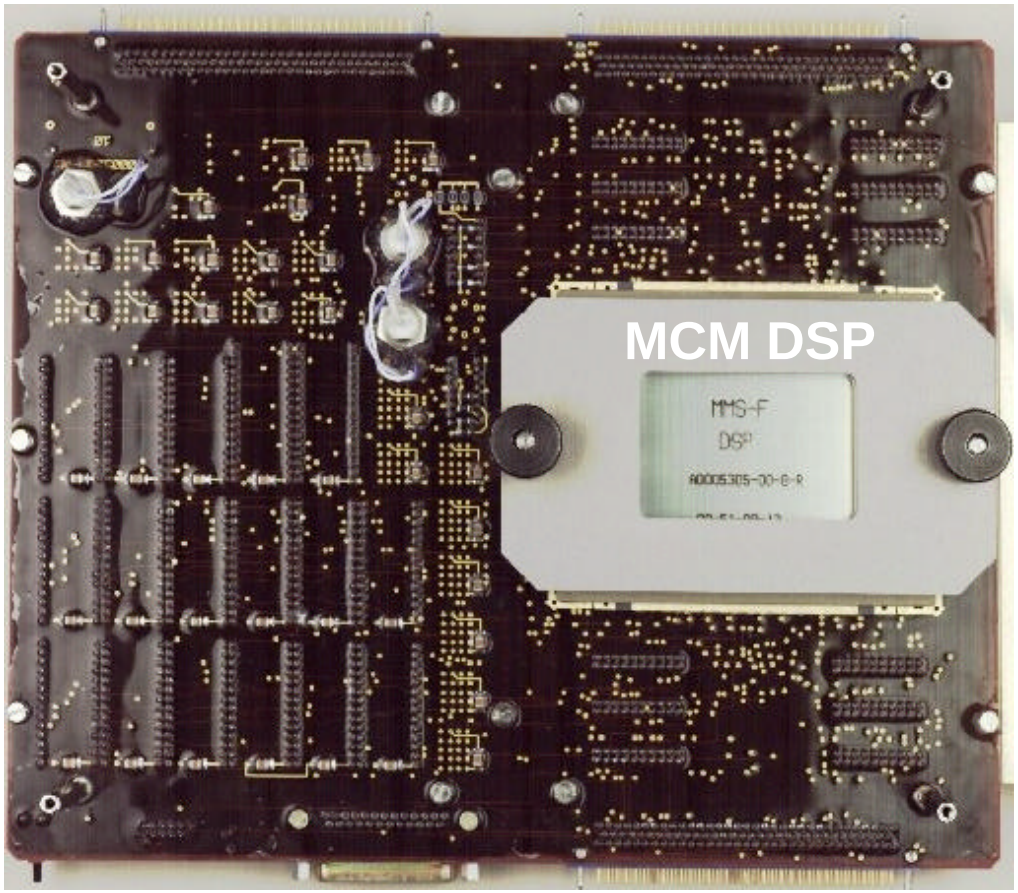
MCM DSP Test board features

- An MCM DSP board has been developped for :
  - Rapid prototyping
  - Software evaluation
  - Software development

- The DSP board implements :
  - The MCM DSP
  - 40k words SRAM for User Applications
  - The EZ-ICE interface for software development
  - Test points for Program Memory and Data Memory observation
  - IO connectors (RS422, 1355 links, FIFO, etc…)

MCM DSP Test board





MCM DSP Validation results

- **MCM DSP electrical characterization completed since 05/99 :**
  - **23 MHz / -55°C / 5V with EDAC protected memories**
  - **16 MHz / +135°C / 5V with EDAC protected memories**

- **Guaranted product performances :**
  - **15 MHz / -55°C to +85°C with VDD > 5V and EDAC protected memories**
  - **14 MHz / -55°C to +85°C with VDD < 5V and EDAC protected memories**

- **Power consumption :**
  - **7 W**

DPC ASIC Assessment and availability

- The DPC ASIC is available from ATMEL Wireless & µC under the product reference T7904E

- DPC Data Sheet can be downloaded from Atmel Web Site

  http://www.atmel-wm.com/products/gab_prod_card.php3

MCM DSP Assessment and availability

- MCM DSP21020F is available of-the-shelf from Astrium
- MCM DSP Validation Board is available of-the-shelf
- MCM DSP VIRTUOSO Board support package is available of-the-shelf
- The MCM DSP Documentation can be requested at the following addresses

pierre-eric.berthet@astrium-space.com

jean-luc.poupat@astrium-space.com

User Base and Applications

- **SAAB : ROSETTA Solid State Mass Memory Controller**
  - EM characterization and EQM qualification successfully completed
- **CRISA : ROSETTA Camera and Star Tracker Instrument Command & Control Terminal**
  - EM characterization successfully completed, EQM qualification in progress
- **ASTRIUM : INMARSAT 4 Digital Payload Processor Unit Controller (OCTM Board with 8 MCM DSP)**
  - EM characterization in progress
- **ALCATEL : Video Chain Signal Processor (image processing & compression)**
  - EM characterization successfully completed, EQM qualification in progress
- **NASA (Jet Propulsion Laboratory) : Scattometer Instrument Data Processor (3 MCM DSP in parallel)**
  - EM characterization in progress

Conclusion

- **Conclusion**
  - **The DPC ASIC and the MCM DSP are available on the market place since 1Q2000.**

- **Many Thanks for their fruitful cooperation and support on this product development :**
  - **M. Sandi HABINC, ESTEC**
  - **Mrs. Françoise BEGHIN, ATMEL Wireless & µC**
  - **M. Michel PORCHER, ATMEL Wireless & µC**
  - **M. Dominique DE SAINT ROMAN, ATMEL Wireless & µC**
  - **The MCM DSP First Users**