Overview

- Introduction
- History
- Project and results
- Applications
  - HIFI
  - SMOG
  - Marshal
- Current development
- Future
  - MOST
  - HIFI
Radiometers

Mixer: 1-2 diodes
Multiplier: 1-2 diodes
Cold LNA: 1-Transistors
IF amp: 10-100 Transistors
Spectrometer: 10-100 M Transistors
Introduction

✧ **Main use:**
  ✓ Autocorrelation spectrometers is used as radiometer back-ends
    » aeronomy
    » radio astronomy
  ✓ Based on time sampling with 1-2 bit encoding precision
  ✓ The coarse sampling leads to 75-95% efficiency, if the signal is noise dominated

✧ **Device**
  ✓ Two main parts of the core
    » quantisation device, ADC type
    » correlator, signal processor
Autocorrelation basics

Wiener-Khintchines theorem;

\[ S(\omega) = \int R(\tau) e^{-j\omega t} d\tau \]

- \( S(\omega) \) = power spectrum
- \( R(\tau) \) = autocorrelation function
The correlator ASICs are 6x6 mm, the IQ samplers 1x1.5 mm, the total modules perhaps 20x50 mm each.

128-1024 channels over 2 GHz BW = 16-2 MHz resolution

in terms of power consumption, each module consumes about 500 mW, + the correlator power of 2 mW/channel used, between 750-2500 mW.
History

- **Sander Weinreb (MIT)**
  - invents the autocorrelation 1960-63, 1-bit
  - finds the first interstellar radio line, OH
- **Basic development**
  - Work with 1, 1.5, 2 bits etc at 1970 + (Cooper etc)
  - basic signal processing
- **Last decade**
  - 1990 state-of-the-art was: 16 channels, 50 MHz and 1 W.
  - A. Emrich introduced total power extraction from autocorrelation data at 1990
Omnisys

- **Omnisys introduced quantisation correction based on real time data 1997**
  - ✓ removed non linearity that has been a problem area during the last decade
  - ✓ simplified design
  - ✓ used for ODIN

- **Omnisys made the first full custom quantiser and correlator ASIC chip-set 1995 - 1998**
  - ✓ 15 GHz Ft Bipolar quantiser
  - ✓ 0.6 um radition tolerant correlator core: 96 channels, 224 MHz sampling, 400 mW
  - ✓ the first chip-set using time multiplexed, TM2, signal processing
    - » reduce power consumption and / or
    - » increase clock speed
Omnisys with ESA funding

- **Design study**
- **Chip-set development**
  - two quantisers
    - real time sampling
    - complex sampling (on Omnisys funding)
  - correlator chip
    - real and complex mode
    - time multiplexing factor of 4
    - 1.3 GHz effective clock rate
- **In parallel (without ESA funding)**
  - signal processing with correction of amplitude and phase errors, based on real time data
  - greatly simplifies the analog/RF design
Current Status

**Spectrometer:**

- ODIN can be considered Omnisys generation II
- The 98-99 project was generation III
  - 0.5 um CMOS / 20 GHz Ft on Bipolar
  - 256 channel / 500 MHz BW chips
  - 4 GHz / 2048 channels = 12 W / 170x11x30 mm
- Designing generation IV of chip set now
  - 0.25 um CMOS / 25 GHz Ft on Bipolar
  - 1 GHz bandwidth specification, 2 GHz likely
  - two chips, one 128 ch and one 1024 channels, but with partial shutdown
- Basic Concept exist that will be used in the future
  - but improvements expected
  - technology and architecture must be optimised
  - 0.18 um and 2000+ channels straightforward
Quantiserr introduction

- **Three designs**
  - Real quantizer, Complex quantizer, 2 channel mixer

- **Chip design and simulation:**
  - Stefan Andersson, Omnisys
  - Michael Wang, KTH
  - Saleh Osman, KTH and Ericsson

- **Process:**
  - Ericsson P71 Bipolar technology
  - NPN minimum size 0.6 x 3 um, ft = 25GHz
  - Resistors 100 and 500 Ohm/square
  - 4 metal layers
  - trench isolation
Complex ADC block

DIV 1, 2, 4, 8
DIV select
LO2
DIV 1, 2, 4, 8
DIV2
1D1
1D2
2D1
2D2
CLK
CLK
DIV select
Real ADC block

- DIV 1, 2, 4, 8
- DIV select
- LO2
- ADC
- DIV 1, 2, 4, 8
- DIV2
- DIV2
- D1
- D3
- D2
- D4
- CLK
- DIV select
Mixer block

Being prototyped on Omnisys budget

- **RF interface**
  - Input frequency: 1-6 GHz
  - Input return loss: <-15 dB (50 ohm system)

- **LO1 interface**
  - Input frequency: 1-6 GHz
  - Input level: -16 to -10 dBm
  - Input return loss: <-15 dB (50 ohm system)

- **IF interface**
  - Buffered differential output
  - Output impedance: TBD (very low)
  - Bandwidth: 0-750 MHz
  - Conversion gain: 15 dB (0 dBm/GHz output)
  - Output power: +7 dBm @ 1dB compression
  - Conversion slope: 0.5 dB/GHz
ADC performance

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>3.3V</td>
</tr>
<tr>
<td>Current consumption</td>
<td>89mA Real, 91mA complex</td>
</tr>
<tr>
<td>max voltage</td>
<td>9V</td>
</tr>
<tr>
<td>min voltage</td>
<td>2.8V</td>
</tr>
<tr>
<td>Out rise/fall time</td>
<td>350ps</td>
</tr>
<tr>
<td>Ref voltage</td>
<td>1.23V</td>
</tr>
<tr>
<td>Voltage swing</td>
<td>min 500mV</td>
</tr>
<tr>
<td>Input frequency</td>
<td>850 MHz</td>
</tr>
<tr>
<td>Input level max</td>
<td>1Vp-p @ Vcc-1V</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>2.3GHz</td>
</tr>
<tr>
<td>Clock level</td>
<td>150 - 400 mVp-p @ Vcc-0.2 - Vcc-1.5V</td>
</tr>
<tr>
<td>Input sensitivity</td>
<td>1mV</td>
</tr>
<tr>
<td>Die size complex</td>
<td>1900 x 1450 um²</td>
</tr>
<tr>
<td>Die size real</td>
<td>2050 x 1750 um²</td>
</tr>
</tbody>
</table>
Complex layout
ADC to CORR interface simulations

<table>
<thead>
<tr>
<th>V(CMOSOUT)</th>
<th>V(IN)</th>
<th>V(LSOUT)</th>
<th>V(REFOUT)</th>
<th>V(CMOSINT)</th>
<th>V(N_16)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Transient analysis: adcdrv.nsx ; all ; 3/7/98 ; 8:29:30

Scaling:
- 4n
- 8n
- 12n
- 16n
- 20n
- 24n
- 28n
- 32n
- 36n
- 40n
- 44n
- 48n

Voltage levels:
- 2V
- 3V
- 2.5V
- 3.2V
- 3.6V
- 4V
- 4.4V
- 2.6V
- 2.8V
- 3V
- 3.5V
- 4V
- 4.5V
- 2.8V
Complex ADC Specification

**General**
Quantisation. Tree level
Demultiplexing factor. Two
LO division factors. Selectable 1,2,4,8 times

**Signal Input**
Single-ended input with separate reference lines for the two quantisation levels.
Sampling rate >1.5Gs/s
Input bandwidth >750 MHz
Input impedance TBD
Input common mode level. TBD
Quantisation levels. Vcom ± 250 mV
Input slope <0.5 dB/GHz
Input offset. < 1mV
Input offset drift. < 100nV / °C
Input bias current. <10 uA
Input offset current <1uA
Complex ADC Performance
Mixer Block

**RF interface**
- Input frequency: 1-6 GHz
- Input return loss: <-15 dB (50 ohm system)

**LO1 interface**
- Input frequency: 1-6 GHz
- Input level: -16 to -10 dBm
- Input return loss: <-15 dB (50 ohm system)

**IF interface**
- Buffered differential output
- Output impedance: TBD (very low)
- Bandwidth: 0-750 MHz
- Conversion gain: 15 dB (0 dBm/GHz output)
- Output power: +7 dBm @ 1dB compression
- Conversion slope: 0.5 dB/GHz
Mixer Preliminary Simulations
Correlator Chip

- 7240µm by 8240µm
- 256 TM 2 complex channels
  - $\times 4 = 1024$ channels
- Effective clock: 1280 MHz
  - $/ 4 = 320$ MHz
- Power = 3-4 mW/GHz/ch
  - depending on data
  - depending on Vcc
  - could be reduced
- 327680 MIPS
<table>
<thead>
<tr>
<th></th>
<th>mW</th>
<th>#</th>
<th>GHz</th>
<th>mW/#/GHz</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bos</td>
<td>1000</td>
<td>16</td>
<td>0.05</td>
<td>1250</td>
<td>used for &quot;comparison&quot; several times</td>
</tr>
<tr>
<td>Omnisys-ODIN</td>
<td>400</td>
<td>96</td>
<td>0.224</td>
<td>18.60119</td>
<td>works in space</td>
</tr>
<tr>
<td><strong>Omnisys&amp;ESA: A</strong></td>
<td><strong>1100</strong></td>
<td><strong>256</strong></td>
<td><strong>1.3</strong></td>
<td><strong>3.305288</strong></td>
<td>presented now, could be updated</td>
</tr>
<tr>
<td>Omnisys&amp;ESA: B</td>
<td>133</td>
<td>128</td>
<td>2.2</td>
<td>0.472301</td>
<td>simulated, will be tested shortly</td>
</tr>
<tr>
<td>Omnisys&amp;ESA: C</td>
<td>1000</td>
<td>1024</td>
<td>2.2</td>
<td>0.443892</td>
<td>design during spring</td>
</tr>
</tbody>
</table>
Demonstrator top
Demonstrator bottom
Test set-up
Real data
100 MHz
768 ch
“strong” signal
Applications

- **ODIN**: flying and working
- **SMOG**: was planned for SMART-1, but not selected
- **Marshal**: plans exist
- **Master**: prototype exist
- **FIRST / HIFI**: planned but rejected ?!
- **MOST**: plans just started
ODIN Spectrometer

- 100-800 MHz bandwidth in steps
- 0.13-1.1 MHz resolution
- 12 W
- Full custom ADC ASIC
- Full custom Correlator ASIC
- MCM-L SSB subsystem at 4 GHz
- MCM-L correlator module, 8 ADC + 8 correlator chips
- 6-Way input mux
- 16-bit CPU controller
ODIN Spectrometer (QM)

100 mm

80 mm

100 mm
"First light" : ODIN data

These are from 5-10 days after launch, cryo etc. not turned on. All Omnisys subsystems function in tested modes.
Omnisys ODIN subsystem examples

Frequency generation and LO phase-lock for four submillimeter front-ends

Complete spectrometer

Control electronics for LO-blocks
SMOG

- mission: find O2
- Swedish - Finnish - ESTEC project
- SMART-1 payload
Basic trade-off

- **The basic specification is:**
  - 2x100 MHz + 1x100 MHz total bandwidth
    *(possible requirement 2x2x100 MHz)*
  - Spectral resolution 200 kHz minimum, 150 kHz desirable
  - Total power variation, ±3 dB (TBD)
  - Total Power level (TBD)

- **Options**
  - Real or Complex
  - Number of chips

- **Inputs**
  - One or two IF
Test for Master (and others ?)

Something useable is being developped
- 4 GHz : 2000 channel design
- based on chip-set described
- funding now from SNSB and Omnisys

funding from ESA for use on Marshal ?

2-6 GHz IF input (or 4-8 GHz)

1 kg, 12 W
FIRST HIFI HRS

- Accept 4-12 GHz input
- 4 inputs, each covering the full band
- No external slope compensation
- 4 x 250 MHz, 4 x 2048 channel nominal mode
- In addition
  - high resolution mode
  - wide bandwidth mode
- 28 V regulated bus input
- ”simple” serial bus for HSK and command
- ”simple” serial bus TBD for data
HRS block diagram

- 4x IF-processors
- 4x IQ converters
- 4x 0.25 GHz, 4x 2048 channels complex correlator
- Power and Power conditioning
- Control Housekeeping and Communication
MOST (Aeronomy)

- Integrated instrument
- 4-8 x 8 GHz back-end
- production of 4-8 times data
- differential measurements
- 8 front-ends at 320/360 GHz
- a few kgs
- 45 W
- on-board, near real-time signal processing (Linux ?)

Interfaces
- one power (with redundancy)
- one data (with redundancy)
- 1-2 mechanical / thermal
MOST

LO with integrated test source

Prime and redundant, serial star network

320 GHz

8-16 GHz

4-8 GHz

LO generation: 4 W x 2

LO gen

Test and debugg port

Prime controller
32 bit CPU, 16 Mbyte Flash, 128 Mbyte DRAM

Cold controller
32 bit CPU, 16 Mbyte Flash, 128 Mbyte DRAM

Control CPU: 2 W x 1

FE: 0.1 W x 8

IF system: 1 W x 4

Spectrometer: 6 W x 4

Filtered, regulated and protected 5 V (TBD) power bus

1+1 data I/O

1+1 Power I/O

43 W

LO gen

OMNISYS INSTRUMENTS

one optical interface

one mechanical interface
Current Project overview

- Chip Scale Packaging (CSP).
- High frequency, low resolution ADC/Sampler: 1.5 bit, goal for the sampling frequency is 2.2 GHz (4+ GHz measured).
- Wideband low resolution spectrometer: goal for the sampling frequency is 2.2 GHz. (4 GHz hoped for)
- Narrowband, high resolution spectrometer: sampling frequency is 2.2 GHz, 1024 channels
- Radiation Tests
- Design of a breadboard and test-setup
Work

- The MASTER, SOPRANO and FIRST technical will be reviewed and an evaluation of possible chip implementations will be made.

- **Chip Scale Packaging:** CSP is a technology offering the well known advantages of a packaged device as compared to naked die. High packaging density is maintained, which is comparable to a naked die implementation on MCM, however the drawbacks due to the KGD problem are avoided.

- **High Frequency, Low Resolution ADC/Sampler:** Further increase of integration density could be achieved if the high frequency, low resolution ADC(s)/samplers were integrated on the same die / package as the correlator.

- **Wideband, Low Resolution Spectrometer:**
  Goal for the sampling frequency is 2.2 GHz (TBC). Emphasis for this chip is the largest possible bandwidth.

- **Wideband, High Resolution Spectrometer:**
  The number of correlator channels: 1024
CSP

- traditional integrated circuit packages has become more and more a limiting factor
- use of MCM technology based on naked die has still a lot of drawbacks.
- KNG (Known Good Die) issue which includes the problem of both testing the chips under realistic conditions as well as the problem of screening, burn-in etc.
- CSP (Chip Scale Packaging) has come up as a solution to these problems. The concept is to provide a package that increase the size of the naked die with only 30-50 %, while traditional packages often are 1000 % bigger than the die.
- added parasitics will be an order of magnitude less than with most traditional packages.
CSP design

- The design is based on a two sided PCB
- 75 um track width and spacing, also using padless vias.
- The PCB is then 15x15 mm and 0.5 mm thick.
- The design has all “bumps” in a ring around the chip, except for the grounding, where 16 bumps are situated in the middle.
- The top of the chip is then “globbed”, i.e. epoxy or silicon based material is applied for physical protection.
Test board
IQ converter

- Baseline: single chip / package spectrometer core
- Design solution:
  - Bipolar IQ converter in same package as CMOS correlator
- Design
  - 1.5 bit I and Q converter
  - 2.2 GHz effective sample rate (8 GHz simulated !!)
- Compared to previous designs
  - Half the power consumption
  - 3-4 times the speed
- Tested with 4 GHz + speed
IQ converter

In 1 Ref 1

Ref 2 In 2

In 3 Ref 3

Ref 4 In 4

Clk nClk

Pre-Amp

Pre-Amp

Pre-Amp

Pre-Amp

Pre-Scaler /1,2,4,8 S1, S2

Div-2

Flip-Flop

Flip-Flop

Flip-Flop

Flip-Flop

Latch

Latch

Latch

Latch

Buffer

Buffer

Buffer

Buffer

Buffer

Out 1-1

Out 1-2

Out 2-1

Out 2-2

Data ref.

Out 3-1

Out 3-2

Out 4-1

Out 4-2

Clkout nClkout

Div Select
<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>2.2-2.8 V</td>
</tr>
<tr>
<td>Spec</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Current consumption</td>
<td>75 mA</td>
</tr>
<tr>
<td>Output swing</td>
<td>&gt; 350 mV</td>
</tr>
<tr>
<td>Spec</td>
<td>differential</td>
</tr>
<tr>
<td>Input frequency</td>
<td>2 GHz</td>
</tr>
<tr>
<td>Spec</td>
<td>750 MHz</td>
</tr>
<tr>
<td>Input dynamic range</td>
<td>1700 mV to Vcc</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>4 GHz</td>
</tr>
<tr>
<td>Spec</td>
<td>1.1 GHz</td>
</tr>
<tr>
<td>Clock swing</td>
<td>2-800 mV</td>
</tr>
<tr>
<td>Spec</td>
<td>differential</td>
</tr>
<tr>
<td>Select signal high min.</td>
<td>Vcc-0.1 V</td>
</tr>
<tr>
<td>Spec</td>
<td>-</td>
</tr>
<tr>
<td>Select signal low max.</td>
<td>Vcc-0.5 V</td>
</tr>
<tr>
<td>Spec</td>
<td>-</td>
</tr>
<tr>
<td>Clock division factor</td>
<td>1, 2, 4, 8</td>
</tr>
<tr>
<td>Input sensitivity</td>
<td>&lt; 1 mV</td>
</tr>
</tbody>
</table>
The input data $Z$, is time division multiplexed (TDM) into two parallel complex data streams $Z_C^0$ to $Z_C^1$ each consisting of a real and imaginary part. ($Z_C^m = R_m + jI_m$).

$$Z_m(n) = Z(nT - mT/4)$$

$$Z_C^m(n) = R_m(n) + jI_m(n) = R(nT - mT/2) + jI(nT - mT/2)$$

$$a \cdot b = \begin{cases} 
1 & \text{for } \{a, b\} = \{1, 1\} \text{ or } \{-1, -1\} \\
-1 & \text{for } \{a, b\} = \{1, -1\} \text{ or } \{-1, 1\} \\
0 & \text{otherwise}
\end{cases}$$

$$C(r) = \sum_{n=0}^{M} Z_C(nT/2)^* \cdot Z_C((n-r)T/2)$$

$$= \sum_{n=0}^{M} R(nT/2) \cdot R((n-r)T/2) + \sum_{n=0}^{M} I(nT/2) \cdot I((n-r)T/2)$$

$$+ j \cdot \left[ \sum_{n=0}^{M} R(nT/2) \cdot I((n-r)T/2) - \sum_{n=0}^{M} I(nT/2) \cdot R((n-r)T/2) \right]$$

$$= RR(\tau) + II(\tau) + j[R(\tau) - IR(\tau)]$$
Correlator results

- 128 Channels and 2 x 64 with separate dissable
- Size : 2.5 x 3 mm
- Power :
  - Clock : 550MHz 1GHz
  - input +1/-1: 80mA/200mW 133mA/330mW
  - always 0: 40mA/100mW 67mA/165mW
  - input +1/0/-1: 53mA/133mW 110mA/270mW

- this is with 128 channels