ESA-ESTEC GSTP - Analog Silicon Compiler for Mixed-Signal ASICs

Analog Module Generator Software - AMGIE & MONDRIAAN
Outline

- Introduction
- Objectives of WP1100 & WP1300
- AMGIE
- Hierarchical Cell Design in AMGIE
- Low Power Optimization in AMGIE
- Radiation Tolerant Design
- Yield Optimization
- Mondriaan
- Conclusions
Introduction

- Software development: WP1100 & WP1300
- WP1100: Tool Requirement Analysis
  - ASICs/GVdP/WP1 report
- WP1300: Software Implementation & Verification
  - Updated AMGIE software
  - Mondriaan toolset
  - Software User Manual
Objectives

- **ASTP4 project**: Analog Module Generator (AMG)
  - Targeted to OPAMP level circuits: automatic synthesis from specifications to layout
  - Both for novice and experienced designers

- Extend and improve Analog Module Generator

- Reorient for expert designers
  - High-performance circuits: high-speed A/D converter
  - Toolbox approach

- Radiation tolerance
  - CSA-PSA circuit
Objectives cont’d

- Translate Objectives into Requirements
- Tool Requirement Analysis (ASICs/GVdP/WP1)
  - Hierarchical cell design in AMGIE
  - Low power optimization in AMGIE
  - Radiation tolerant design
  - Yield optimization
  - Mondriaan
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AMGIE: Definitions

Behaviour

Vout := A(V+ - V-)
+constraint specifications:
  Av0 > 60dB
  GBW > 1 MHz ...

Specifications

Topology Selection

Schematic synthesis

Structure

Sizes & Biasing

IB = 10uA
W1 = 10u L1 = 1u
W2 = 12u L2 = 1u
W3 = 18u L3 = 2u

Geometry

Layout Generation

Layout
AMGIE

- Synthesis of OPAMP level complexity circuits
- Design methodology
  - Performance driven
  - Hierarchical
  - Design styles
    - Full custom
    - Fixed
- Cell Library
  - Custom topologies
  - Fixed cells
    - Manual
    - Synthesized
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Hierarchical Cell Design in AMGIE

- Implementation of stubs
- Design Controller
- Sizing & Optimization tool
  ⇒ Specification Translation tool
- Layout tool
  ⇒ Layout Assembly tool
AMGIE: Design Flow

- Top down
- Bottom up
Design Controller

Old Design Flow (ASTP4 AMG)

New Design Flow (GSTP AMGIE)
Hierarchical Cell Design: Sizing Tool

- AMGIE sizing & optimization tool
  - Sizes of devices
  - Biasing of devices

- Hierarchical
  - Sizes of devices
  - Biasing of devices
  - Specifications of subcells
    - Specification translation

- S&O tool
  - Modified data handling
Hierarchical Cell Design: Layout Tool

- LAYLA [Lampaert ‘99]
  - Analog place & route
  - Direct performance driven, analog constraints
    - Symmetry
    - Matching
    - Parasitics
  - Optimized for typical analog circuits
    - OTA
    - Opamp
    - Comparator
    - ...

LAYLA: Miller_p circuit

- Circuit level: fully functional layout
- Module level?
Module Placement & Routing

Specs → Placement
Netlist → Placement
Technology → Placement

Commercial Layout Environments → Placement

Placement → Routing

Routing → Device Generators
Exterior Cells

Improved LAYLA

- External Cells
- Floorplanning with soft cells
- Circuits & Modules:
  - OTAs
  - Comparators
  - CSA, PSA
  - CSA-PSA Module
  - A/D & D/A ?

⇒ Mondriaan
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Low Power Optimization: Problem

- Optimization algorithms
  - Global: Simulated Annealing
  - Local: Hooke-Jeeves
    ⇒ highly constrained problems

- Optimization process
  - Black box
  - Only cost trace is visible
  - Final result can be investigated
  - How to find good cost function parameters?
Low Power Optimization: SQP

- Added **gradient** based optimization algorithm
  - Sequential Quadratic Programming (**SQP**)
  - Active constraint set

![Buffer Diagram]
Example: Power-Area Tradeoff

Power Area Trade-off

- $A_v > 1000, V_{off} < 3 \text{mV}$
- $A_v > 200, V_{off} < 3 \text{mV}$
- $A_v > 200, V_{off} < 10 \text{mV}$

Power [W] vs. Area [$m^2$]
Low Power Optimization: Viewer

- Optiman viewer
  - GUI
  - Control center for optimization
  - Displays state: current and best
  - Optimization trace: history of process
  - Internals optimization process

- Gives control to
  - Experienced users
  - Library developers
OPTiman

Y = f(X_{\text{var}}, X_{\text{fixed}})

\text{opt cost} = g(Y)

s(Y) < 0

1. Start/Pause
2. Stop
3. Pop up Specs Window (A)
4. Pop up fixed X parameters Window (B)
5. Pop up a View Window (C)
6. Pop up a Graph Window (D)
7. Pop up a Trace Window (E)
8. Pop up a Schematic Window (F)
9. Pop up Penalty Window (G)
10. Pop up the Plot Window (H)
11. Make a hardcopy of all windows

logw.m1 = log(w.m1/WMIN)

logl.m1 = log(l.m1/LMIN)

vgst.m1 = vgs.m1-vt.m1

a: \% times violated last 60 evaluations
b: \% times violated last 600 evaluations
c: total \% times violated
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Radiation Tolerant Design

- Problem description

![Diagram of NMOS transistor with labels V_T, n, and M1]
Radiation Tolerant Design

● Counter irradiation effects by design
  ○ Layout measures
  ○ Adapt sizing models: W & L, parasitics

● Verify design
  ○ Commercial simulator
  ○ Irradiation parameters
Edgeless Device – Gate All Around

- Avoid the leakage path!

![Diagram of an edgeless device with labels for Drain, Gate, Source, $W_{eff}$, and $L_{eff}$]
Gate All Around Device

\[
\frac{W_{\text{eff}}}{L_{\text{eff}}} = \frac{8}{\ln\left(\frac{W_2}{W_1}\right)}
\]

\[
\frac{W_2}{W_1} = \exp\left(\frac{8}{\frac{W_{\text{eff}}}{L_{\text{eff}}}}\right)
\]
Device Generator

CADENCE & LAYA
Radiation Tolerant Design: Sizing

● Margins
  - $V_T$ Shifts
  - Leakage currents

● Gate all around device
  - Use geometric model
  - $W$ & $L$
  - Parasitics: AS, AD, PS, PD, NRS, NRD, …
KULeuven PDFE Example

Rf

GAA

CSA

Diff

INT

550um

1.1mm
Radiation Tolerant Design: Verification

- Verification
  - Commercial simulators offer simulation of irradiation effects
  - Hspice has been integrated in the verification tool
  - 2 examples:
    - NMOS transistor
    - Simulated KULeuven PDFE
NMOS Transistor: Subthreshold Slope
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Yield: Problem Description

- **Nominal** Design
- Manufacturing tolerance
  - Inter-die
    - Wafer batches
    - Different wafers in one batch
    - Modeled through spice parameter $6\sigma$ intervals
  - Intra-die
    - Same devices, unequal parameters
    - Mismatch
- **Yield**
  - Some circuits are not within spec
Inter-die Yield Optimization

- simultaneous sizing for nominal performance and yield/robustness
  - automatically derived sensitivities to calculate yield/Cpk during sizing

Inter-die

DONALD

all design equations & variables

input set
(W,L,θ)

SPICE-like computational plan

symbolic derivatives

input set
(θ,L,V_{node},I_{branch})

computational plan to calculate nominal point executable

computational plan to calculate sensitivities executable

by propagation of variances on symbolic model

[Debyser ICCAD98]
**Inter-die Yield Optimization: Example**

- **example**: current-buffer OTA
  - random starting point
  - nominal/yield/Cpk optimization
  - Monte-Carlo verification

<table>
<thead>
<tr>
<th>specs</th>
<th>yield model</th>
<th>Monte Carlo</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>$\bar{y}$</td>
<td>$\sigma_y$</td>
</tr>
<tr>
<td>GBW&gt;100MHz</td>
<td>165</td>
<td>23.1</td>
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<tr>
<td>$A_{v0}$&gt;60dB</td>
<td>78.0</td>
<td>1.68</td>
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<tr>
<td>PM&gt;60deg</td>
<td>60.2</td>
<td>0.2</td>
</tr>
<tr>
<td>OR&gt;3.0V</td>
<td>3.1</td>
<td>0.05</td>
</tr>
<tr>
<td>$V_{off}$&lt;5mV</td>
<td>4.8</td>
<td>0.14</td>
</tr>
<tr>
<td>$I_{tot}$&lt;3.0mA</td>
<td>2.6</td>
<td>0.4</td>
</tr>
</tbody>
</table>

**CPU times**

- Monte Carlo yield model optimization: 2h20’ (300s)
- 10”
- 2h15’
Example: Results

- 1: pdf distributions without yield/Cpk (nominal only)
- 2: pdf distributions with yield/Cpk (nominal + yield)
Intra-die Yield: Mismatch

- A/D converter: INL specification
- MOS mismatch model [Pelgrom JSSC’89]: variance on
  - $V_T$
  - $\beta$

\[
\sigma_{\Delta V_t}^2 = \frac{A_{Vt0}^2}{WL} + S_{Vt0}^2 D^2
\]

\[
\sigma_{\Delta \beta / \beta}^2 = \frac{A_{\Delta \beta / \beta}^2}{WL} + S_{\Delta \beta / \beta}^2 D^2
\]

- Sizing model includes mismatch yield through equations
- Mismatch verification
Mismatch verification: Comparator

\[ V_{\text{in}+}, V_{\text{in}-} \]

\[ M_{1a}, M_{1b} \]

\[ V_{\text{out}+}, V_{\text{out}-} \]

\[ M_{2a}, M_{2b}, M_{3a}, M_{3b}, M_{4a}, M_{4b}, M_{5a}, M_{5b} \]

\[ M_{\text{bias}} \]

\[ \phi_1, \phi_2 \]

\[ I_{\text{dsextra}}, V_{\text{meas}}, \text{rs}, \text{rd}, \text{delv}t = \ldots \]
Transient Simulation

output voltage at a fixed time point

$\Delta V_{out}$

[VdPlas ICECS99]
Result Monte Carlo Simulation

![Histogram of Monte Carlo Simulation Results with a Fit Line](chart.png)
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Mondriaan: Introduction

- Often used analog signal processing architectures: generation, propagation, multiplication

[VdPlas CICC98]
Examples

A/D converter

D/A converter
Generation of Regular Layout Structures

- **Hierarchy**
  - ☹ changes lead to a complete redesign of the cell hierarchy
  - ☹ exceptions difficult to handle

- **Stretch & Tile [Neff]**
  - ☻ extremely fast generation
  - ☹ all connectivity by abutment
  - ☹ large setup time
Mondriaan Features

- Regular array of cells
- Use abutment for power, biasing, ...
- Bus & Channel routing for extra connectivity
  - Y bus routing connects to cells
  - X channel routing connects to Y routing
- Mondriaan Flow
- Bus and Tree device generators
Mondriaan: Layout Model

- Matrix of master cells (master1, master2, ...)
- Optional column spacer cells (sp1, sp2)
Mondriaan: Layout Model

- Symbolic view: X & Y channel routing

contact area

X-Y
Mondriaan Flow

Diagram:
- Cell outline
  - Floorplan Generation
    - Floorplan
      - Routing
        - Routed floorplan
          - Technology Mapping
            - Technology data
              - Cell layout
              - Mask layout
            - Mapping directives
            - Routing directives
          - Netlist

Flowchart:
- Cell outline
  - Floorplan Generation
    - Floorplan
      - Routing
        - Routed floorplan
          - Technology Mapping
            - Technology data
            - Cell layout
            - Mask layout
          - Netlist
          - Routing directives
          - Mapping directives

Example: 4-bit Current Source Array

- 1 current source == 4 MOS transistors
- symmetric placement
- Floorplan

<table>
<thead>
<tr>
<th>1A</th>
<th>2A</th>
<th>0A</th>
<th>3A</th>
<th>5A</th>
<th>6A</th>
<th>6B</th>
<th>5B</th>
<th>4B</th>
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<td>0A</td>
<td>7A</td>
<td>7B</td>
<td>0B</td>
<td>3B</td>
<td>14B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13A</td>
<td>2A</td>
<td>1A</td>
<td>8A</td>
<td>8B</td>
<td>1B</td>
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<td>9C</td>
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<td>11C</td>
<td>12C</td>
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<tr>
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<td>1D</td>
<td>8D</td>
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<td>1C</td>
<td>2C</td>
<td>13C</td>
<td></td>
<td></td>
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<td>3D</td>
<td>0D</td>
<td>7D</td>
<td>7C</td>
<td>0C</td>
<td>3C</td>
<td>14C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>--</td>
<td>4D</td>
<td>5D</td>
<td>6D</td>
<td>6C</td>
<td>5C</td>
<td>4C</td>
<td>--</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Floorplan:

- Each cell represents a MOS transistor.
- Dummies are used to ensure symmetric placement.
- The layout is designed to minimize area and maximize performance.

The table shows the placement of the transistors in a 4-bit current source array, with dummies included for symmetry.
Layout of 4-bit Array
Bus and Tree Generators

Buses

Tree
Bus Generators

- N-to-N connections: 6 types
- Signal distribution, clock distribution, …
Tree Generators

- 1-to-N connections: 3 types
- Clock distribution, biasing, power, ground, ...
14-bit D/A Converter

- DIGITAL CLOCK DRIVER
- ANALOG CLOCK DRIVER
- FULL DECODER
- SWATCH ARRAY
- CURRENT SOURCE ARRAY

Dimensions: 4.1x3.2mm

DAC00
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Conclusions

- Improved AMGIE
  - Hierarchical cell design
  - Low power optimization
  - Yield optimization
- Radiation tolerance
  - GAA
  - Verification
- Mondriaan
  - Layout for A/D converters
Publications


