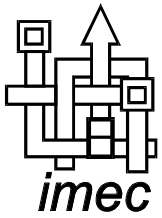
ESA-ESTEC GSTP - Analog Silicon Compiler for Mixed Signal ASICs

Irradiation of CSA-PSA

&

Design of a CMOS High-Speed 8-bit 100MS/S ADC core



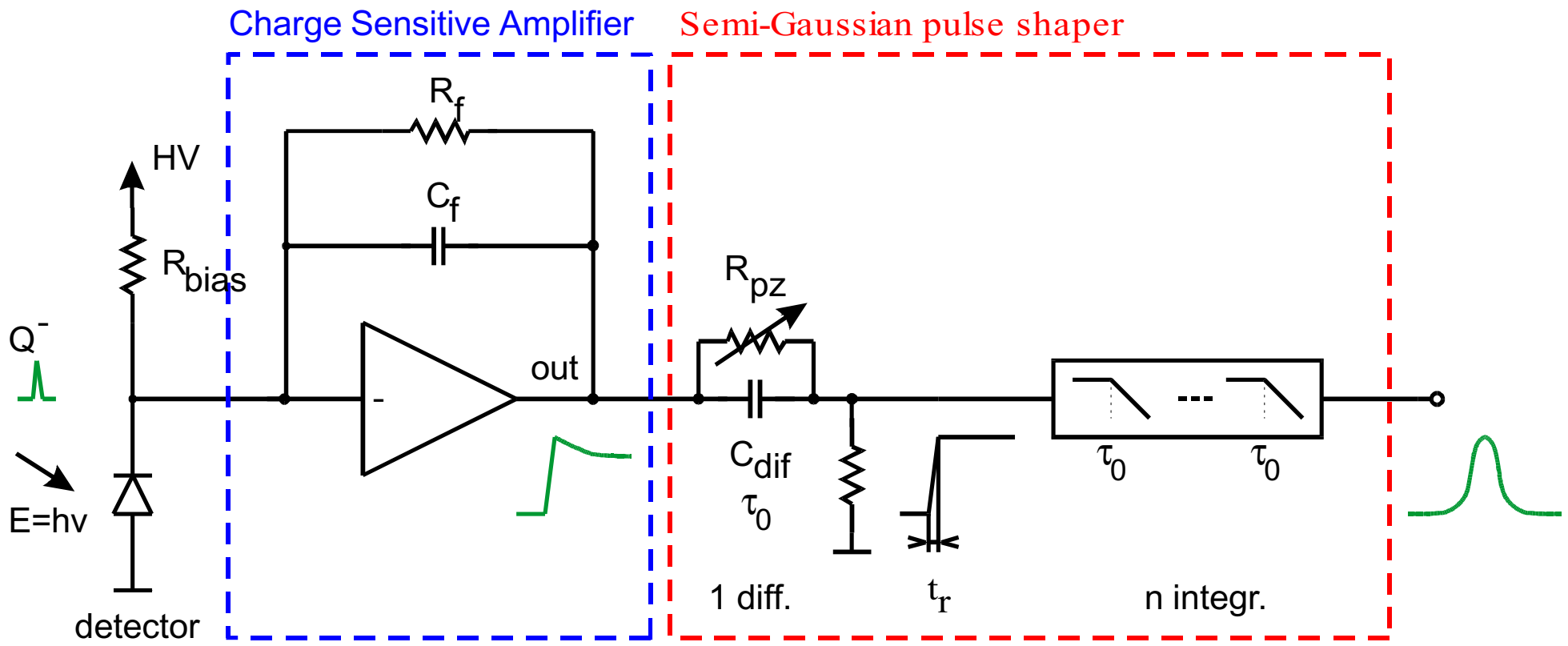
Outline

- Irradiation of CSA-PSA chip [designed and fabricated in ASTP4 project]
  - Objectives
  - Measurement setup
  - Measurements
  - Conclusions
- Design High-Speed 100MS/s 8-bit ADC
  - Objectives
  - Design methodology
  - Architectural level design
  - Device level design
  - Layout
  - Measurements
  - Conclusions

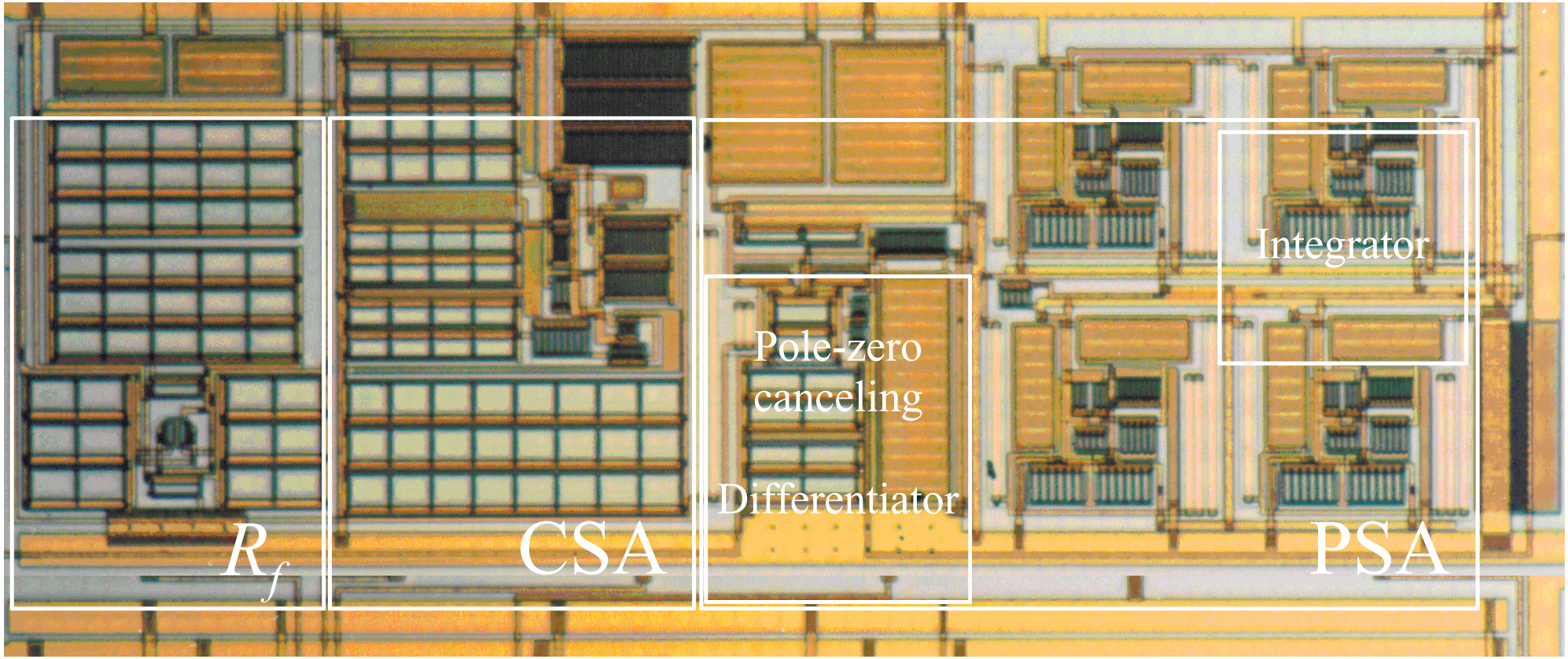
Irradiation CSA-PSA: objectives

- Perform an initial evaluation of the total dose hardness of the commercial 0.7μm CMOS process from MIETEC
  - radiation tolerance evaluation of standard CMOS technology
- Total dose testing on CSA-PSA chip :
  - designed and fabricated in ASTP4 project “VLSI Design Tools-Module generation for analog silicon compilation” with the ESTEC division of the ESA (Contract 9890/92/NL/GS).
- Workpackage
  - WP1200

CSA-PSA: block-diagram



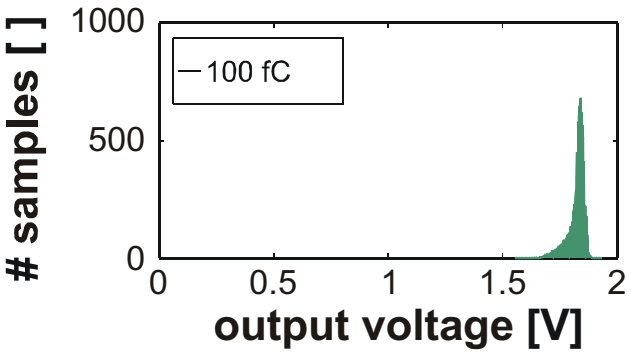
CSA-PSA: micro photograph

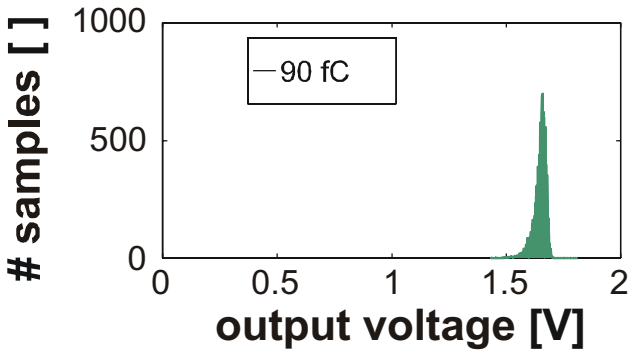


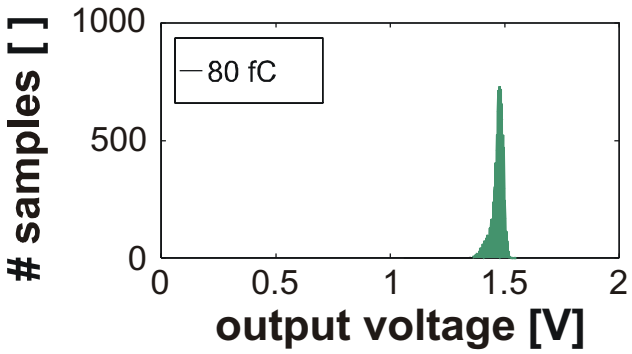
CSA-PSA: measurement setup

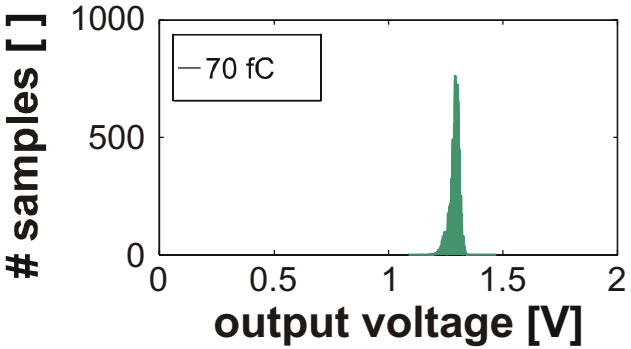
- Compliant with AD3
- Five samples were exposed to 50 krad
- Two of them were afterwards exposed to 100 krad
- Measurements:
  - for good comparison additional noise and linearity measurements were done before irradiating the samples
  - for each sample 11 inputs were applied: varying from 5, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100fC
  - for each input signal a histogram, comprising 30.000 samples, was measured
  - linearity and noise were calculated from histograms

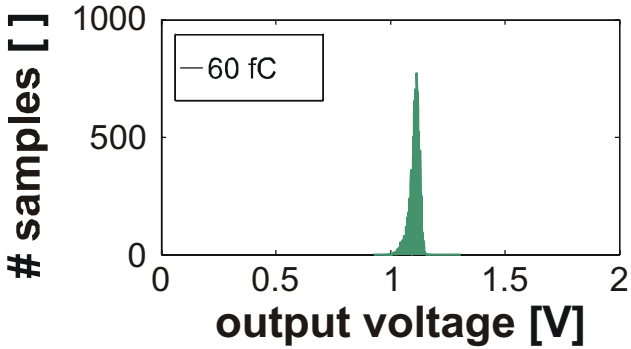
CSA-PSA: measurement results

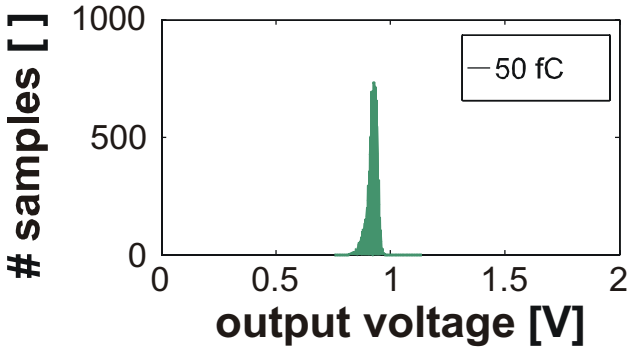




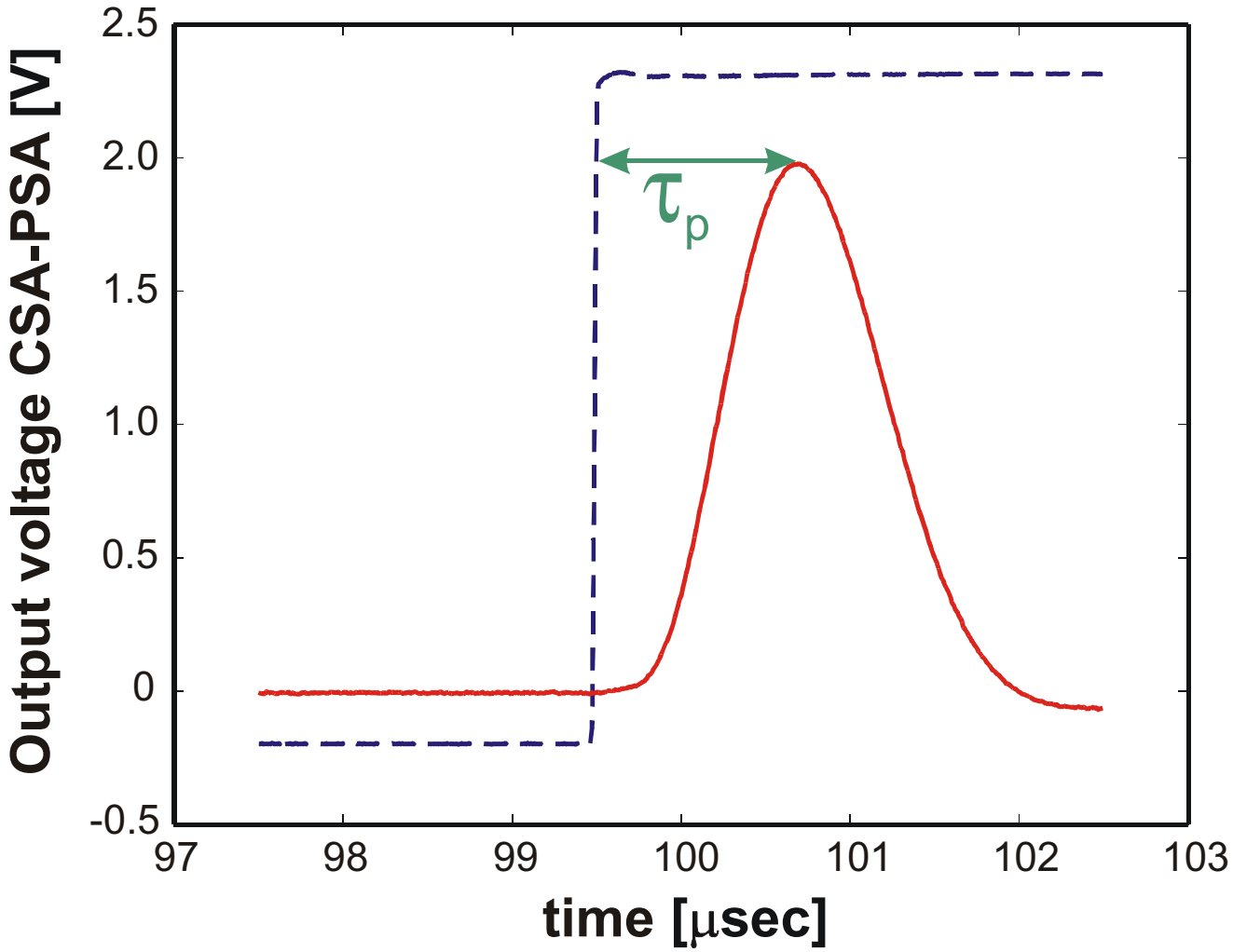






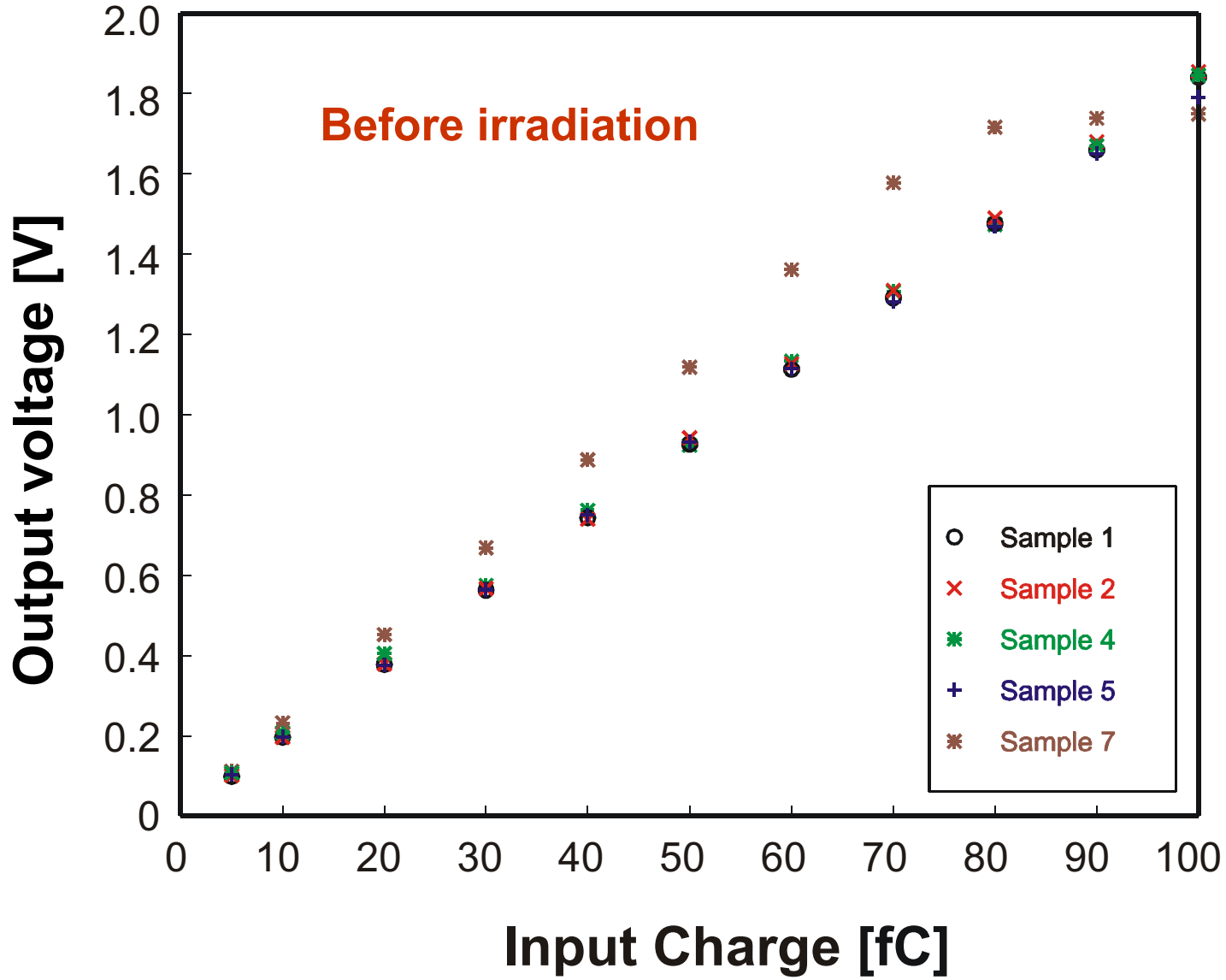


CSA-PSA: measurement results cont'd

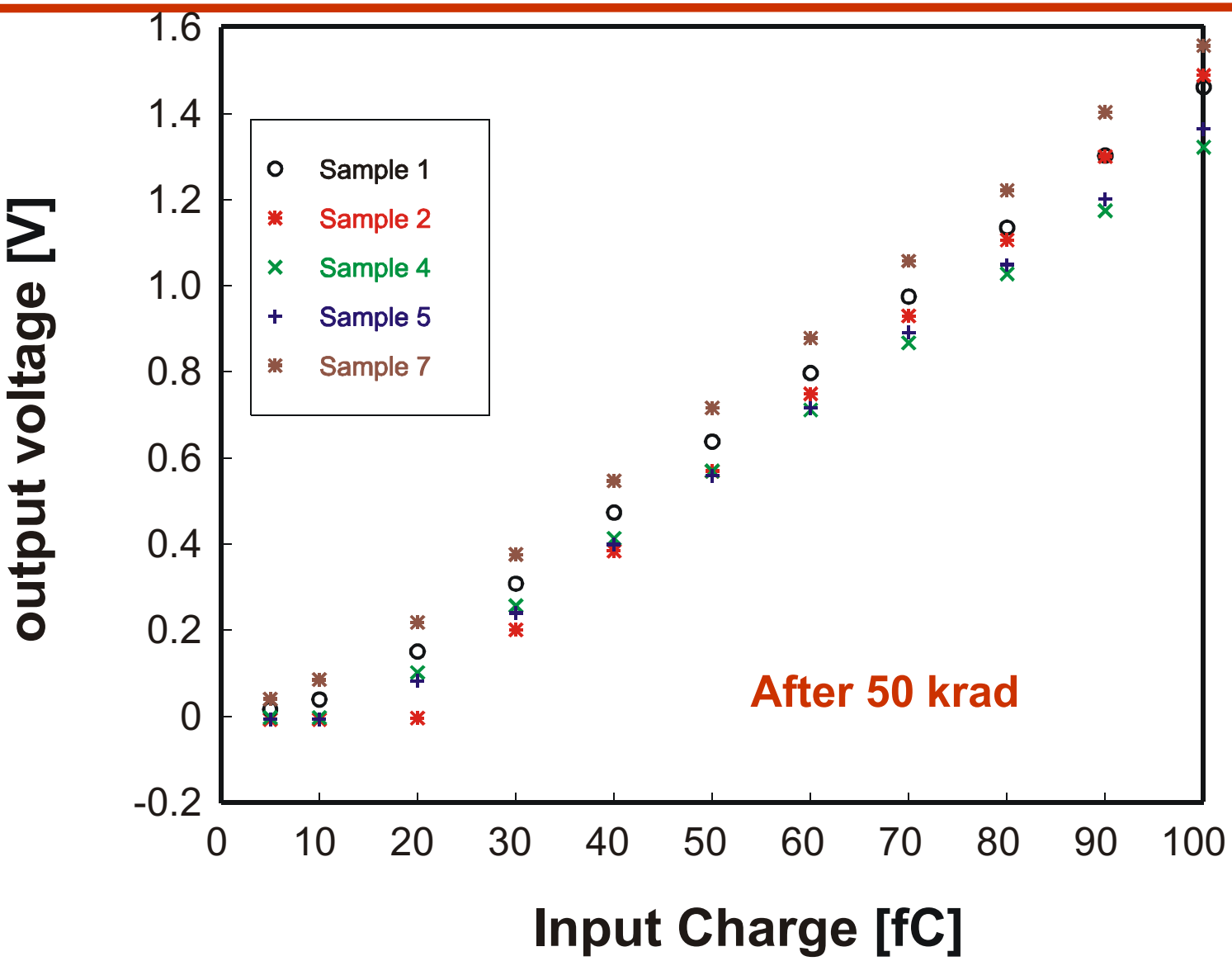


- gain:18mV/fC
- peaking time: 1.14 μs
- noise: 899 e^-RMS
- linearity < 0.5 %

CSA-PSA: measurement results cont'd



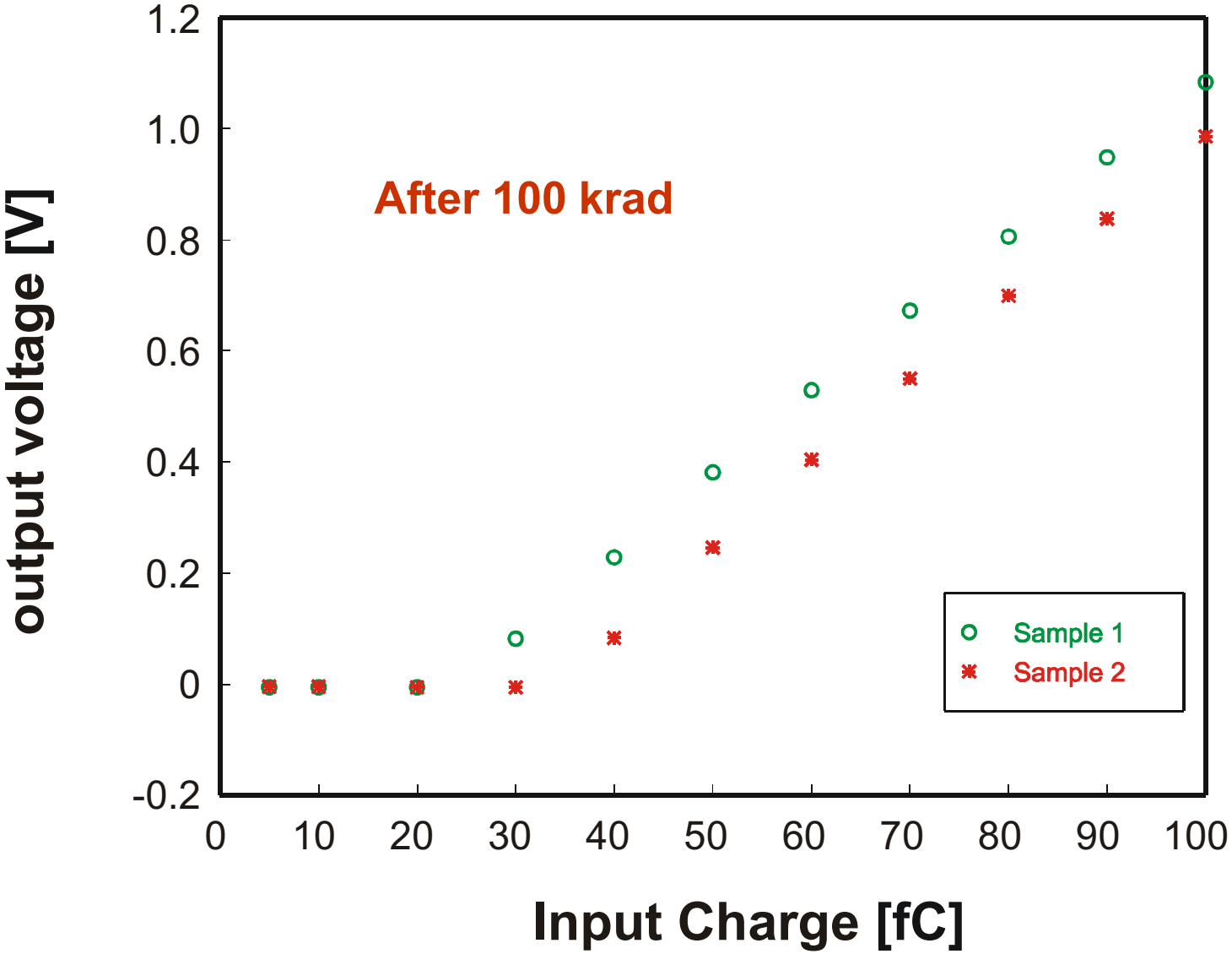
CSA-PSA: measurement results cont'd



CSA-PSA: measurement results cont'd

- After exposure to 50 krad
  - a slight decrease in conversion gain: from 18mV/fC to 16mV/fC
  - the peaking time decreases slightly from 1.14 to 1.17µs
  - the noise level shows little change
- Conclusion 50 krad irradiation
  - all chips survived the irradiation testing of 50 krad quite good
  - only a slight decrease in performance is noticed
  - good recovery after 24 hours
  - full recovery after 168 hours.

CSA-PSA: measurement results cont'd



CSA-PSA: measurement results cont'd

- After exposure to 100 krad
  - a further decrease in performance
  - the conversion gain dropped by a factor of two
  - the peaking time increased from 1.14µs to 1.20µs
  - the noise level increased slightly After 24 hours annealing little recovery was seen, after 168 hours of annealing both samples had fully recovered from the irradiation
- Conclusion 100 krad irradiation
  - both samples survived irradiation
  - little recovery after 24 hours annealing
  - full recovery after 168 hours of annealing

CSA-PSA: conclusions

- the Alcatel Microelectronics CMOS 0.7μm technology shows good radiation tolerance
- deep submicron CMOS technologies can be a viable alternative to expensive radiation hard technology:
  - gate all around
- the sample set was too small to draw finalizing conclusions, but same message was heard on RadTol meeting

CSA-PSA: conclusions cont'd

- RadTol 49 meeting
  - gate allround techniques for analog as well as digital libraries
  - promising results were presented at the RadTol meeting
  - ⇨ plain CMOS is a true candidate for future space applications.
- Publications originating from this work
  - J. Vandenbussche, F. Leyn, G. Van der Plas, G. Gielen, "Total Dose Testing of a Standad CMOS Particle Detector Front-End for Space Applications", RadTol meeting R49, Geneve, October 28 1998.
  - J. Vandenbussche, F. Leyn, G. Van der Plas, G. Gielen, and W. Sansen, "A Fully Integrated Low-Power CMOS Paritcle Detector Front-End for Space Applications", IEEE Transactions on Nuclear Science, Vol. 45, pp. 2262-2272, August 1998.

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  - Design methodology
  - Architectural level design
  - Device level design
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  - Measurements
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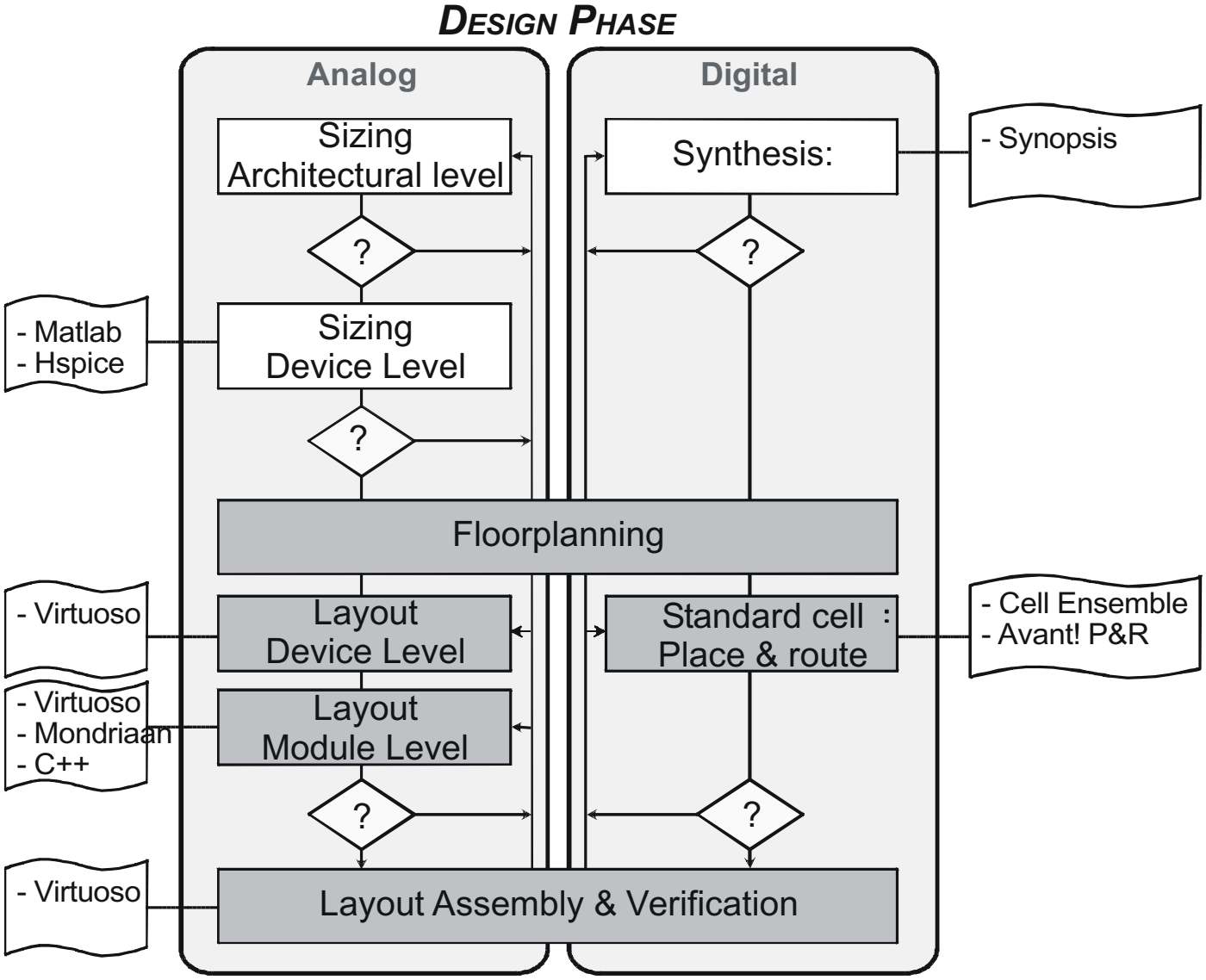
Objectives

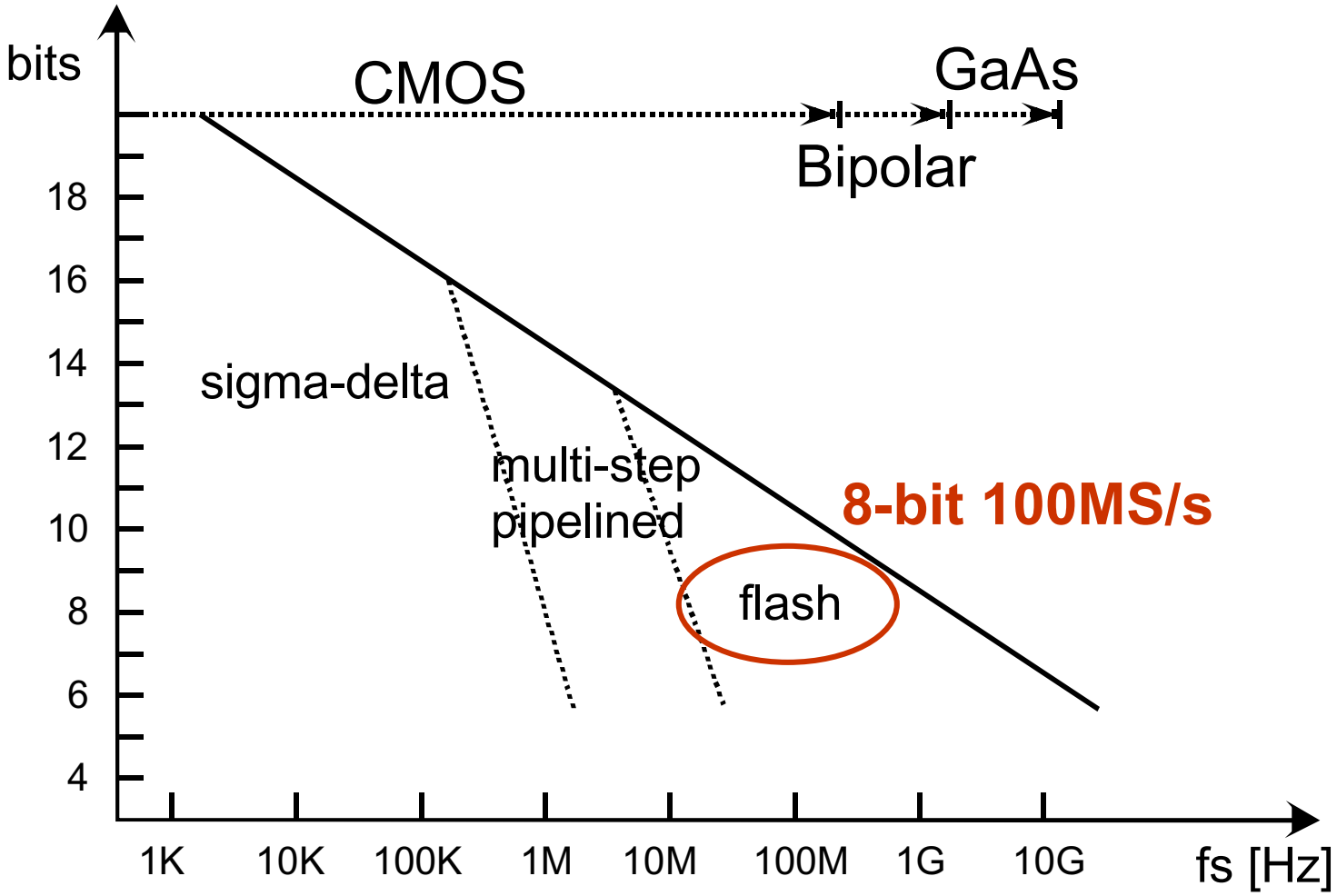
- Address how state-of-the-art design can be enhanced using AMGIE functionality
  - topologies change as technological boundaries move on
  - what about design re-use?
  - how to speed up the design, what tasks can be automated?
- Demonstrator design:
  - 8-bit ADC at 60-100MS/s is a typical component in receiver front-ends
  - design of high-speed ADC core for high-speed base station application (GPS, video decoding, TV decoding, satellite decoding, WLAN, …)
- Workpackages:
  - WP 2120, WP 2200, WP 2300, WP 2400, WP 2500

Design Methodology



- symbolic analysis for sizing level
- no analog tools for module level
  - MONDRIAAN Tool
  - bus generator
  - equal delay routing
- assembly manually

Architectural Level: overview topologies



Architectural Level: overview cont'd

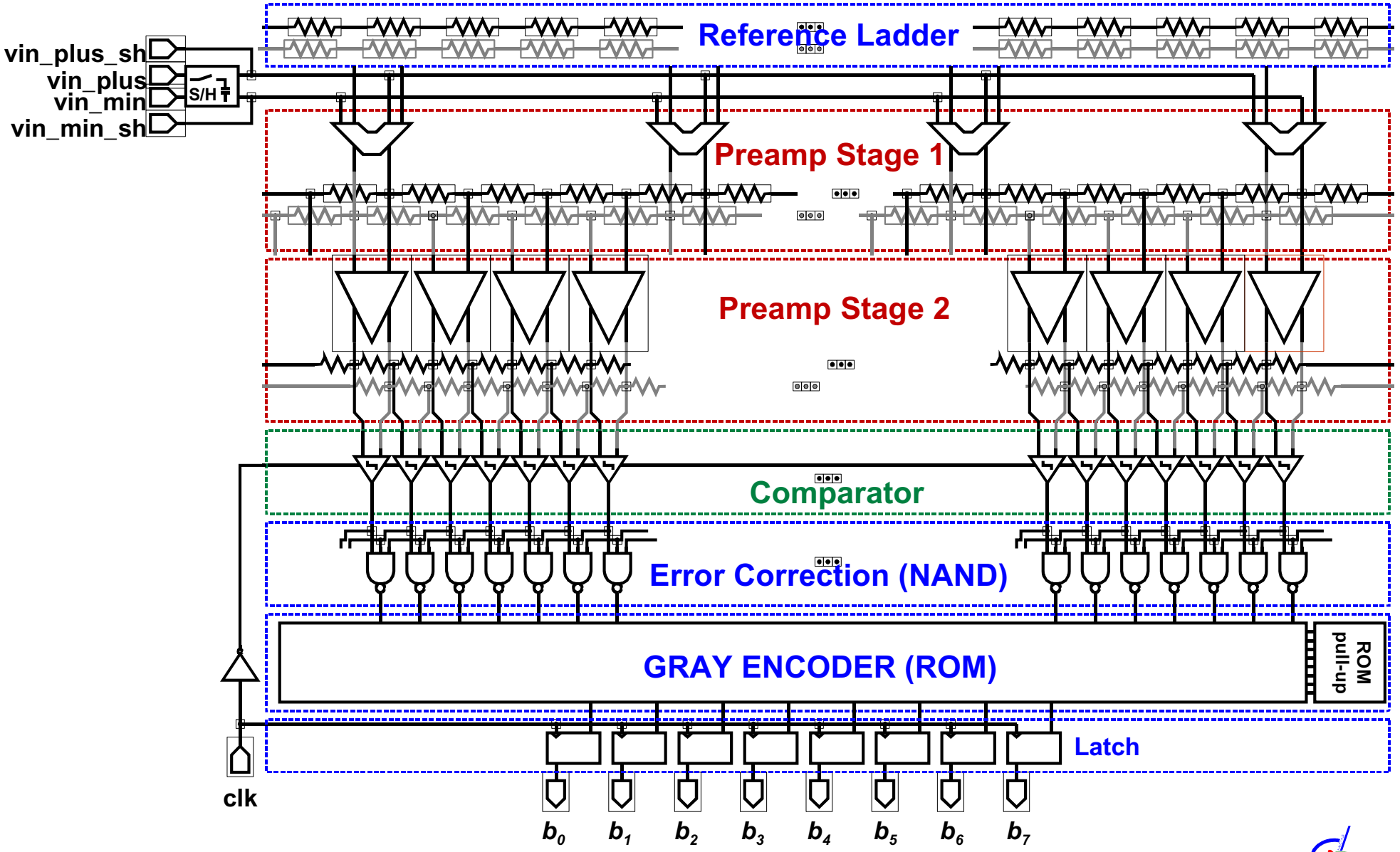
- Possible candidates for 8-bit 100MS/s ADC:
  - pipelined architecture
    - low power
    - sampling speed shifts to higher frequencies as technology scales down
    - no publications on such high-speed 'working' designs
  - flash:
    - consumes a lot of power
    - intrinsically the fastest architecture with its full parallel implementation
    - 8-bit 80MS/s CMOS flash ADC has been published

⇨ Only the flash architectures are capable of obtaining the targeted specifications in the 0.35 μm CMOS technology

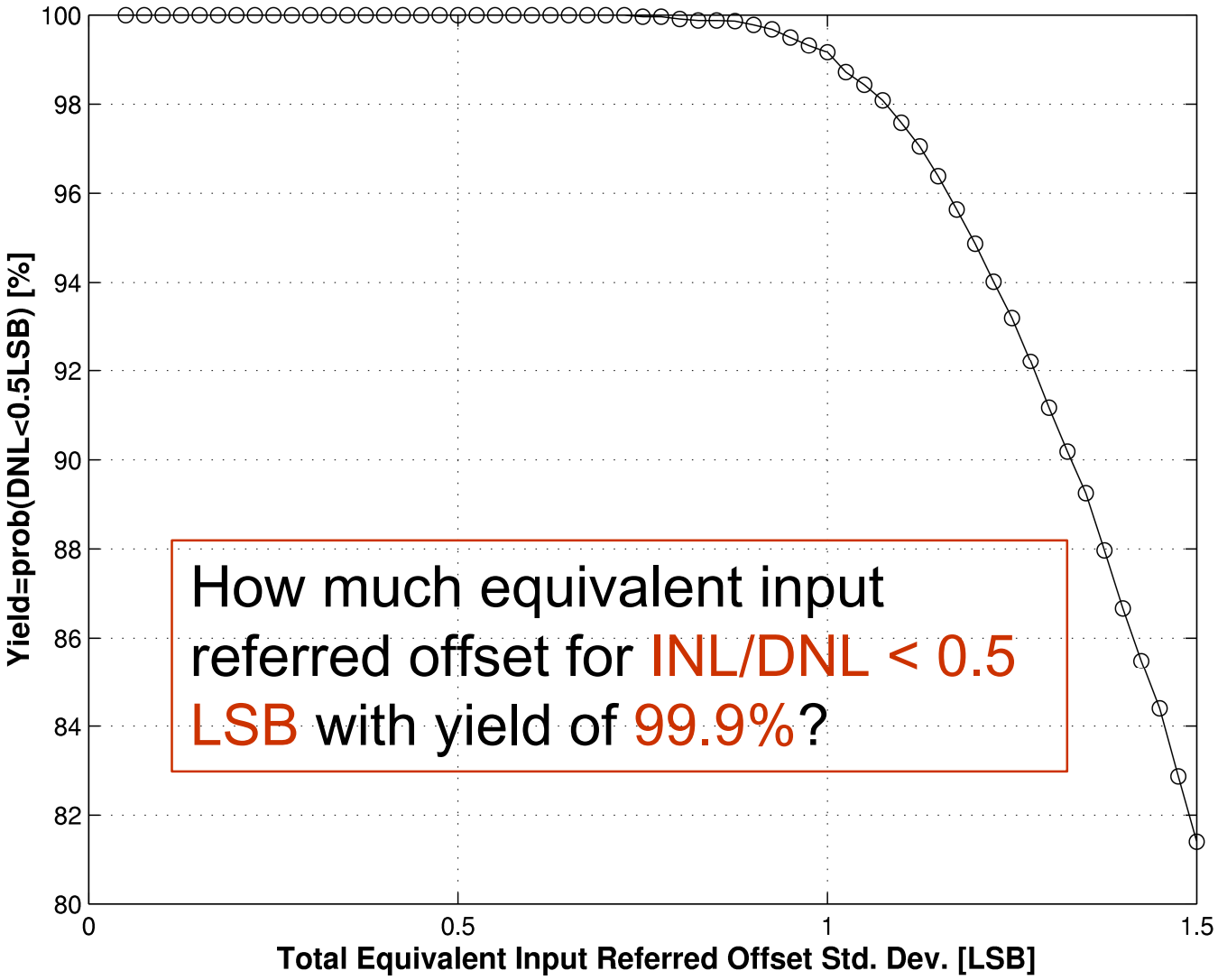
Architectural Level: Flash ADC

- Problems classical flash ADC
  - large power consumption (2^N comparators)
    - solution: folding
  - large input capacitance, resulting in bandwidth limitations for input signal frequencies
    - solution: interpolation
  - input feedthrough
  - kickback noise
- Additional improvements
  - averaging (Bult ISSCC) by preamplifiers
  - new fully differential input stage
  - new enhanced comparator to avoid kickback noise

Architectural Level: block diagram



Architectural Level Design



- Static performance:
  - INL/DNL < 0.5 LSB with yield 99.9%
  - Monte-Carlo simulations
  - $\sigma_{offset} < 0.7\ LSB$
- Dynamic performance:

  ...

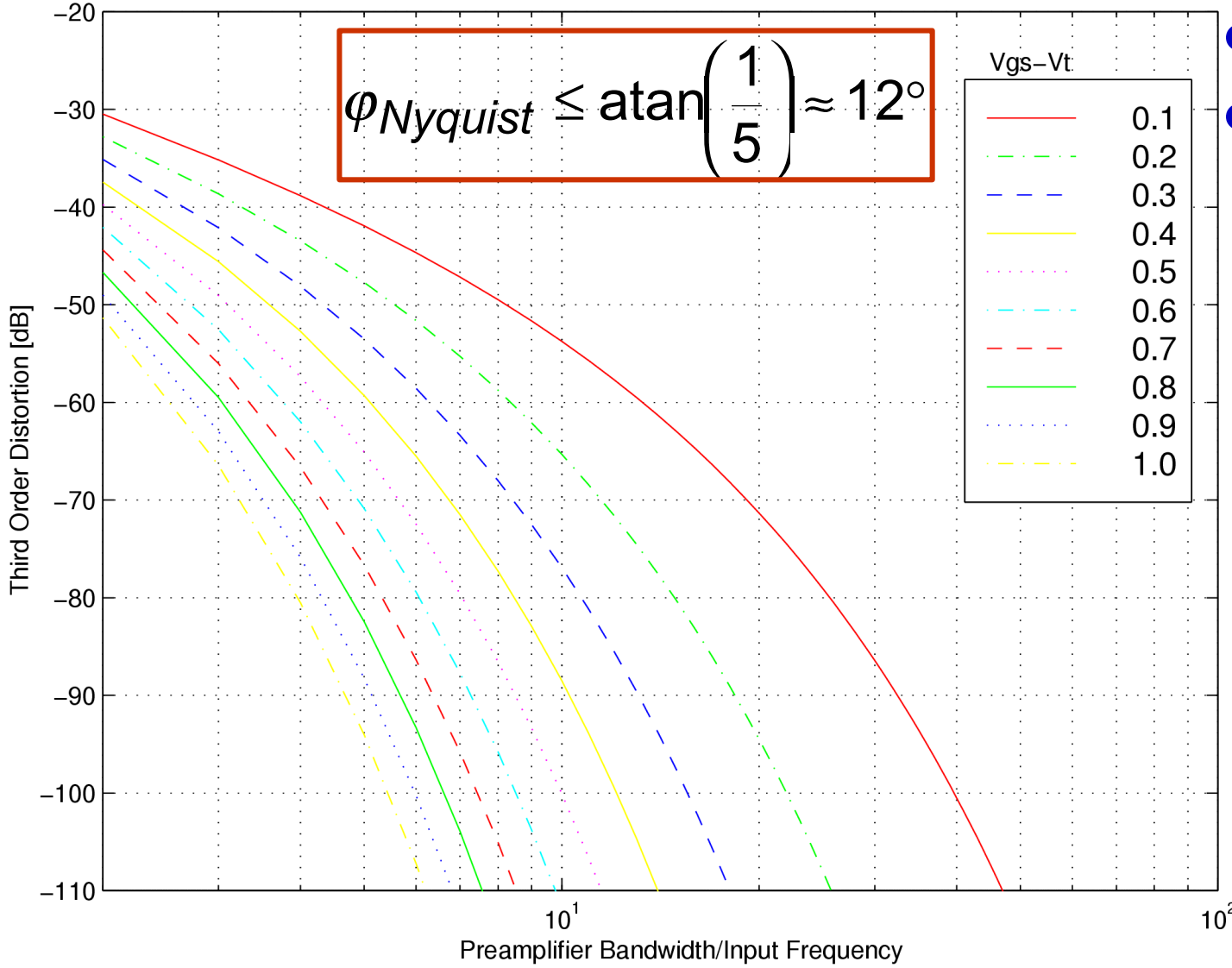
Architectural Level Design cont'd

$$\sigma^2_{total,offset} = \sigma^2_{preamp\_st1,offset} + \left(\frac{\sigma_{preamp\_st2,offset}}{A_{preamp\_st1}} \right)^2 + \left(\frac{\sigma_{comp,offset}}{A_{preamp\_st1} \cdot A_{preamp\_st2}} \right)^2$$

- For optimal dynamic performance:
  - Mismatch contribution of comparator should be negligible
  - Comparator can be optimized for speed

$$\Rightarrow \quad A_{preamp} = A_{preamp\_st1} \cdot A_{preamp\_st2} = f(INL, technology) \geq 15$$

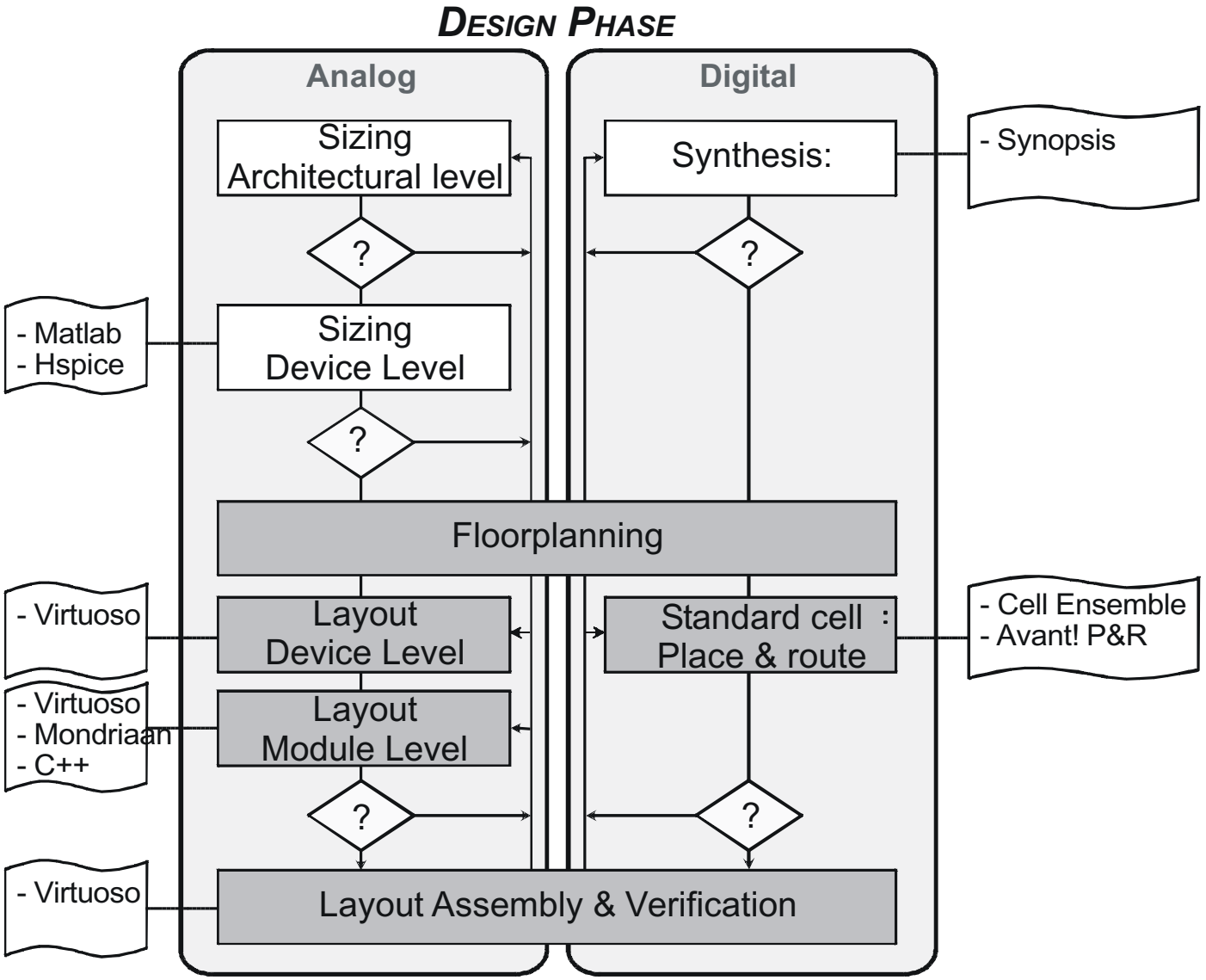
Architectural Level Design cont'd



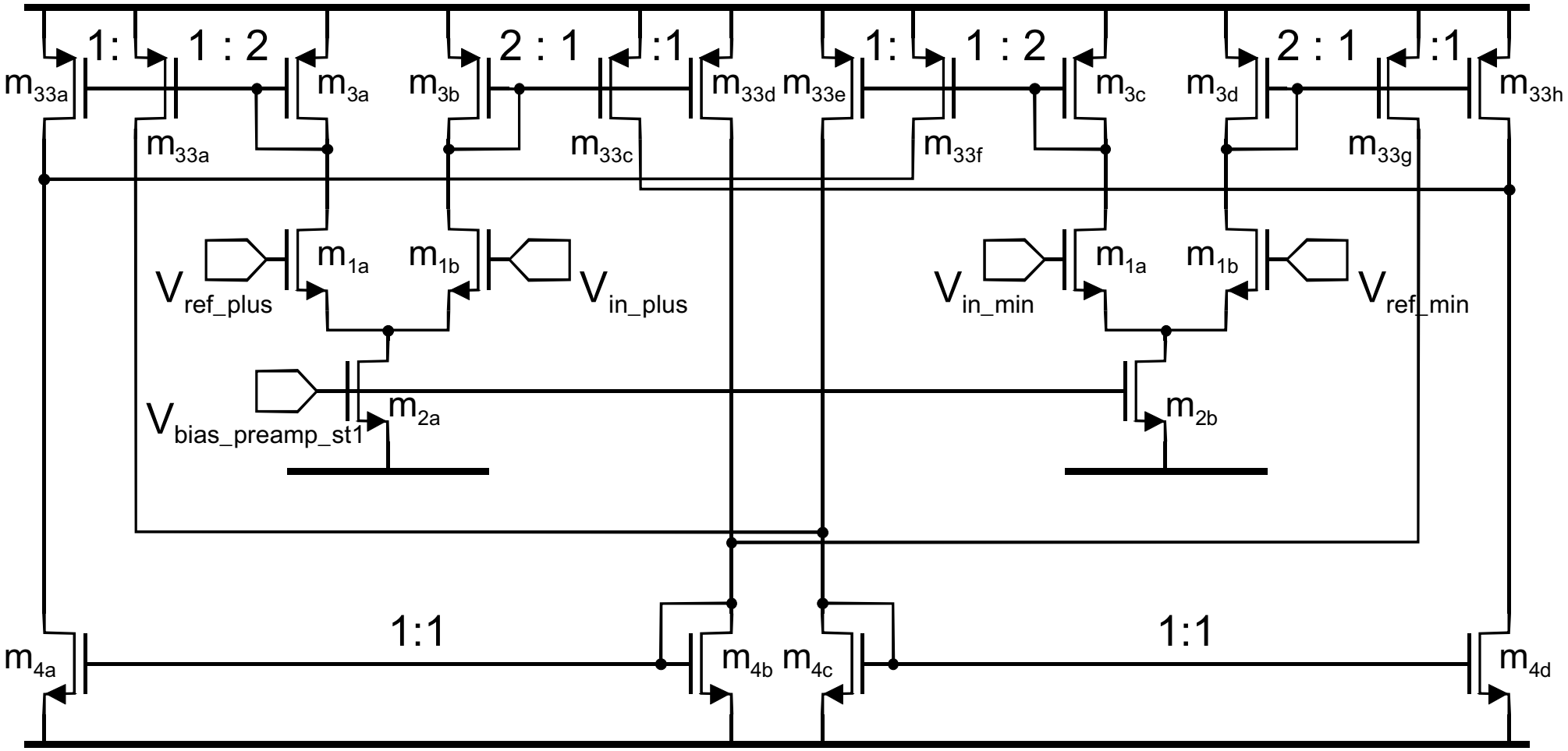
- Static performance
- Dynamic performance
  - Admissible phase shift for Nyquist performance?
  - V_{gs}-V_t = 0.3 V
  - *Preamplifier Bandwith/Input Frequency* = 5.
  - 50dB 3rd order distortion (8bit)

⇨ $f_{p,preamp}$ > 250MHz

Design Methodology



Device Level Design: 1st preamp stage



Device Level Design: 1st preamp stage cont'd

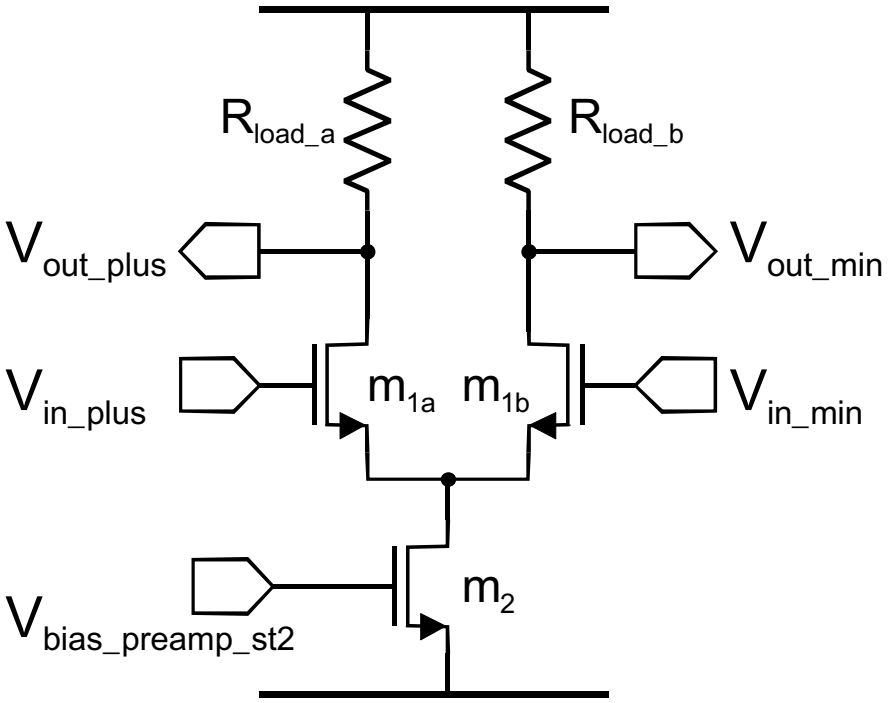
- Constraints from architectural design
  - $A_{preamp\_st1} = 10$
  - $f_{dominant,preamp\_st1} > 500MHz$
  - $\sigma^2_{preamp\_st1} = \frac{3}{4}\sigma^2_{total,offset} \leq \frac{3}{4}(0.7LSB)^2$
- Additional design equation derived using ISAAC tool
- Sizing script (Matlab) using ASA optimization algorithm

Device Level Design: 2nd preamp stage

- Constraints from architectural level
  - $A_{preamp\_st2} = 2$
  - $f_{dominant,preamp\_st2} > 500MHz$

    $\varphi_{Nyquist} \leq \text{Arctan}\left(\frac{1}{5}\right) \approx 12°$
  - $\sigma^2_{preamp\_st2} = \frac{1}{4}\sigma^2_{total,offset}$

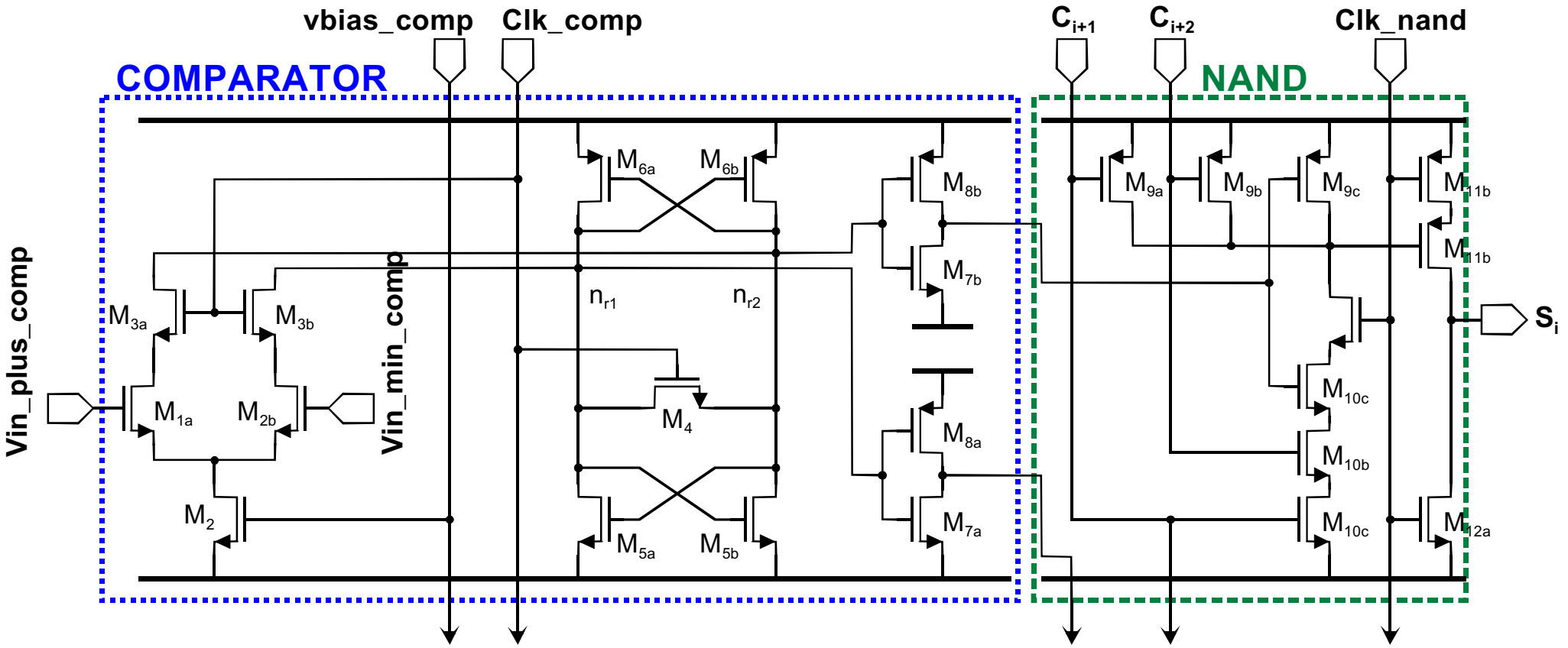
    $\leq \frac{1}{4}(0.7\ LSB)^2$



- Additional design equation derived using ISAAC tool
- Sizing script (Matlab) using ASA optimization algorithm

Device Level Design: comparator

- very fast regenerative structure
- reset when clock is high



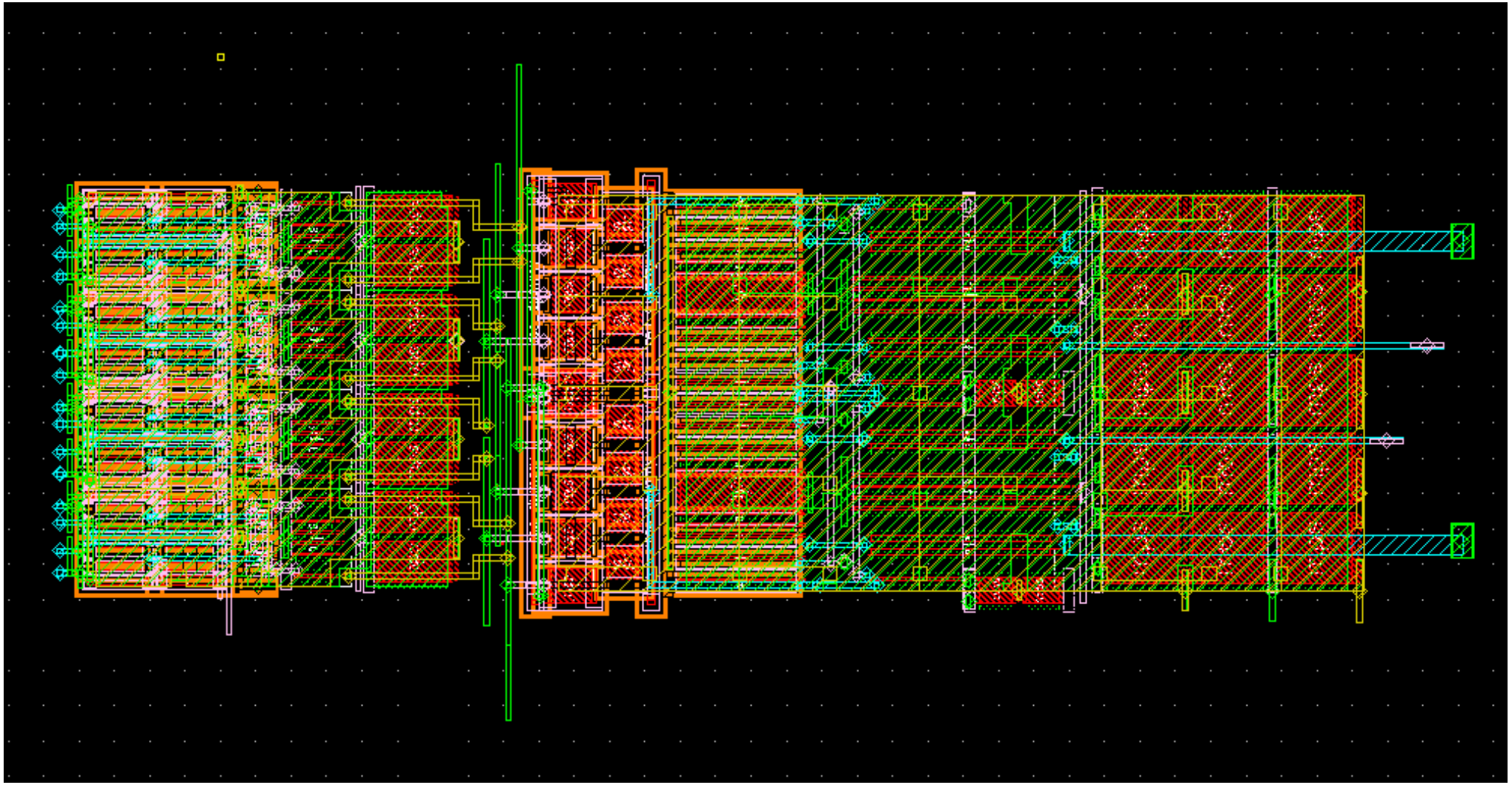
Device Level Design: digital back-end

- encodes the thermometer code in Gray code
- 3- input NAND gate in the ROM decoder,
  - additional error correction is done,
  - avoid bubbles in the output
  - avoid metastability
- standard cell synthesis doesn't meet high-speed specs
  - 'manual' design
  - Maple scripts for sizing
  - eldo for transistor level simulations

Layout generation

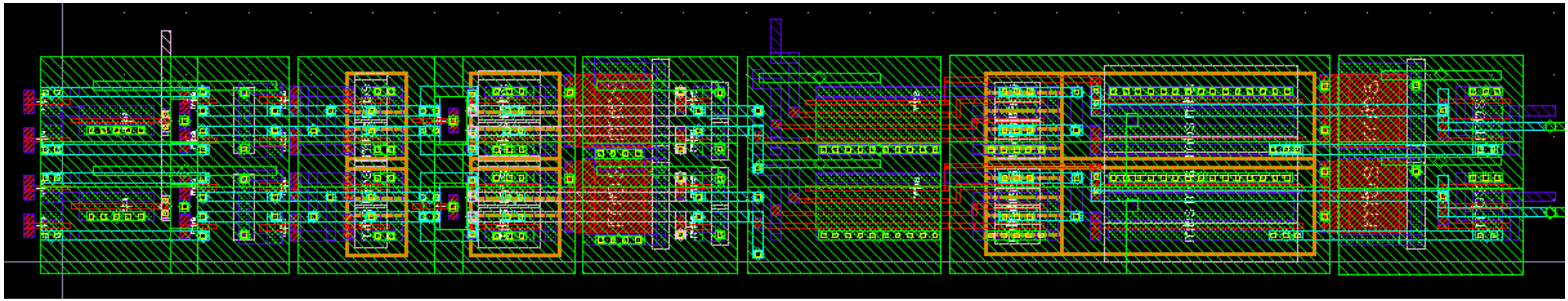
- Layout-driven design: sized schematic alone does not constitute an operational converter
  - analog and digital power supplies have been separated
  - around the perimeter of the chip 1 nF of decoupling capacitance has been integrated to provide stable power supplies
- Layout preamplifier stages
  - layout of the preamplifiers was done manually
  - devices were generated using LAYLA
  - placement and routing was done manually
  - MONDRIAAN for regular arrays/connections
  - additional 500 pF of decoupling capacitance internally
  - guard rings to reduce substrate (digital) noise coupling

Layout generation cont'd



Layout generation cont'd

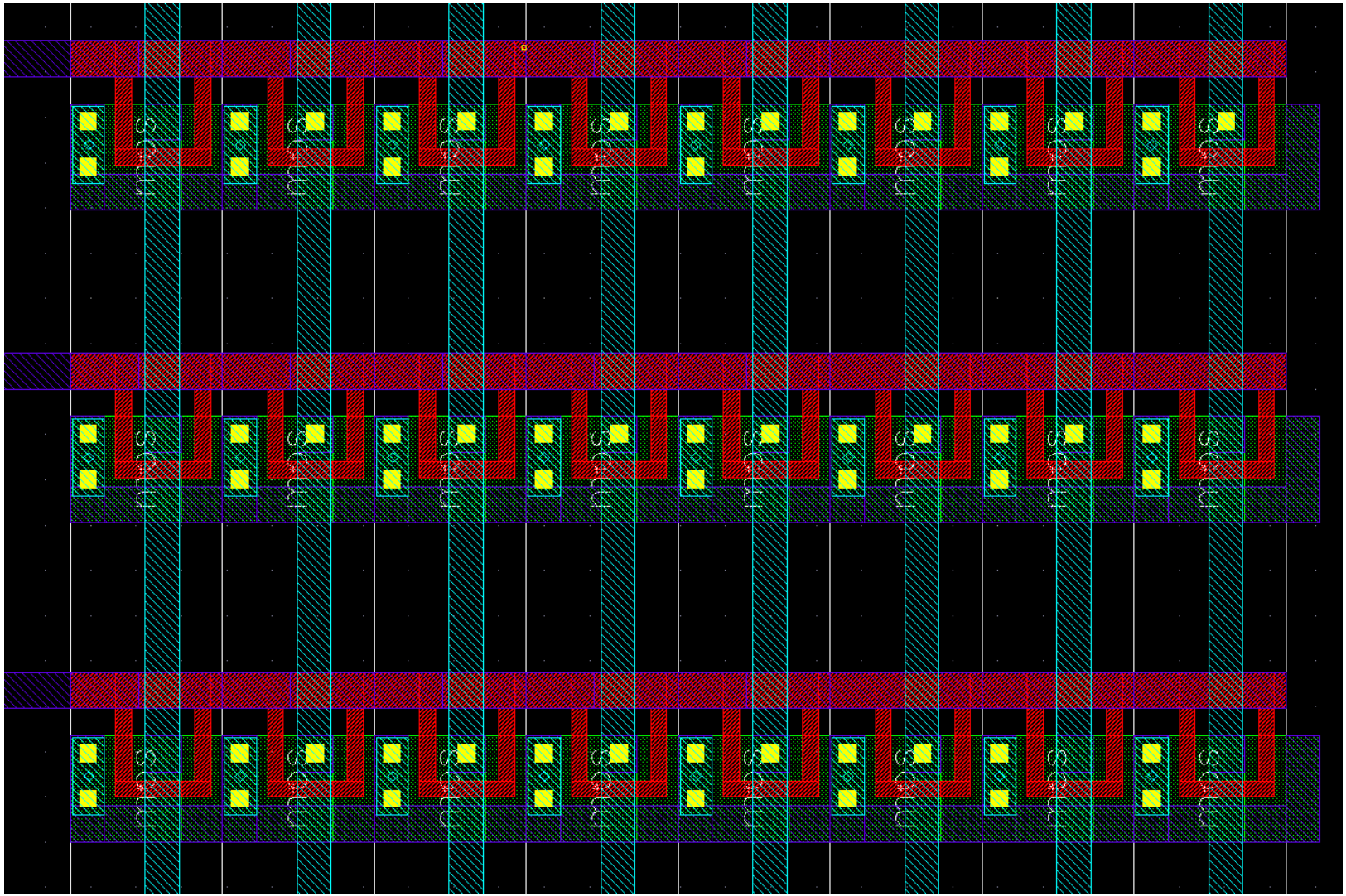
- Comparator
  - layout manually
  - placement & routing using Mondriaan for regular arrays/connections



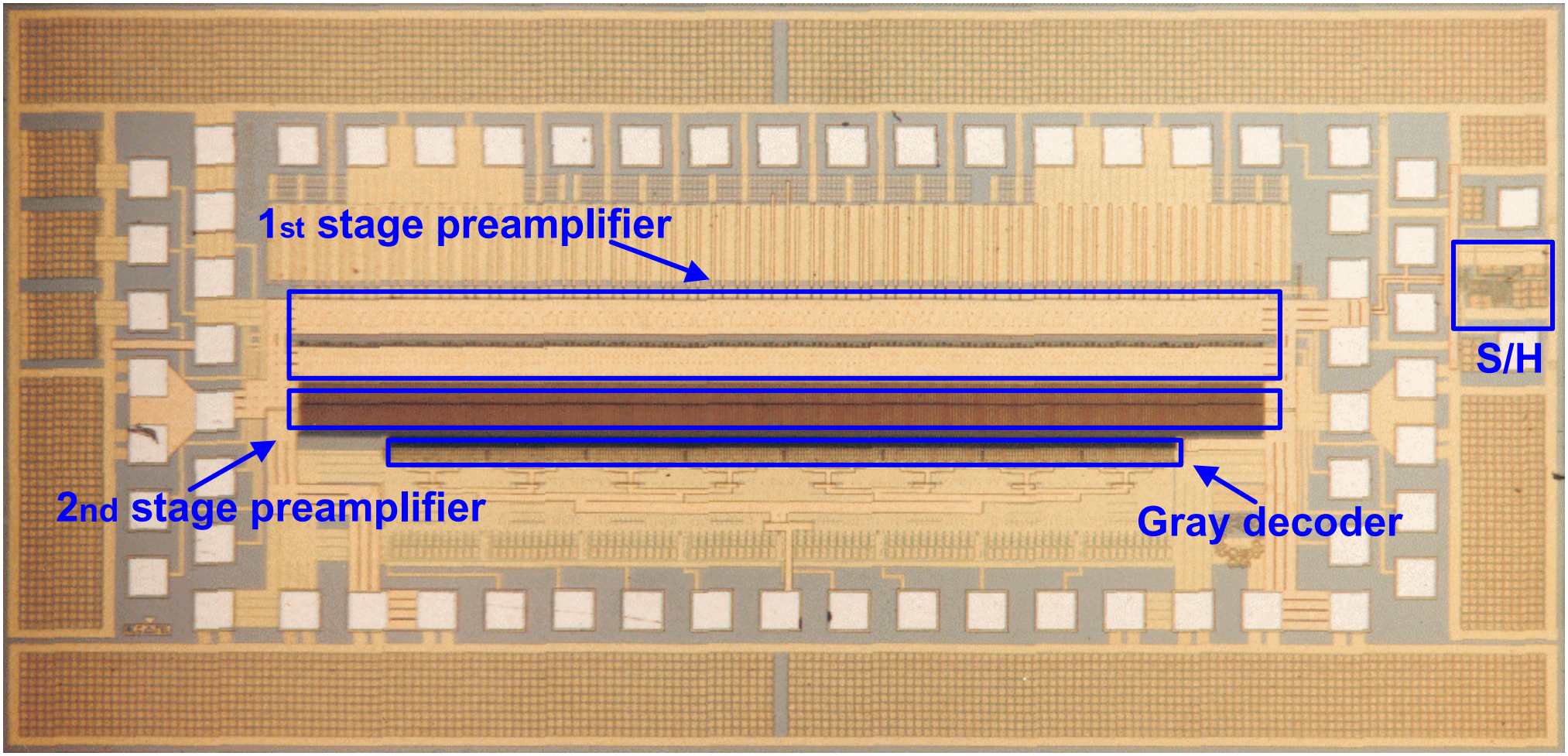
Layout generation cont'd

- ROM decoder
  - ROM cell manually
  - ROM array generated using the MONDRIAAN tool
- A buffered binary clock tree
  - clock tree generated using MONDRIAAN
  - the design and layout of the clock buffer was done manually

Layout generation cont'd

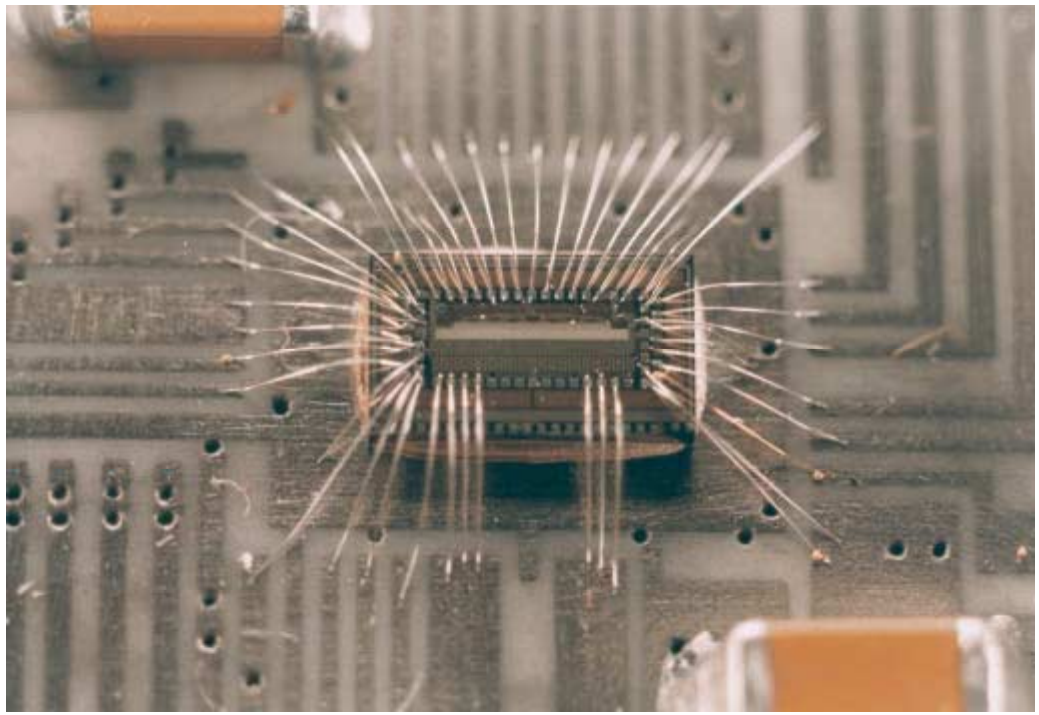


Layout: micro photograph

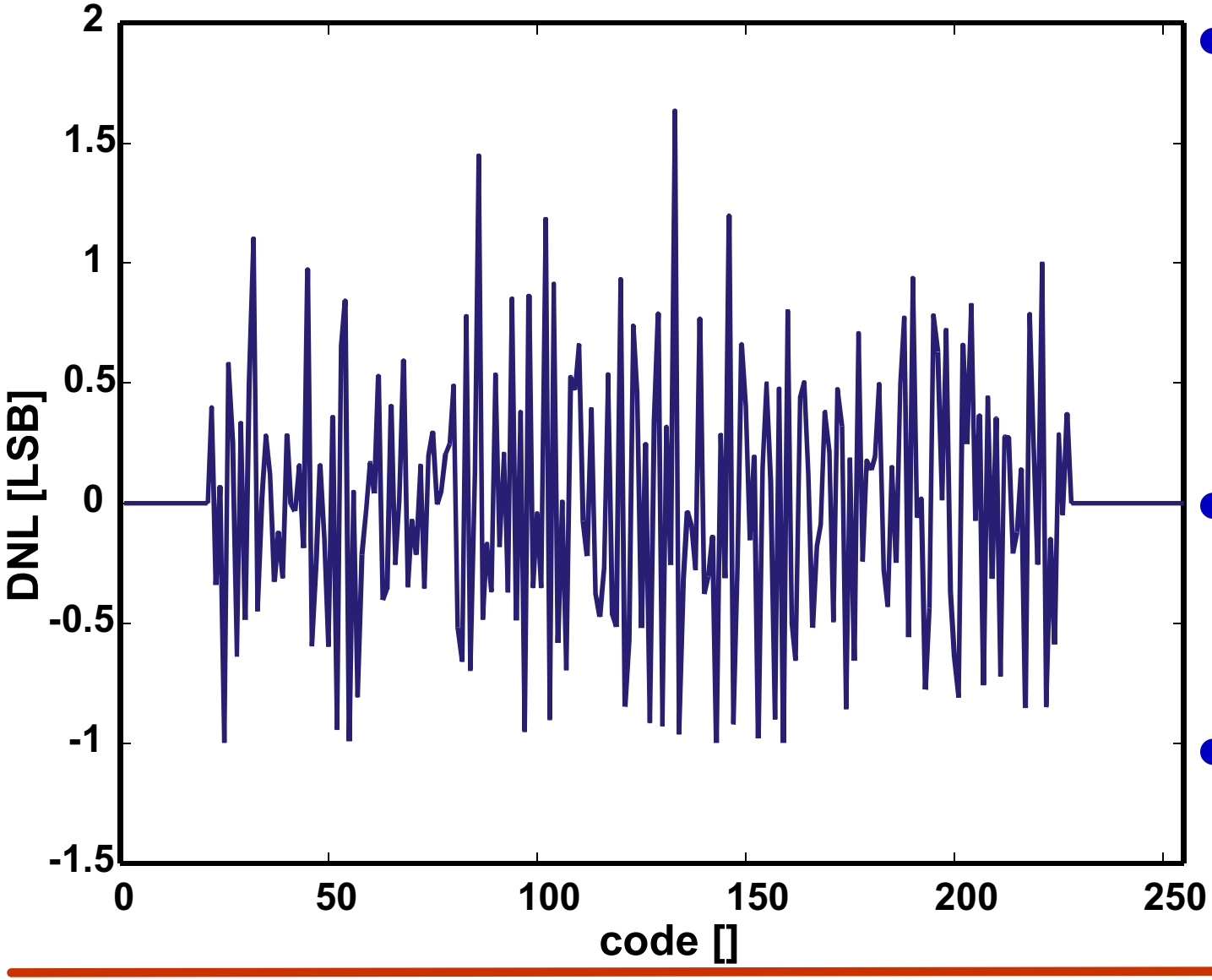


Characterization High-speed ADC

- Functional testing
  - static measurements (INL/DNL)
  - dynamic Measurements (SFDR/SNDR)
  - datasheet
- Irradiation testing
  - budget reallocated for redesign
- Dedicated test PCB was developed



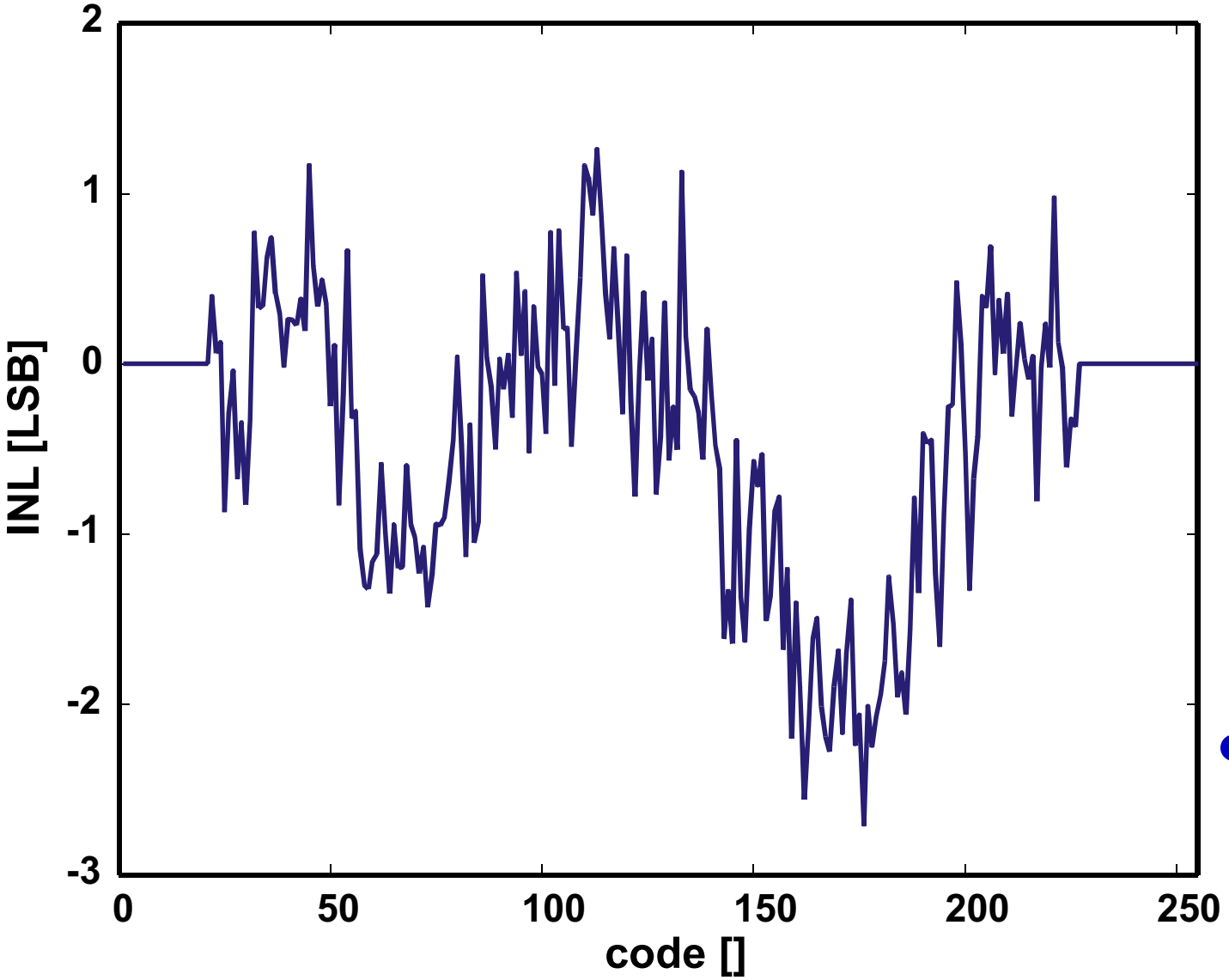
Characterization: static measurements



- Full speed measurement
  - f_{clk} = 100 MS/s
  - f_{in} = 3 kHz
  - calculate histogram
  - after unwrapping INL/DNL can be calculated
- With default biasing ADC shows missing codes
- After tuning:

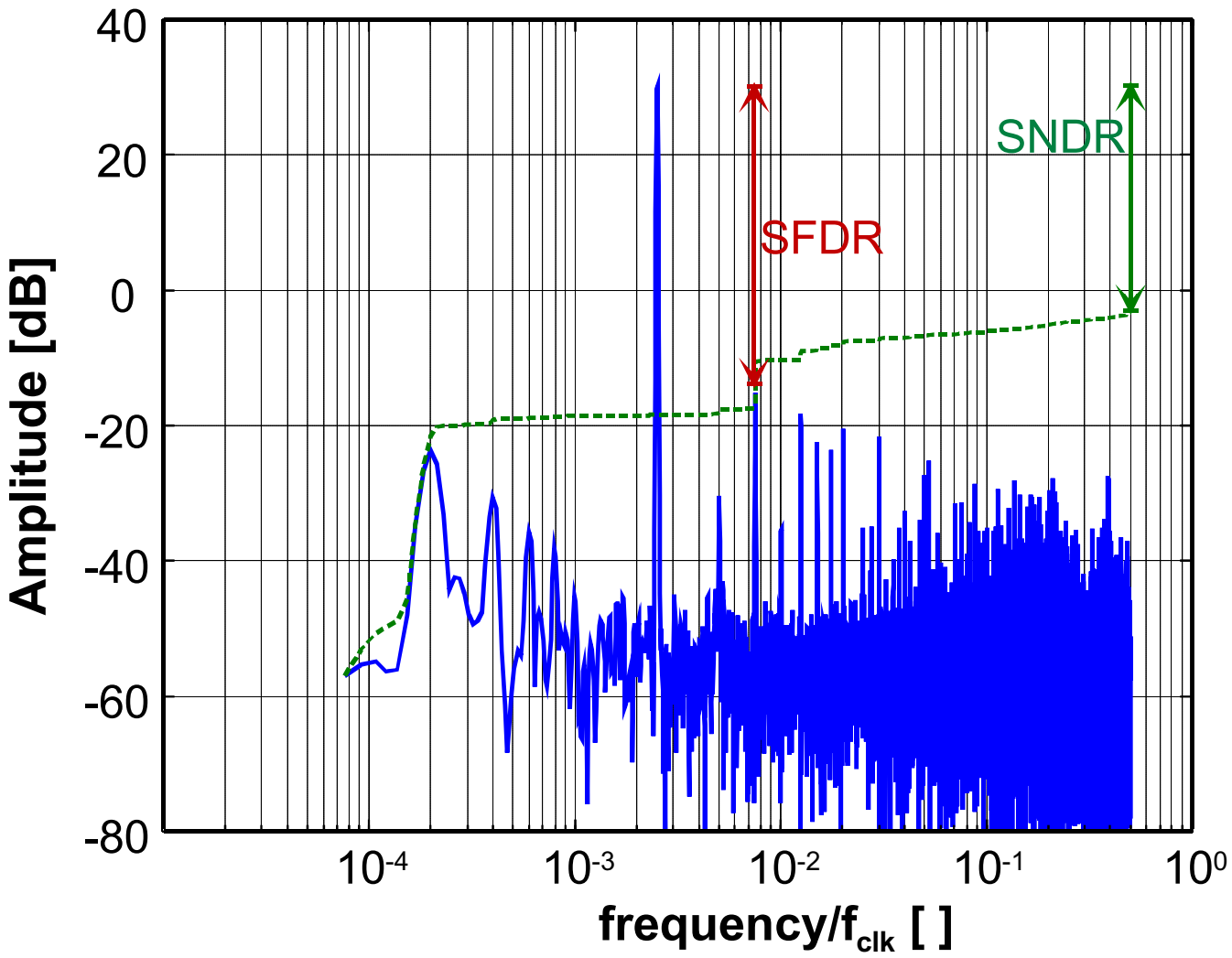
  DNL < 1.6 LSB

Characterization: static measurements cont'd



- After tuning:
  INL < 2.7 LSB

Characterization: dynamic measurements

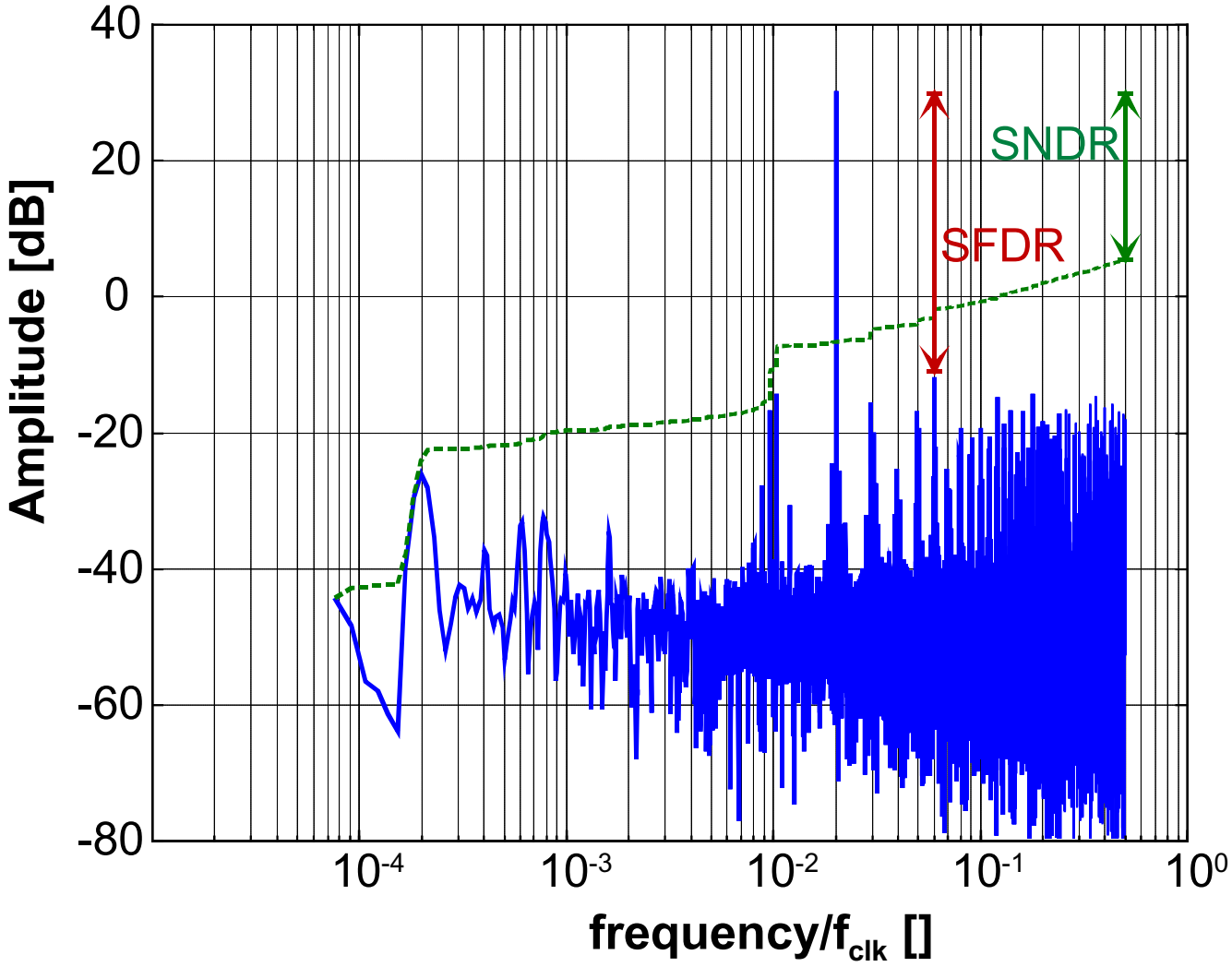


- After tuning
- f_{clk}= 100MS/s
- f_{in} = 6 kHz

SFDR = 46 dB

SNDR = 38 dB

Characterization: dynamic measurements cont'd



- After tuning
- f_{clk}= 100MS/s
- f_{in} = 5 MHz

SFDR = 42 dB

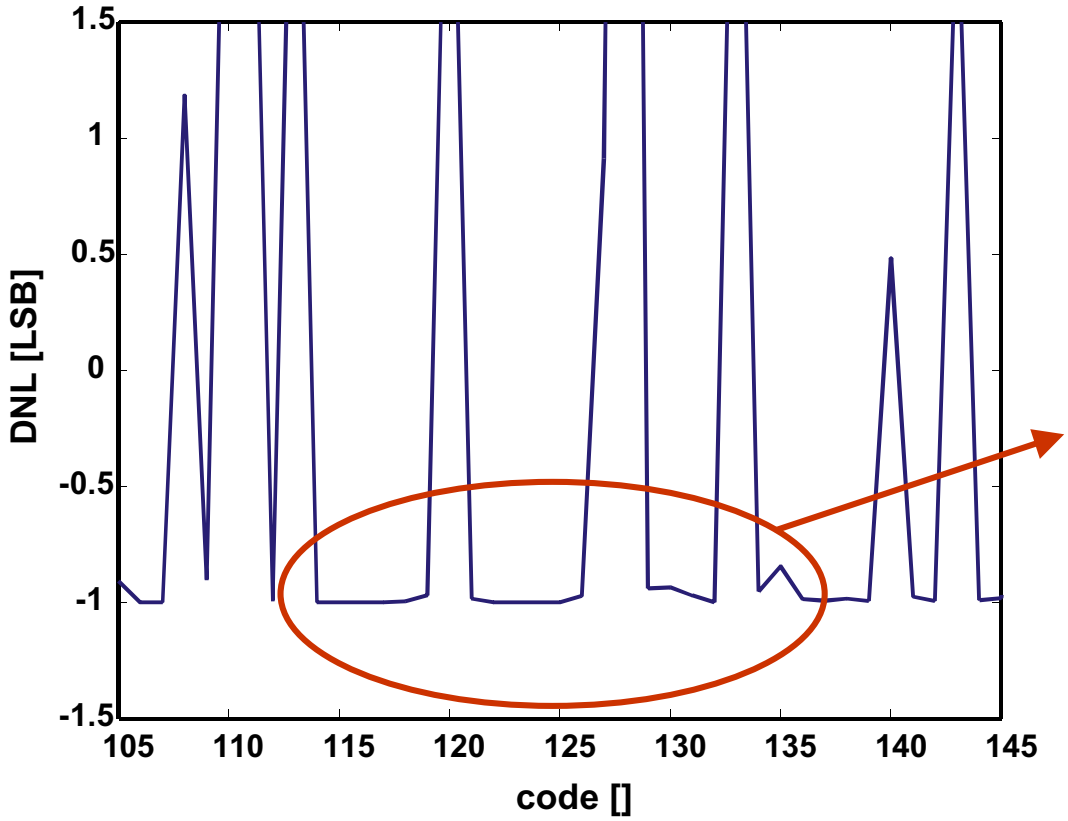
SNDR = 29 dB

Characterization: datasheet

Specification	Target value	First Design
input capacitance	< 100 pF	3 pF
input range	> 0.5 V ptp	1.3 V ptp
latency	not specified	1 clock cycle
INL/DNL	< ½ LSB	2.7/1.6 LSB
SFDR	> 45 dB	46 dB @ f_{in}=6 kHz 42 dB @ f_{in}=5 MHz
SNDR	> 40 dB	38 dB @ f_{in}=6 kHz 29 dB @ f_{in}=5 MHz
ENOB	6.5 bits @ 30 MHz	NM
parallel output	ok	ok
digital output: • logic family • data format	CMOS levels Gray Code	CMOS levels Gray Code
Conversion rate	1 code/clock cycle	1 code/clock cycle
Update rate	60 MS/s	100 MS/s
Drive Capability	-	10 pF@100MS/s 5 pF @200MS/s
radiation tolerance	50 krad	NM

Measurement analysis

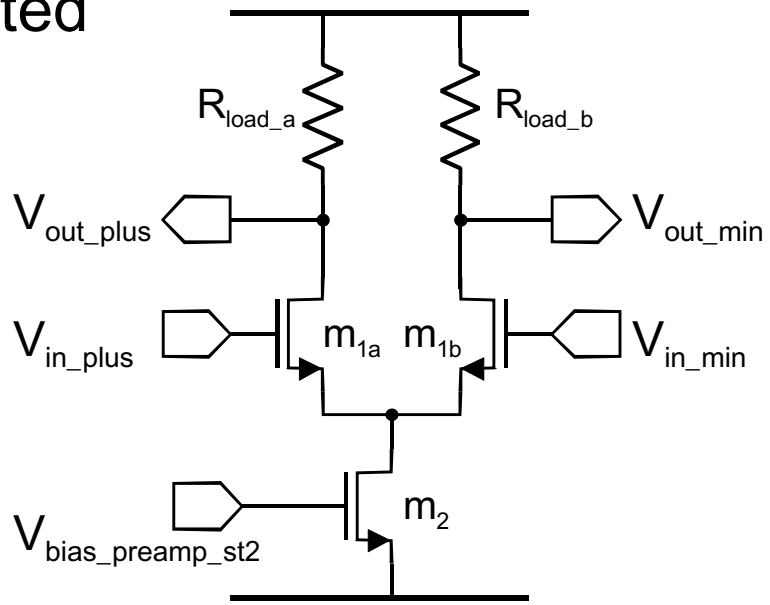
- High-speed ADC is working at 100 MS/s
- Slightly out of spec
- INL measurements show missing codes



Codes are never excited

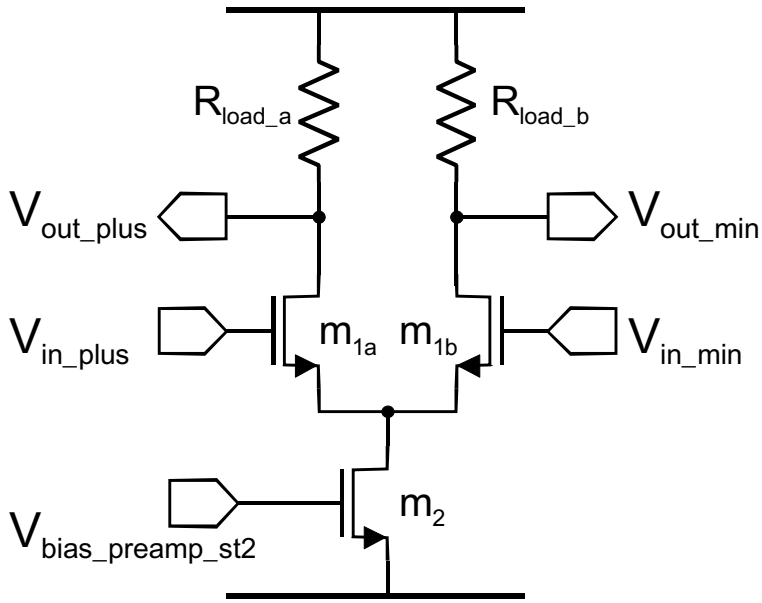
Measurement analysis cont'd

- Malfunctioning second stage preamplifier
  - common mode output 2nd stage preamp too low
  - ⇨ input transistor of the comparator out of the saturation region
  - ⇨ no gain in comparator
  - ⇨ mismatch amplified instead of attenuated
- Hypothesis consolidated by:
  - additional (symbolic) analysis comparator [Van der Plas ECCTD '98]
  - transistor level simulation with tuned biasing
  - measurements with tuned biasing: no more missing codes

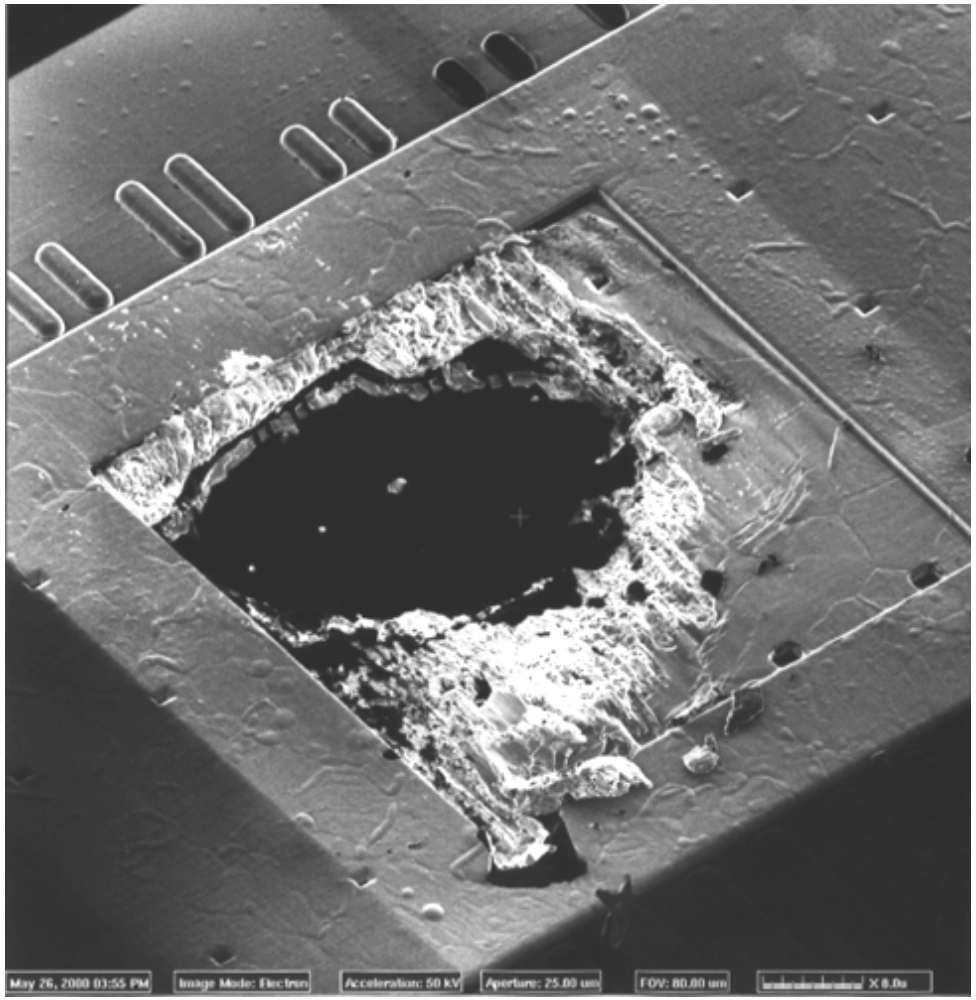


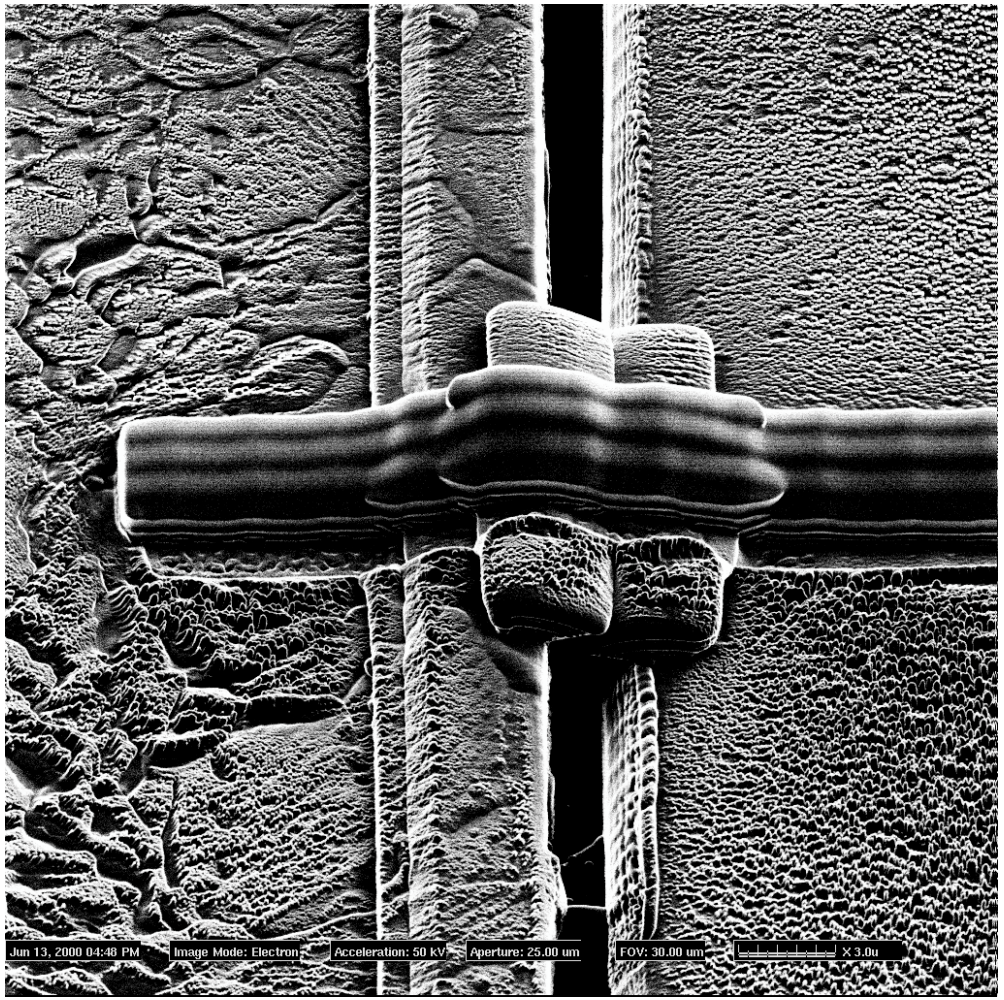
Measurement analysis: solutions

- Possible solutions …
  - increasing the DC current through the 2nd stage preamp
    - current source diff pair no longer in saturation!
  - isolating power supply 1st and 2nd stage preamp with FIB
    - large setup times (days), not routine job!
    - 3 samples FIBed, none were functional afterwards
  - ⇨ Redesign?



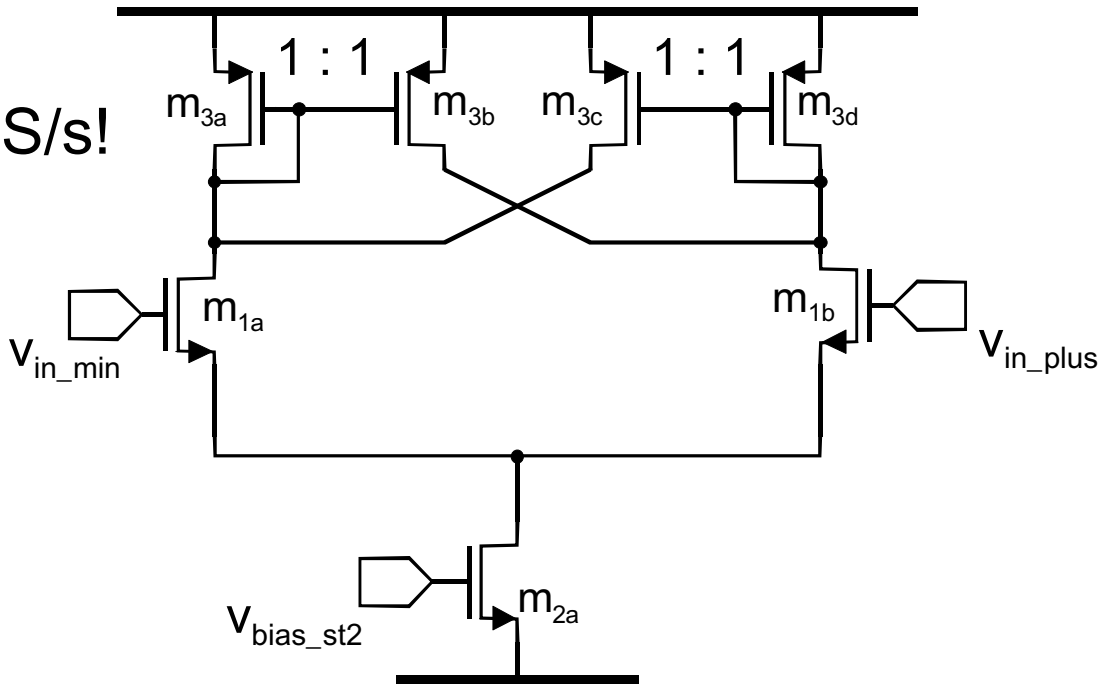
Measurement analysis: solutions cont'd



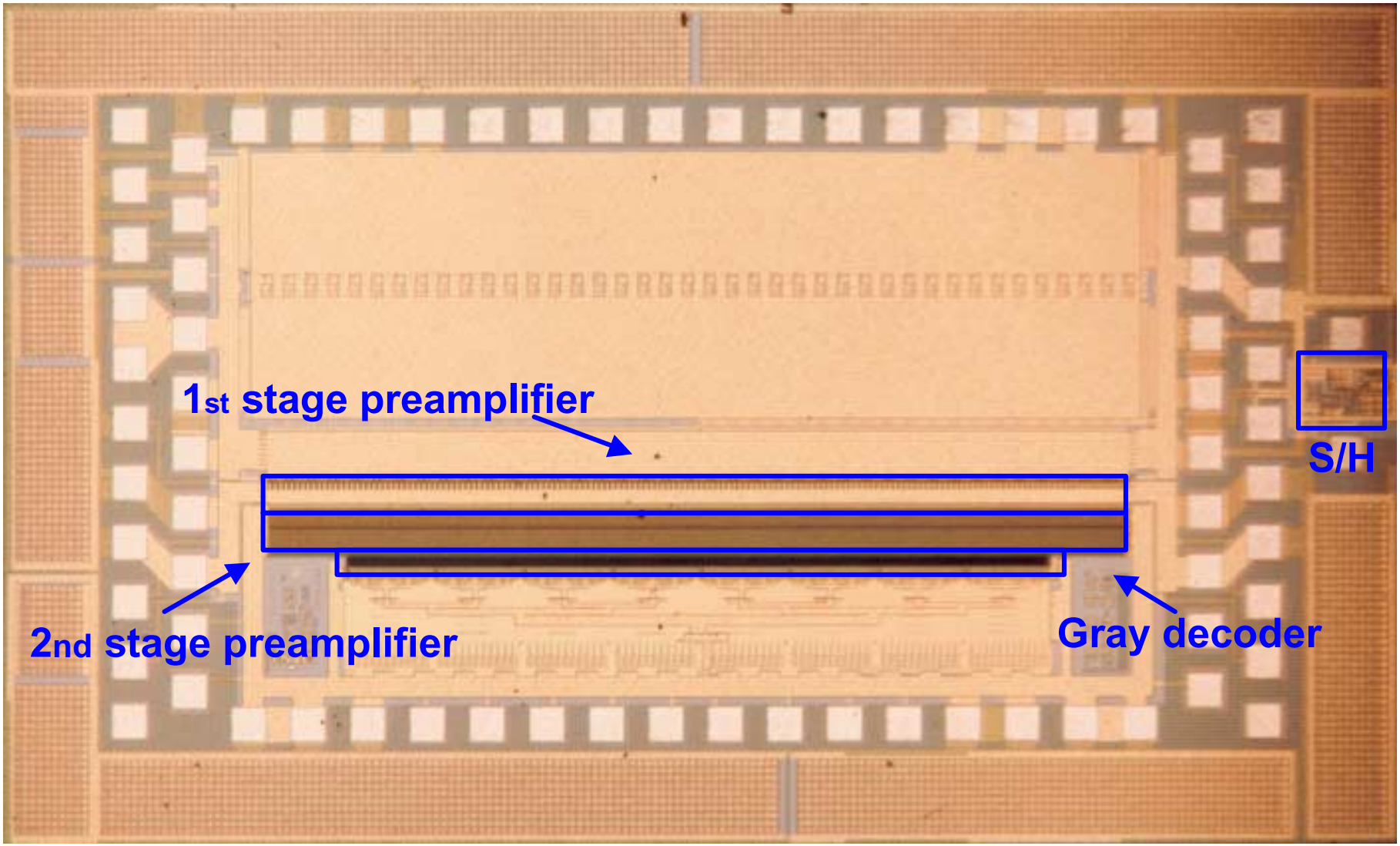


Redesign High-Speed ADC

- New topology for 2nd stage
- Comparator upscaled
  - 1st design runs up to 200 MS/s!
  - lower mismatch
- Separate power supply for 1st and 2nd stage preamplifiers



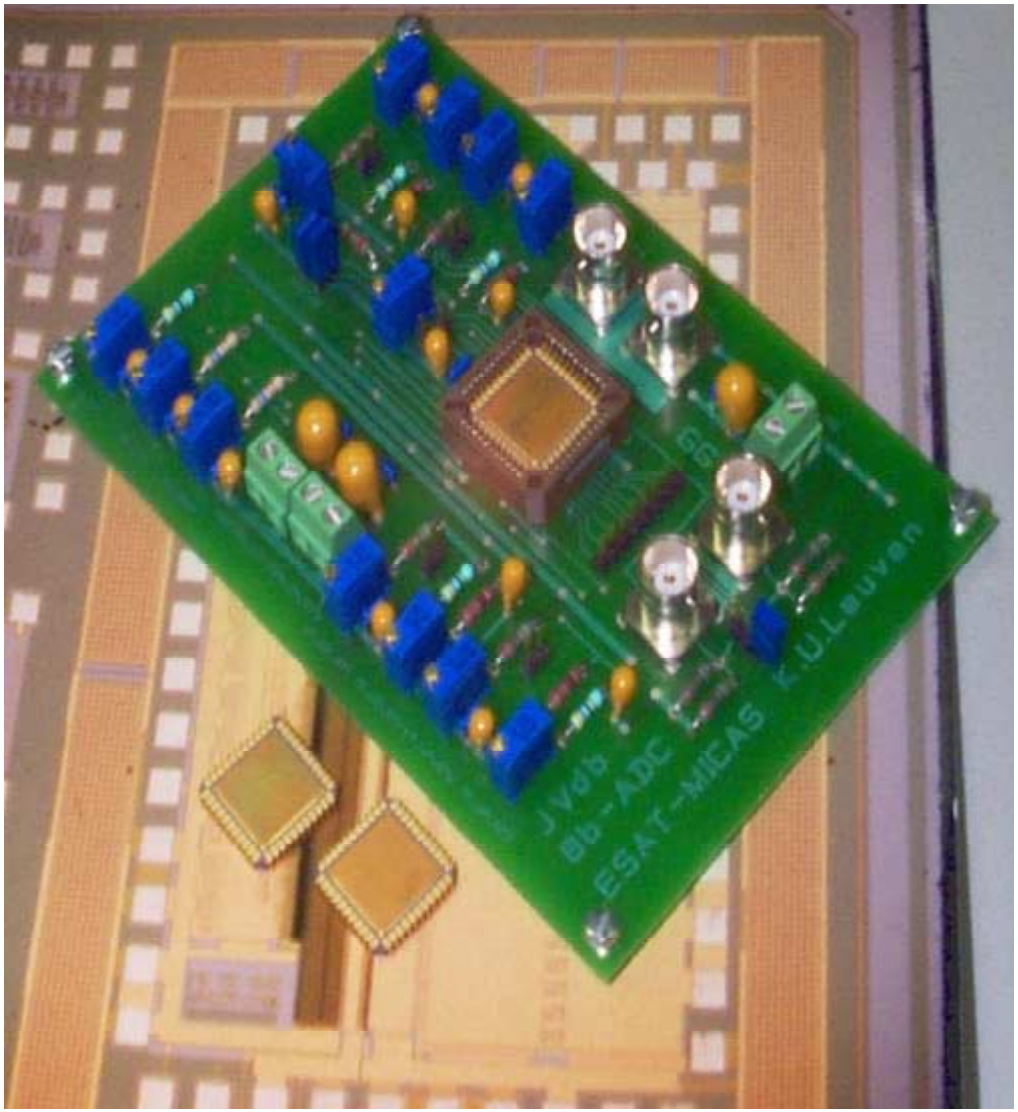
Redesign High-speed ADC cont'd



Redesign High-Speed ADC: datasheet

Specification	Target value	First Design	Redesign
input capacitance	< 100 pF	3 pF	4.8 pF
input range	> 0.5 V ptp	1.3 V ptp	1.3 V ptp
latency	not specified	1 clock cycle	1 clock cycle
INL/DNL	< ½ LSB	2.7/1.6 LSB	0.3/0.6 LSB
SFDR	> 45 dB	46 dB @ f_{in}=6 kHz 42 dB @ f_{in}=5 MHz	-
SNDR	> 40 dB	38 dB @ f_{in}=6 kHz 29 dB @ f_{in}=5 MHz	-
ENOB	6.5 bits @ 30 MHz	NM	-
parallel output	ok	ok	ok
digital output: • logic family • data format	CMOS levels Gray Code	CMOS levels Gray Code	CMOS levels Gray Code
Conversion rate	1 code/clock cycle	1 code/clock cycle	1 code/clock cycle
Update rate	60 MS/s	100 MS/s	100 MS/s
Drive Capability	-	10 pF@100MS/s 5 pF @200MS/s	10 pF@100MS/s 5 pF @200MS/s
radiation tolerance	50 krad	NM	-

Conclusions



- Results
  - high-speed 100MS/s 8-bit ADC core (packaged/naked die)
  - test PCB delivered
- ADC core was used as external part in WLAN prototype [IMEC]
- Publications

Publications

- G. Van der Plas, J. Vandenbussche, G. Gielen and W. Sansen, "Mondriaan: a Tool for Automated Layout Synthesis of Array-type Analog Blocks", Proc. on the IEEE 1998 Custom Integrated Circuits Conference, pp. 485-488, California, May 1998.
- J. Vandenbussche, G. Van der Plas, W. Verhaegen and G. Gielen, "Statistical Behavioral Modeling of A/D Converters", IEEE/VIUF International Workshop on Behavioral Modeling and Simulation, Florida, October 1998.
- G. Van der Plas, W. Daems, E. Lauwers, J. Vandenbussche, W. Verhaegen, G. Gielen, W. Sansen, "Symbolic Analysis of CMOS Regenerative Comparators", European Conference on Circuit Theory and Design, pp. 86-89, Italy, August 1999.
- G. Van der Plas, J. Vandenbussche, W. Verhaegen, G. Gielen and W. Sansen, "Statistical Behavioral Modeling for A/D Converters", Proc. IEEE 1999 International Conference on Electronics, Circuits and Systems, pp. 1713-1716, Cyprus, September 1999.