Microelectronics Section

SCOC3
Spacecraft Controller On-a Chip with LEON3

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Contents

System-On-Chip in Space

- General aspects of SOC
  - Improve performance vs. component count and power consumption
  - Improve reliability (replace PCB interconnect by on-chip interconnect)
  - Increased complexity for chip development and verification
- Commercial Electronics → high part count → silicon cost driven

  → Minimise chip area for each project

  → SOC = diversified (customer and project specific) ASIC
- Space Electronics → low part count → ASIC are NRE cost driven

  → SOC for multiple projects, containing union set of functionalities

  → SOC to be used by multiple equipment manufacturers

➔ Two main types of development:

→ Limited number of SOC-ASIC as off-the-shelf ASSP (Application Specific Standard Product)

→ Variety of SOC developments on FPGA

Portable IP cores in HDL for SOC development

- Introduction of VHDL in the early 90's
  - Essential for IP-core based design
- First IP cores late 90's - early 2000's
  - TM, TC, VME, CAN, PCI, 1355, 1394, Sparc LEON1/2
  - Internal or external (ESA contracts) development
  - Distribution on ad-hoc basis or as open-source
  - Procurement of commercial 3rd party IP
  - Re-use subject to complex licensing schemes
- Introduction of the AMBA 2.0 standard in 2000
  - AMBA package http://microelectronics.esa.int/soc/amba.vhd
- ESA space IP-core service since 2003
  - Open source distribution discontinued (legal implications)
  - http://microelectronics.esa.int/core/corepage.html

SOC-related activities at ESA

- Internal R&D activities to evaluate SOC design tools and standards
  - Prosilog http://microelectronics.esa.int/papers/CarlqvistFinal_Report.pdf
  - OCP-IP http://microelectronics.esa.int/mpd2007/ESA-IP-Cores-Service-MPD2007.pdf
    http://microelectronics.esa.int/papers/OCP-PresentationMartaPosada.ppt
  - SystemC http://microelectronics.esa.int/papers/final_nlaine.pdf
- SOC studies and ASSP development (TRP/other corporate ESA funding)
  - Chipsat http://microelectronics.esa.int/soc/chipsat_abstract.pdf
  - AGGA3 http://microelectronics.esa.int/mpd2004/AGGA3-MPD2004_final.pdf
  - SpaceWire-RTC http://microelectronics.esa.int/mpd2004/AGGA3-MPD2004_final.pdf
  - SCOC1 http://microelectronics.esa.int/soc/soc.html#scoc1
- Proprietary SOC ASIC (GSTP/ARTES4 funding)
  - Cole http://microelectronics.esa.int/mpd2007/COLE-System-on-chip-MPD2007.pdf
  - MDPA http://microelectronics.esa.int/mpd2007/MDPA_Pres_March_2007.pdf
  - LEON3-DARE (test chip on 0.18 mm UMC with radiation hardened library)
    http://microelectronics.esa.int/mpd2007/LEON3_DARE_ASIC_Rev1.pdf

SCOC Development Programme

- **Building blocks for SOC**
  - ESA contract 13345/98/NL/FM
  - Defining a generic IPR model for the cores
  - SCOC feasibility study and definition
- **SCOC1 development 02/2002 – 05/2004 part of contract 13345**
  - Specification based on LEON1 (AMBA version)
  - IP core development: PTCD, 1553 (derived from ASIC designs), Spacewire
  - IP cores provided by ESA (PCI interface, CTM, PTME)
  - Development of the Board for LEON and Avionics DEmonstration (BLADE)
  - Design and validation of SCOC into BLADE (Xilinx Virtex 2000 target)
- **SCOC2 development under EADS Astrium funding**
  - Evolution based on LEON2 to improve the architecture and develop new IPs
  - Validation with Microsat Astrium Enhanced Versatile Architecture (MAEVA) FPGA prototype board (Virtex 2)
- **SCOC3 activity started 09/2006**
  - ESA TRP contract 20167/06/NL/FM

SCOC3 Project Overview

- **Specification phase (Q4/2006 – Q1/2007)**
- **Architectural Design (Q1/2007 – Q1/2008)**
  - Migrate design to LEON3 and GRLIB
  - IP core upgrade and new design (performance monitoring)
  - Verification at VHDL RTL level
  - Feasibility Study with ASIC synthesis and timing analysis
- **Validation and SW Activities under EADS Astrium funding**
  - S/W development (drivers, boot, self-tests, …)
  - Virtex 4 (LX200) FPGA validation/demonstration board
  - Progressive integration of the IP macros
- **ASIC implementation in follow-up contract (GSTP, TRP, 2008-2009)**
  - Detailed design and ASIC manufacturing (baseline Atmel ATC18RHA)
  - Validation and release as a standard component (ASSP)

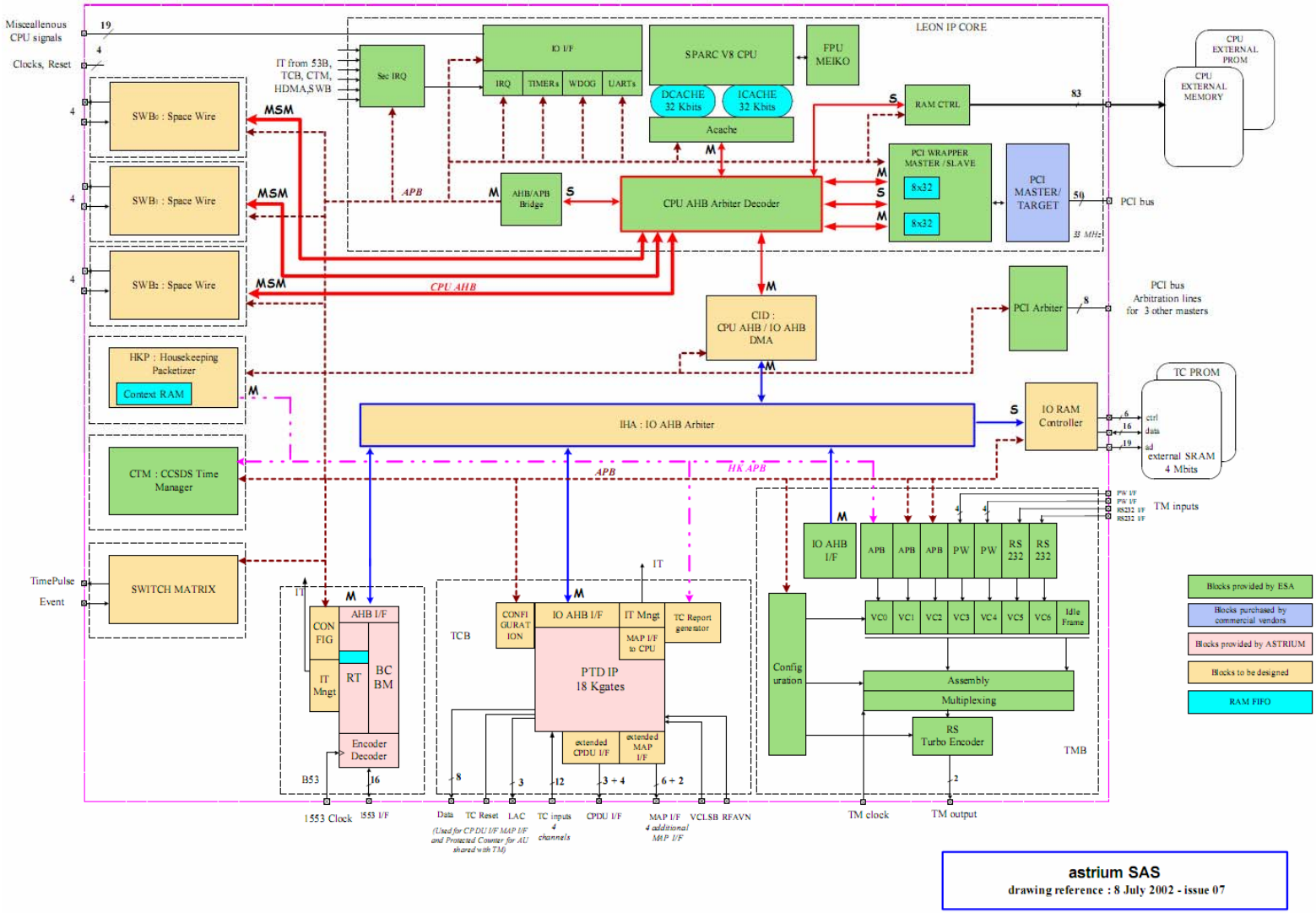
SCOC Applications

- Multiple spacecraft types…
  - Telecommunication satellites
  - Earth Observation and Science
  - Microsatellites
  - Launchers
  - Probes
- … different mission duration, availability and cost requirements
  - High reliability
  - Low cost
- Diverse architectures
  - Simplex
  - Duplex with cold redundancy
  - Duplex with hot redundancy
  - Triplex redundancy
  - Replace components of existing architecture

SCOC3 Specification

- LEON3-FT with GRFPU-FT at 120 MHz
- Dual AMBA-AHB bus architecture
  - CPU bus and IO bus may operate at different frequencies
- CCSDS TM/TC interfaces
  - MAP interface for cross-strapping
- OBDH interfaces
  - 1553, Spacewire, CAN, UART
- Other resources
  - CCSDS Time management, housekeeping telemetry packetiser
- Power management
- Debug facilities
  - IP Monitor: AMBA statistics and trace for peripheral bus
  - LEON DSU for CPU bus
- Target technology: ATC18RHA, package BGA472

SCOC1 Architecture

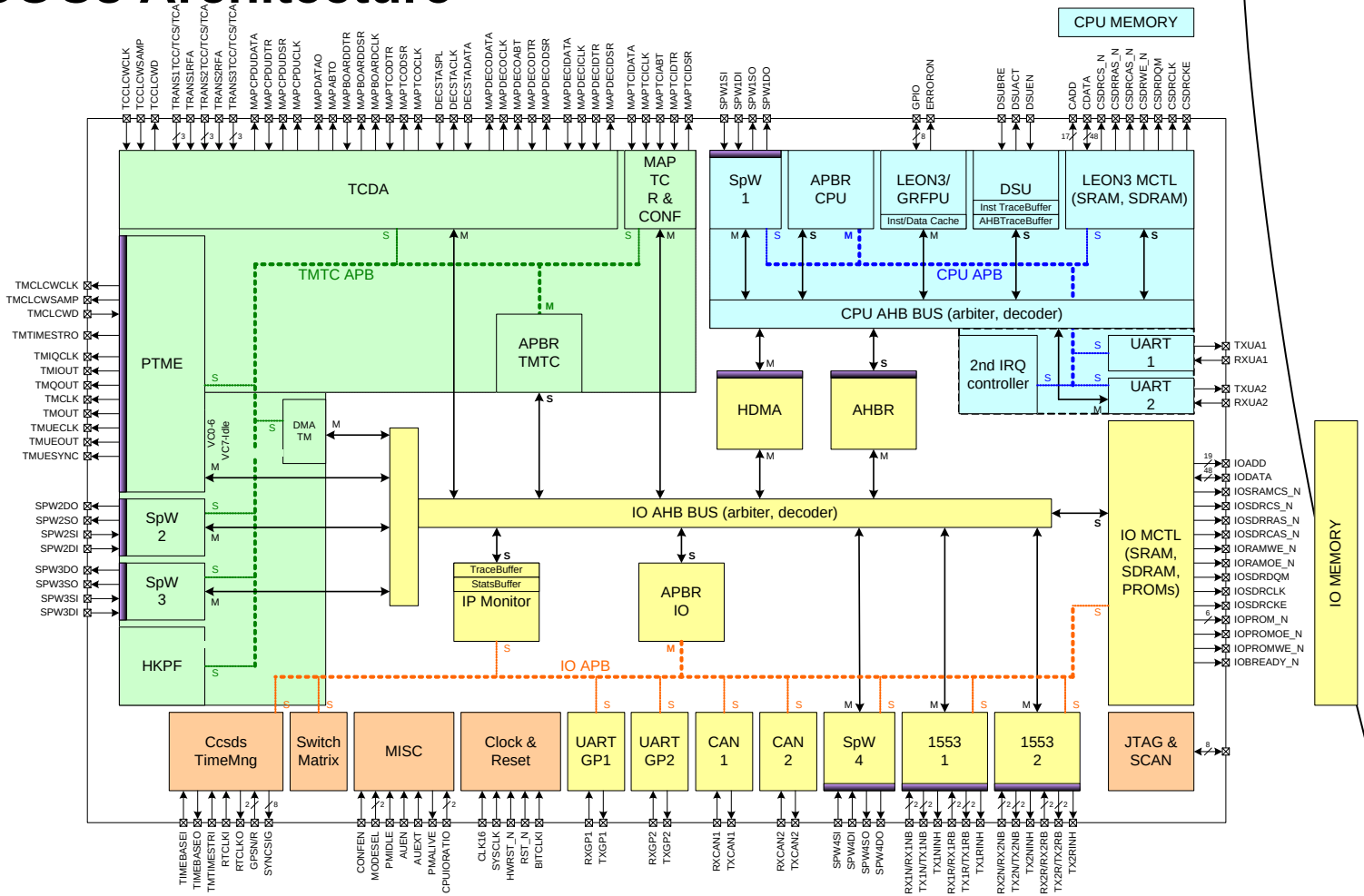


SCOC1 → SCOC3 Evolution

SCOC uses IP cores of diverse origin (Astrium, ESA, Gaisler Research)

Function	SCOC1	SCOC3
CPU	LEON1 with Meiko FPU	LEON3 with GRFPU (target 120 MHz)
Memory Controller	SRAM only	SRAM, SDRAM with Reed-Solomon ECC
On-chip bus	Dual AMBA-AHB at equal frequency, DMA bridge	Dual AHB, different frequencies, modified structure, DMA and write-through bridge
Spacewire	3x SPW-AMBA (new IP)	4x SPW, upgrade to RMAP standard
CCSDS Telemetry	PTME	PTME with DMA extension
CCSDS Telecommand	PTCD derived from ASIC	PTCD evolution to TCDA
Other interfaces	1x1553, 1x PCI	2x1553, 2xCAN, 2xUART
Debug units		LEON3-DSU IO-AHB trace and statistics IP
Miscellaneous	CCSDS Time management, event switch matrix, housekeeping packetiser	CCSDS Time management, event switch matrix, housekeeping packetiser

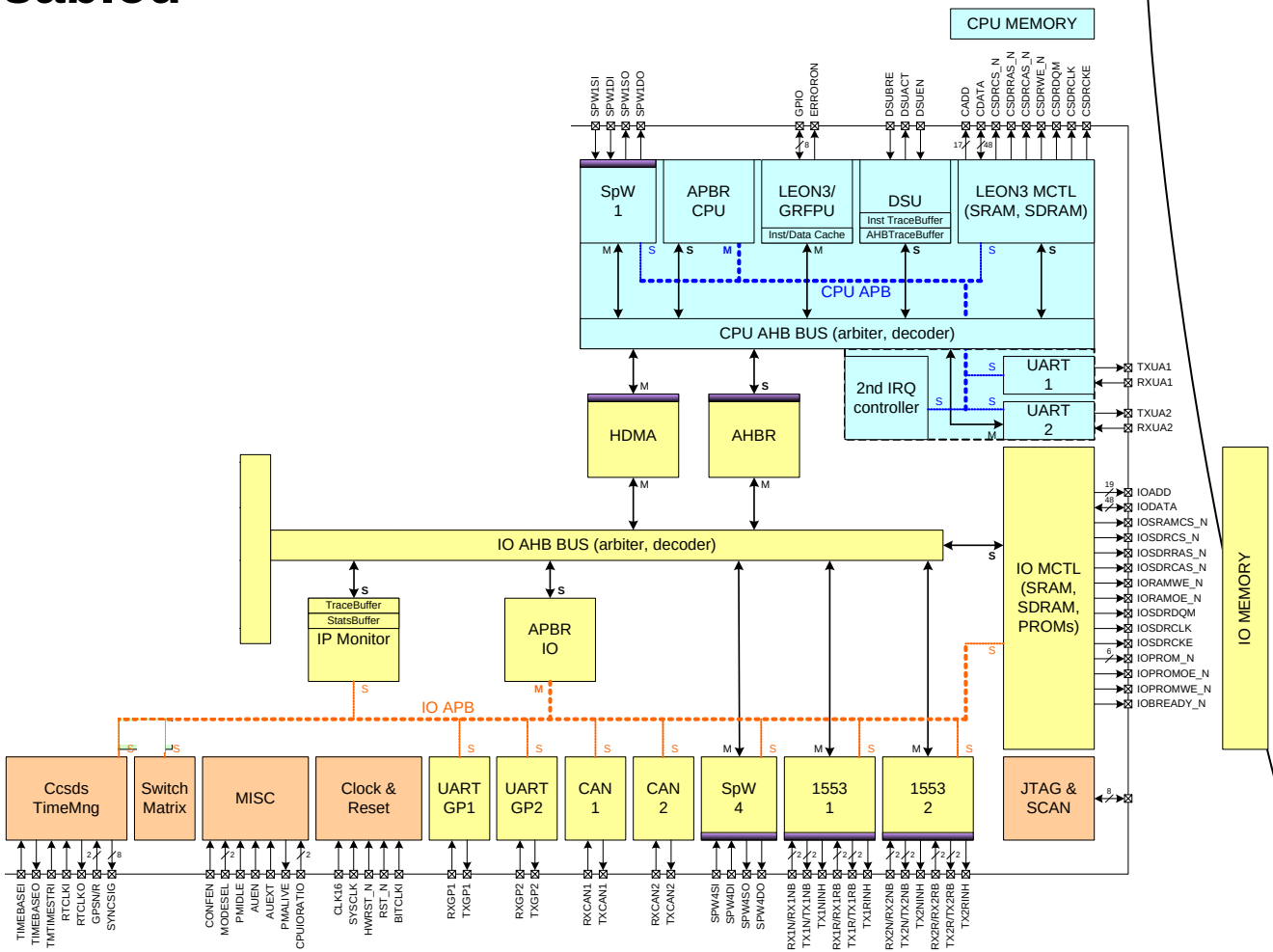
SCOC3 Architecture



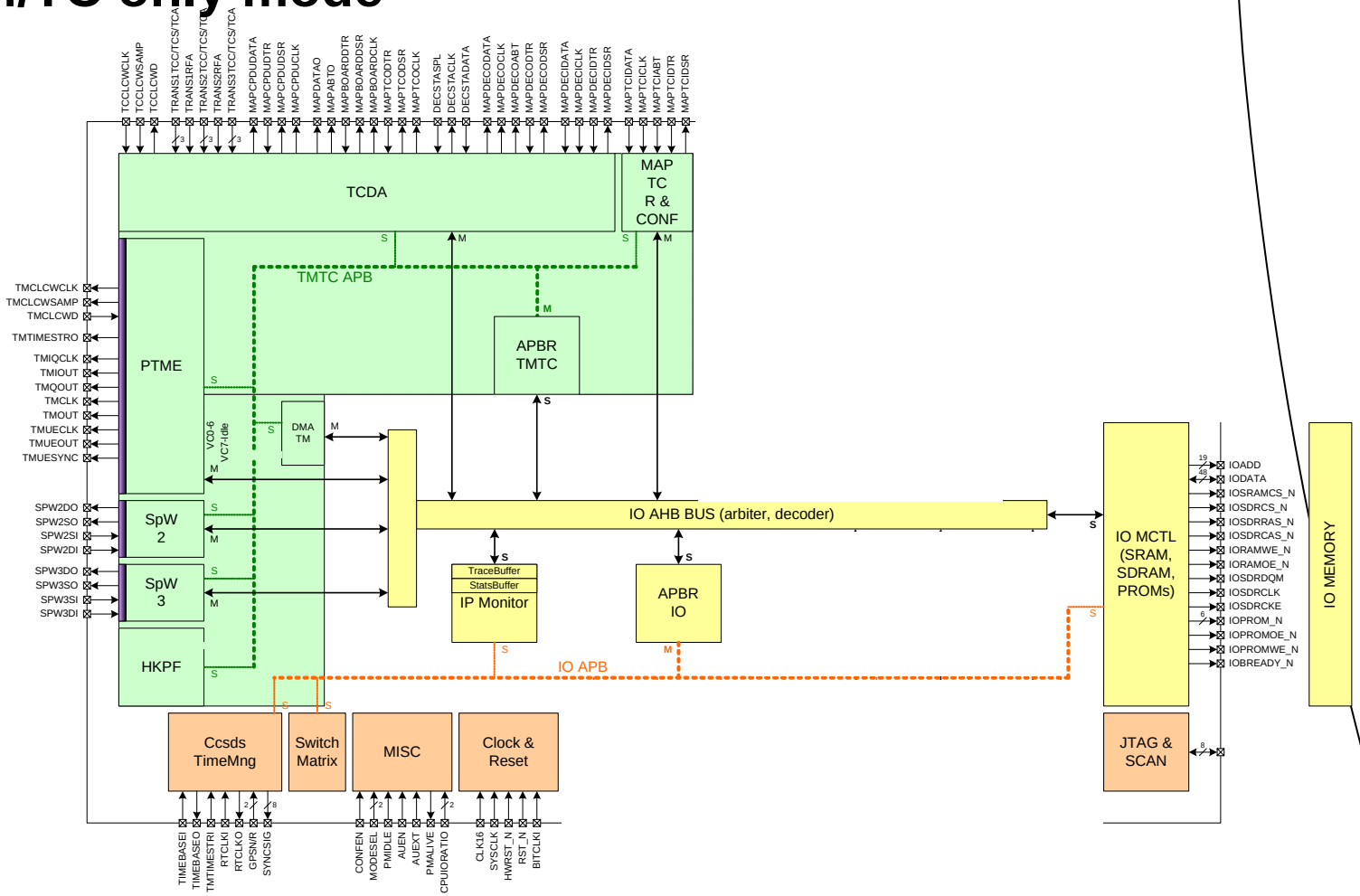
SCOC3 Operating modes

- Bootstrap pins to disable part of SCOC3
  - Power consumption scales with system requirements
- Full mode
  - SCOC3 as spacecraft main computer for control and data handling
  - SCOC3 may also take over payload processing
- TM/TC disabled
  - Processor and I/O only
  - SCOC3 can be used for payload data handling and processing
- TM/TC only – CPU and I/O disabled
  - SCOC3 replaces conventional TM/TC subsystem using ‘discrete’ components
  - Configuration from PROM without CPU intervention
- I/O disabled
  - SCOC3 as main computer with separate on-board communication structure

TM/TC disabled



TM/TC only mode



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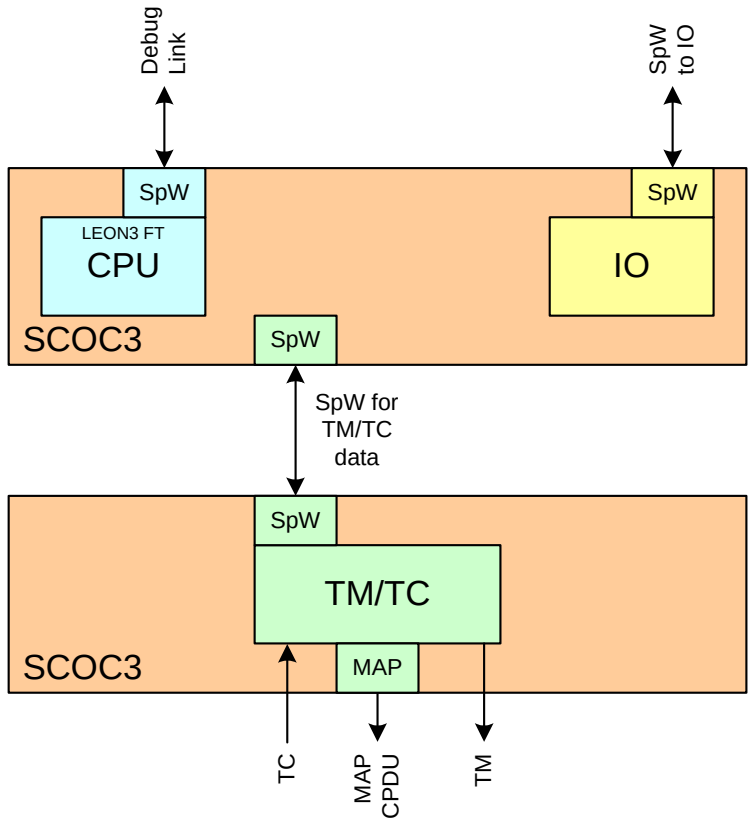
ESA

Redundancy concept: different architectures

Architectures	Simplex	Duplex (hot)	Duplex (cold)	Duplex (two CPU/IO chips and two TM/TC chips)
CPU SpW	Any use (ground debug link,…)	Any use but mainly Inter Processor Link between the CPU SpW of the two SCOC3	Any use (ground debug link, context memory,…)	Any use as direct connection between SCOC3 (CPU/IO) to SCOC3 in TM/TC operating mode
MAP Interface	Connection to MAP internal on boards	Cross-strapping of the received TC between the MAP interface of the two SCOC3	No cross-strap and data pass over IO SpW for context storage	Cross-strapping of the received TC for the two SCOC3 in TM/TC operating mode
CLCW	N/A	Cross-strapping of CLCW word between the two SCOC3	No cross-strap and data pass over IO SpW for context storage	Cross-strapping of CLCW word for the two SCOC3 in TM/TC operating mode
IO SpW	Any use (IO connection link,…)	Cross-strapping between the two SCOC3	Cross-strapping to a Context memory	Connection between SCOC3 (CPU/IO) to SCOC3 in TM/TC operating mode
TM/TC SpW	User TM external access	User TM external access	User TM external access	User TM external access

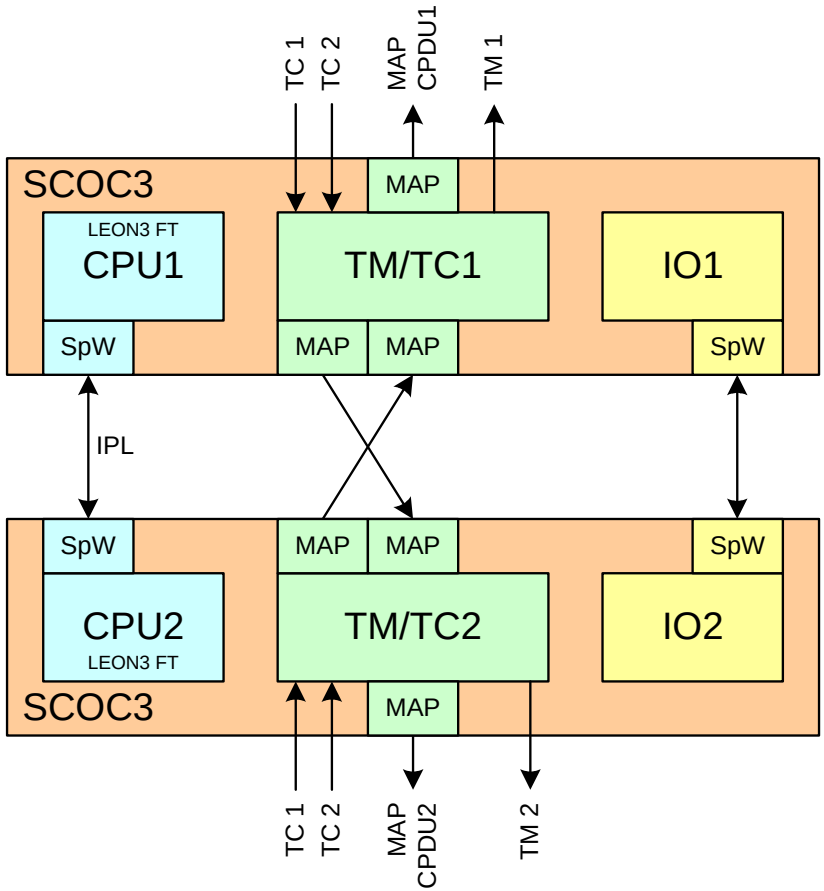
Simplex architecture with two chips

- Spacewire interfaces based architecture



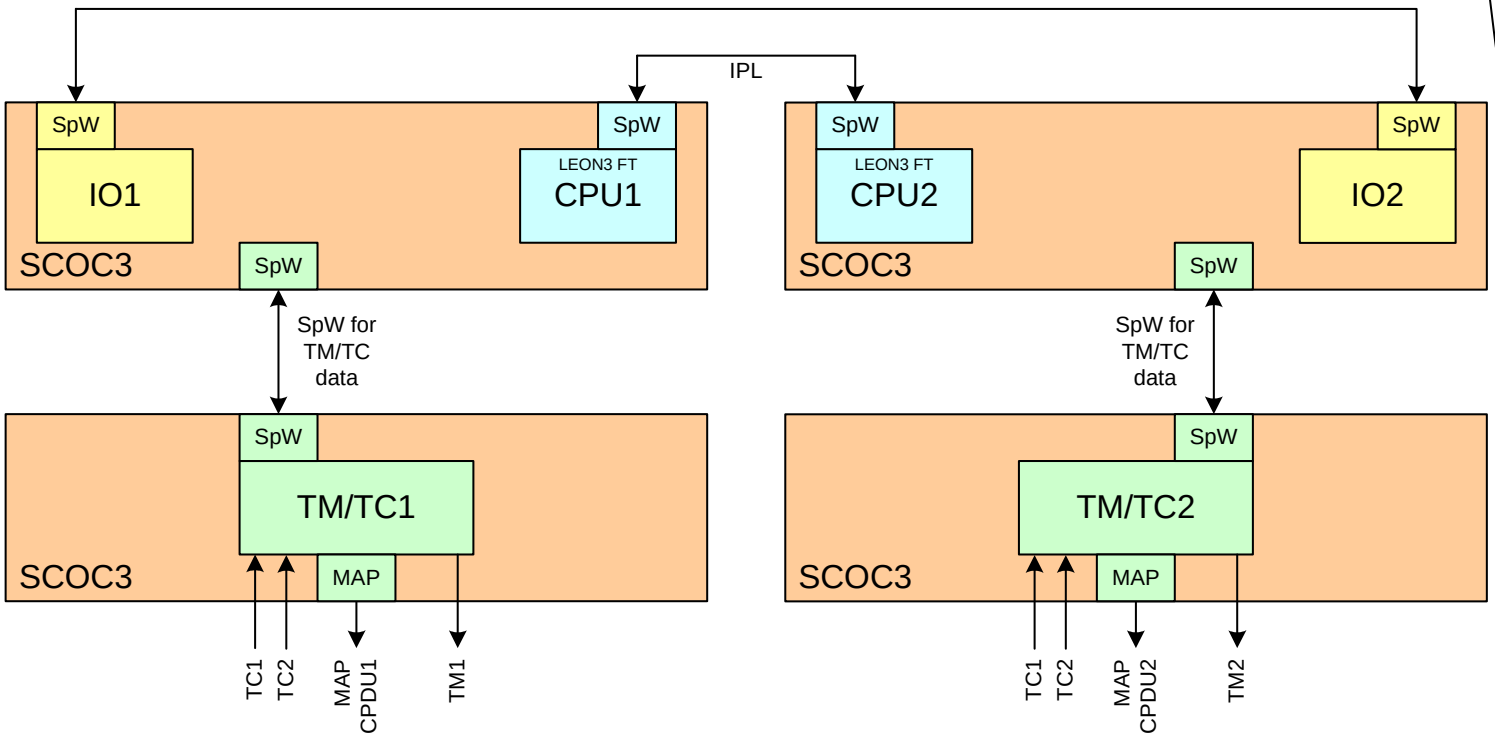
Cross-strapping with SCOC3

- Hot redundant architecture with MAP and Spacewire interfaces



Cross-strapping with SCOC3 and two chips

- Spacewire interfaces based architecture

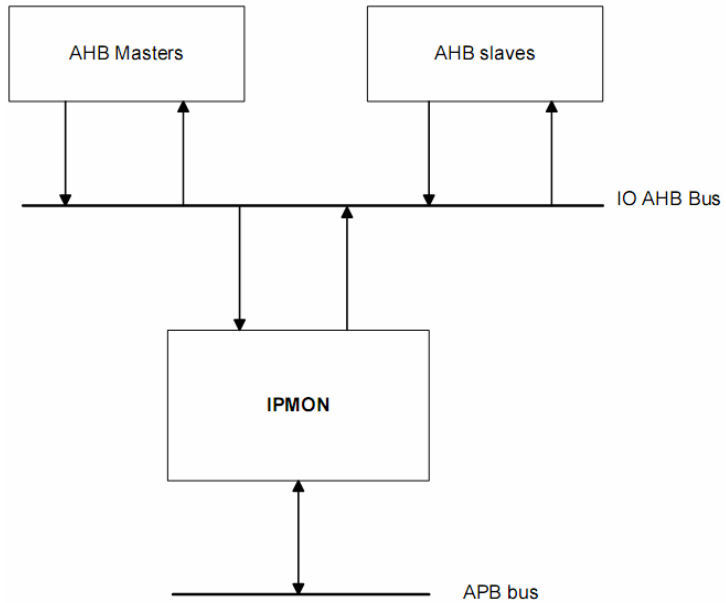


SCOC3 Software Environment

- Software sources
  - 3rd party commercial software
  - open source software
  - dedicated development
- Elements to be developed/procured
  - Drivers with IPs
  - Development environment based on C
  - Tools: GRMON, TSIM, …
  - SCoC3 simulator created
  - RTEMS and/or VxWORKS Operating System
  - Service Interface software
  - Reuse of DHS layers from Pleïades or Bepi-Colombo

Debugging with AHB statistic monitor (IPMON)

- Trace buffer depth is limited
  - 1k bus transactions ~ 10 - 100 us
- Performance monitoring by counting
  - Successful bus cycles
  - Master/Slave Wait states
  - Retry, Split, Lock, Error
  - Grant delays
- Statistics by master/slave pair

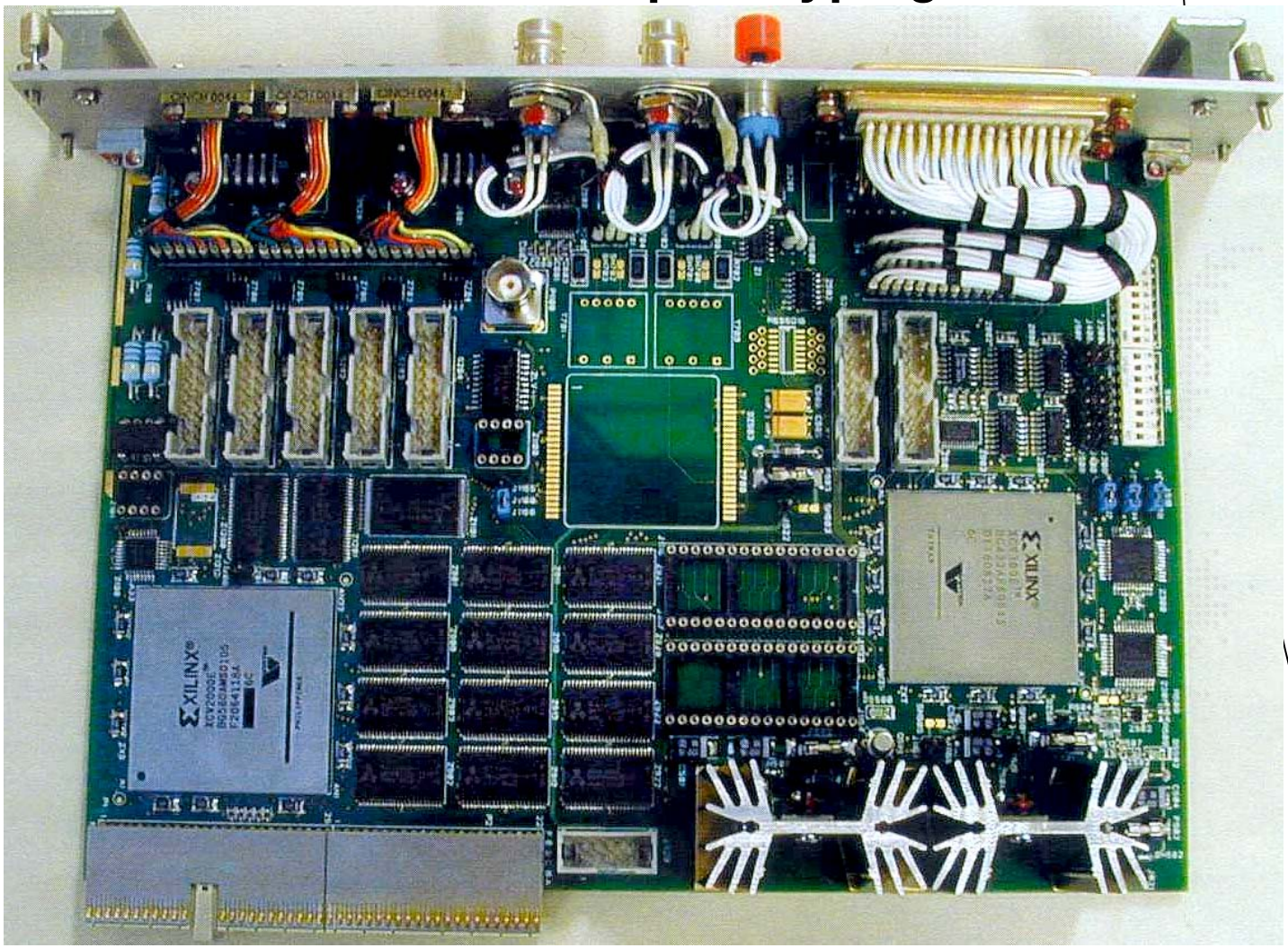


- Counting intervals defined by multiple watchpoints, triggering on
  - AHB address/data pattern/range, read/write transaction, AHB response
  - Access by/to a certain master/slave
  - and/or combination of different conditions
- Statistics readout via AHB

SOC Development methodology

- Standardization of the interfaces…
  - … on-chip using IP cores
    → AMBA standard with GRLIB extension
  - … off-chip to reduce number of IP to develop
    → Spacewire to replace other on-board interfaces?
- Verification methodology
  - Limited scope of RTL simulation
    → At top-level only for basic checks and debugging
  - Hardware/Software Co-simulation
    → Testbench environment with emulators
  - FPGA prototyping
    → A new breadboard was developed

The BLADE Board for SCOC1 prototyping



The BLADE Board for SCOC1 prototyping

Board for LEON and Avionics DEmonstration (BLADE)

- XCV200E for SCoC
- PROM/SRAM
- XCV300E for test support
- Board configuration
- Spacewire interfaces
- 1553 interface
- TM/TC interfaces
- CPCI connector
- Test point connectors
- DC/DC power regulation

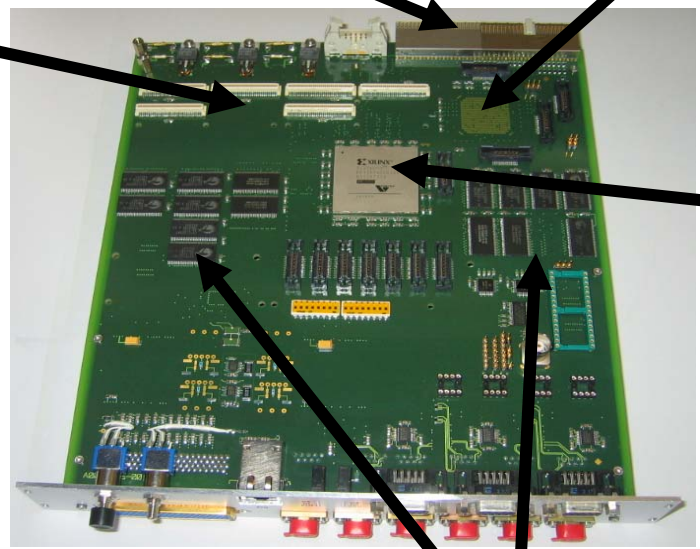
MAEVA Prototyping board for SCOC2 and AT697

Microsat Astrium Enhanced Versatile Architecture (MAEVA)

Standard CPCI connector

Slot for AT697

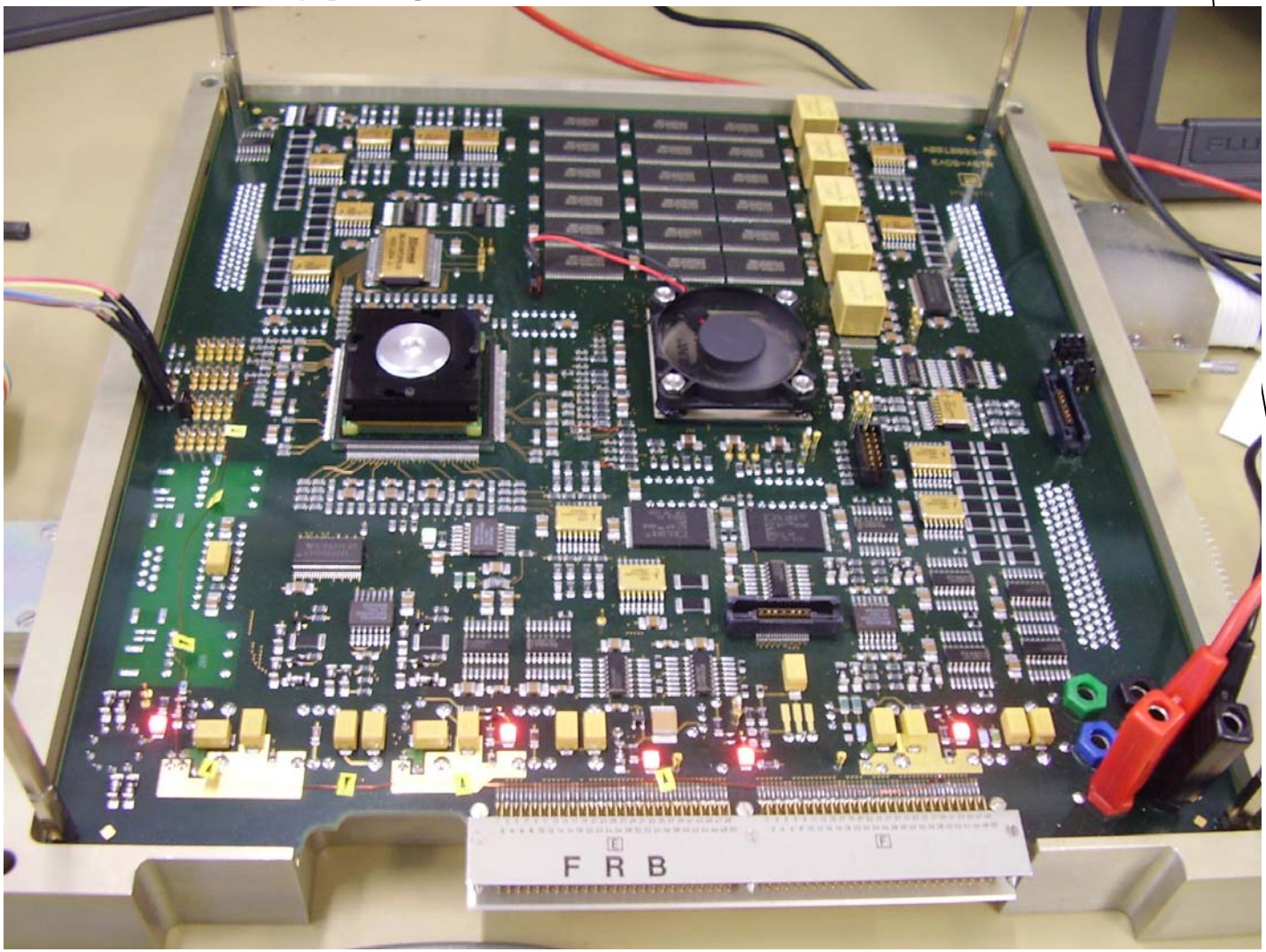
2 standard PMC Slots



XC2V6000 or XC2V8000

CPU and IO S(D)RAM NETROM footprint

Virtex 4 Prototyping board



Virtex 4 Prototyping board

- Xilinx Virtex 4 LX 200
- Actel SX72
- Banks of SDRAM (CPU and IO AHB busses)
- Banks of EEPROM (IO AHB bus)
- LVDS drivers (Spacewire, Fast signals)
- 1553 interface (transceiver and transformer)
- TM/TC interface
- RS422 drivers
- Test connectors
- DC/DC interface

Conclusion

- SCOC3 - a versatile SOC component to be made available as commercial product (ASSP)
- Functional blocks and operating modes allow its use in
  - Spacecraft control, TM/TC
  - On-Board Data Handling and communication
  - Payload Data Processing
  - … or a combination: Single chip spacecraft controller
  - Cross-strapping interfaces supporting diverse cost/availability concepts
- First ESA project using LEON3/GRLIB on a space-qualified ASIC
- Accompanied by software/driver development
- Contacts
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