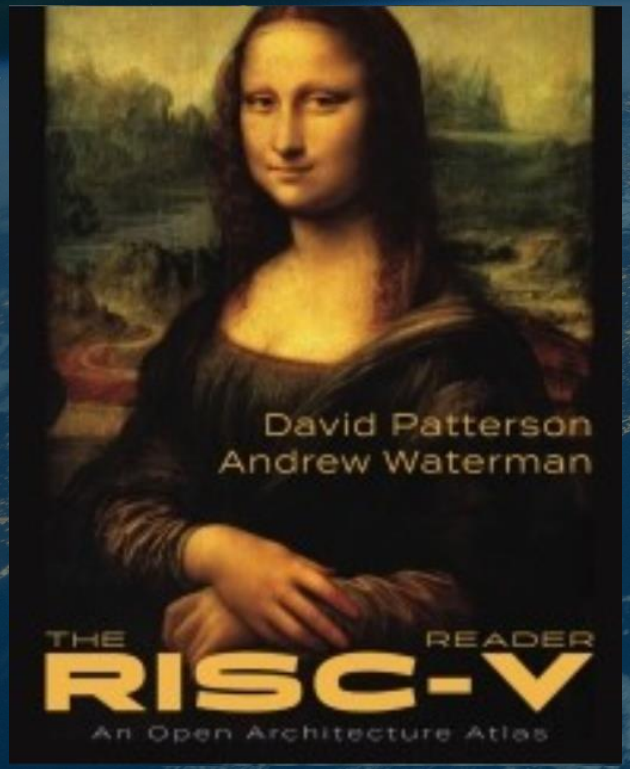


RISC-V
First Steps Into Space

18 November 2021

Roland Weigand, ESA Microelectronics Section
(contributions by G. Furano, S. di Mascio, W. Roenninger, K. Appels)

Four Generations SPARC in space

- ERC32 – Based on a commercial SPARC-V7 IP-core
  - TSC69xx standard microprocessors products by Atmel
- LEON2 SPARC V-8 IP-core owned by ESA
  - AT697F by Atmel, several ASSPs (AGGA-4 etc) and proprietary ASICs
- LEON3 IP-core owned by CAES (aka Cobham Gaisler)
  - GR712RC dual-core processor, ASSPs (SCOC3), ASICs, many FPGAs
- LEON4/5 IP-cores, introducing L2 cache and dual-issue (LEON5)
  - GR740 / GR765 standard microprocessors

SPARC Compliant SCD V8

- SPARC is now in all our missions – 1000s of flight parts – a success story
- Demand in space continues, but SPARC is obsolete in the commercial world

What's next?

What is RISC-V – and what it is not

- RISC-V is not a processor chip, and it is not a processor IP core
- RISC-V is an **open Instruction Set Architecture** (ISA)
  Specification is public and free for use https://riscv.org/technical/specifications/
- Other ISA's may be open, but not free (e.g. ARM, Intel)
  You will be sued if you design and sell a processor based on their spec
  You can license their IP, but are usually not allowed to modify it
- RISC-V is not an open source IP – IPs can be open source, commercial, or proprietary
  - Many open source IPs exist (e.g. Rocket, Shakti, NOEL-V)
  - Commercial IP vendors (e.g. Andes/Taiwan, SiFive/US)
  - Proprietary chip developments (e.g. AliBaba XT910…)
- RISC-V is highly scalable (32-/64bit, standard extensions)
  - Prepared for custom extensions
- RISC-V seriously threatens the market of ARM & Co

RISC-V®
RISC-V: The Free and Open RISC Instruction Set Architecture

Why RISC-V?

25 years ago, ESA has selected the SPARC open ISA to build a very successful range of space microprocessors
→ RISC-V, like SPARC, is also an open ISA

RISC-V defines a versatile instruction set from microcontroller to high performance computing and AI
→ Several interesting standard extensions (V = vector, P = packed SIMD, H = Hypervisor)
→ Room for custom extensions for specific applications

RISC-V is suitable for security evaluation and radiation mitigation
→ Thanks to competing IP vendors or open source IP, access, evaluation and modification of IP is easier

RISC-V provides independence from single sources, countries and export restrictions
→ The non-profit RISC-V Foundation is incorporated in Switzerland, a 'neutral' country, many independent IP vendors

RISC-V does not come for free, but at fair cost
→ Good quality IP and support will never be for free
→ thanks to competition, the cost will likely be lower and license negotiations easier

RISC-V seems the most obvious choice for space, and it should be preferred over proprietary architectures.
Space is intrinsically different with respect to commercial mass market.

Goal: Standardize the use of RISC-V ISA for all our computing products (HPC, AI, uC, FPGA, COTS)
One ecosystem for different product classes → Benefit / cost saving on the SW side

RISC-V R&D for Space

RV4S - RISC-V in space applications

- http://microelectronics.esa.int/finalreport/FR-RV4S-FR-0013-i1r0.pdf
- Cobham Gaisler, University of Nebrija Madrid (ES), QinetiQ (BE)
- Comparison of RISC-V IP cores (Rocket, LowRISC, Boom, SHAKTI, Pulp)
- Selected Berkeley Rocket IP
- SEU mitigation (TMR…) on Xilinx Ultrascale FPGA
- Fault injection, SW Ecosystem
- ITI contract 175 k€
- Completed 12/2019

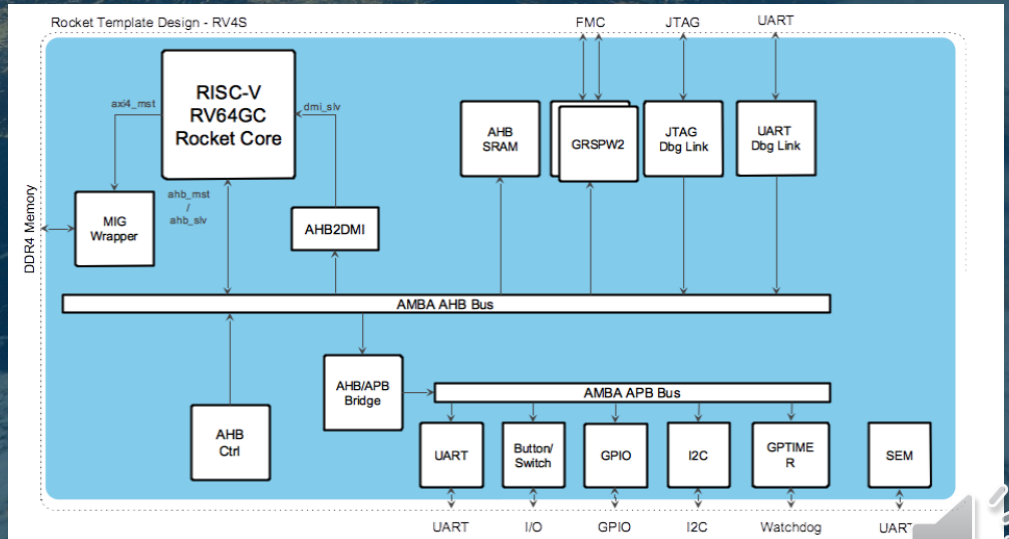


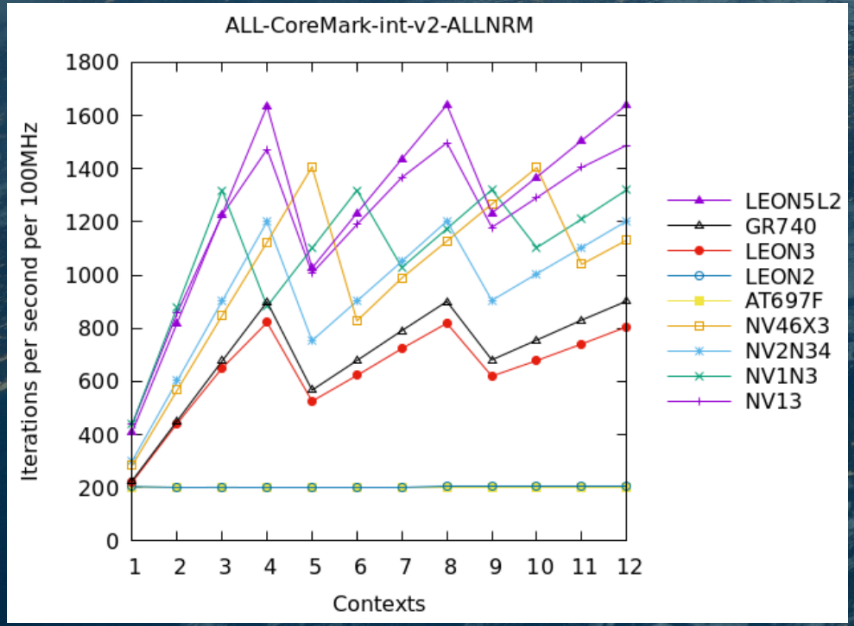
Figure 1: RV4S SoC Block Diagram

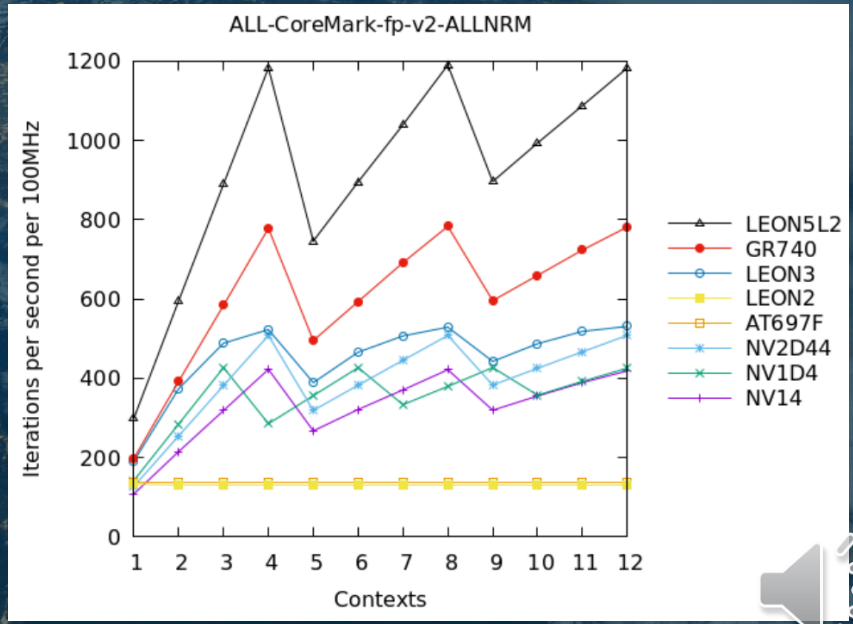
Evaluation of and extensions for NOEL-V

- Contractor: DAITEQ (CZ)
- Extensive benchmarking
  - PWLS : Paranoia, Whetstone, Linpack, Stanford
  - Coremark, Coremark-Pro, FPMark
  - Comparison of NOEL-V, LEON's and PolarFireSoC (SiFive cores)
- Adaptation of DaiFPU (originally designed for LEON2) to NOEL-V
- SIMD Instruction extensions
  - SWAR = SIMD Within A Register
- Work in progress (see next slide)

Comparative benchmarking NOEL-LEON

- http://microelectronics.esa.int/riscv/Daiteq-LEON-NOELV-Benchmark.pdf (draft, in progress)
- Left: NOEL-V outperforms LEON2/3/4 on integer workloads
- Right: NOEL-V slower on FP workloads, only a light FPU is currently available





VGSM Phase 1: RISC-V Test Chip in UDSM

- **VGSM**: 5th Generation Space Microprocessor
  = following 4 generations of SPARC (ERC32, LEON2, LEON3, LEON4)
- TDE Tender in open competition in preparation (ITT issue Q4/2021)
- 450 k€ Technology Budget Approved (TDE)
  - Select and tailor RISC-V IP core and associated peripherals
  - HDL implementation / verification
  - Define and implement the radiation hardening(-by-design) concept
  - ASIC prototype in a Multi-Project-Wafer (MPW), UDSM <= 28nm
    - → reduced configuration (budget-driven, less cores / memory)
  - Functional tests, benchmarking, radiation tests (TBC)

GR7xV - Multi-Core NOEL-V

- ESA contract with Cobham Gaisler
- 1st Phase budget approved (Sweden), covering
  - Implement and verify chip design in HDL
  - Select ASIC technology (ST 28FDSOI, GF-22FDX, or smaller?)
  - FPGA prototypes
  - Implement evaluation board
  - Perform functional tests and benchmarking
- 1135k€ (co-funded: 850k€ public + 285k€), kicked off in Q3/2021
- Industry driven ARTES activity

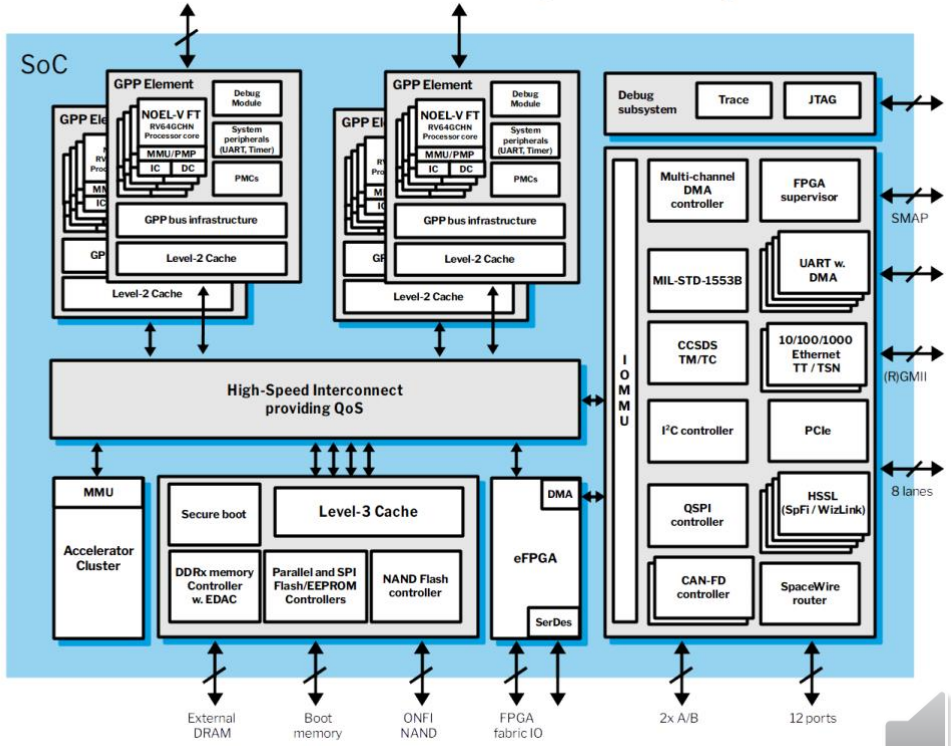
GR7xV – 16-core NOEL-V Processor

CAES PIONEERING ADVANCED ELECTRONICS

In development
No guarantee of product launch

Baseline Features

- Fault Tolerant 64-bit RISC-V Hexadeca-core with islands of 4 general-purpose processors each with dedicated L2 Caches
- Accelerators for high-performance computation
- eFPGA fabric for glue logic
- Minimum performance targets:
  - GPP: 19.2 GOPS, 9.6 GFLOPS, 7700 DMIPS – 31000 DMIPS
  - Accelerator: 1.23 TOPS of INT8.32 for MDL, 19 GFLOPS FP16, 8.5 GFLOPS FP32
  - TID: target 100 krad(Si)
- DDR2/3/4 SDRAM, SPI and NAND memory I/F (w. EDAC)
- CCSDS TM/TC functions on-chip
- Increased focus on cyber-security and isolation (processor and SoC design features)
- Software support effort on the way: XtratuM support provided before component launch
- First available in plastic package, ceramic later
- Target technology: TBD



GOMX-5 APPs (Advanced Payload Processors)

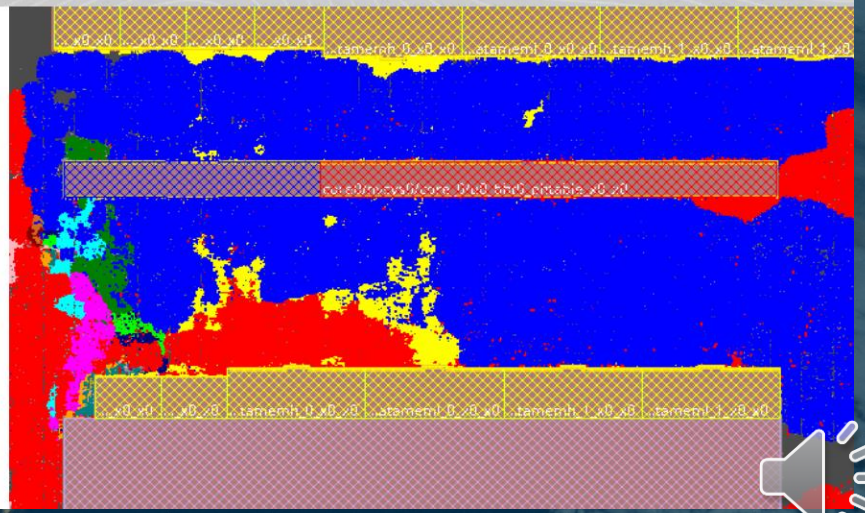
- GOMX-5 Cubesat by GOMspace, launch planned 2022
- IOD Payload unit with 5 PCI104 boards (10x10x10cm)
- First (TBC) space flight of NOEL-V

LEON5 and NOEL-V on STM 28nm GEO P2

CAES PIONEERING ADVANCED ELECTRONICS

Rad-hard demonstrator with LEON5FT SPARC V8 32-bit processor and NOEL-V RISC-V 64-bit processor

- ST 28nm FDSOI GEO P2 technology
- Specialized design with LEON5 and NOEL-V sharing resources, consumes less than 1 mm^2
- Proves implementation on target technology.
- Technology hardness and processor core fault tolerance features will be demonstrated through SEE test campaign.
- Collaboration between STM and Gaisler R&D teams
- Manufactured using European supply chain, fab in Crolles (FR)



TRISAT-R mission

TRISAT-R

3U CubeSat mission targeting a MEO orbit and objective to perform a radiation analysis with four scientific payloads for radiation monitoring and IOD of several other technologies.

Mission and technologies

- IOD of a highly miniaturized nanoscale platform with fault tolerant features
- **IOD of first RISC-V processor (NOEL-V) in Space by CAES (Cobham Gaisler)**
- Provide mapping of ionizing radiation and radiation effects with on-board instruments:
  - RadMon from CERN
  - CHIMERA RHA from ESA
  - TID monitor from SkyLabs

- Prime University of Maribor, Slovenia
- Status **Phase D**

- Launch vehicle VEGA-C maiden flight in 2022
- Orbit MEO, 5865 km,
- Platform **NANOSky I (1st generation) avionics**
- Dimensions Nanosatellite, standard 3U form factor
- Communication UHF/VHF (GFSK)

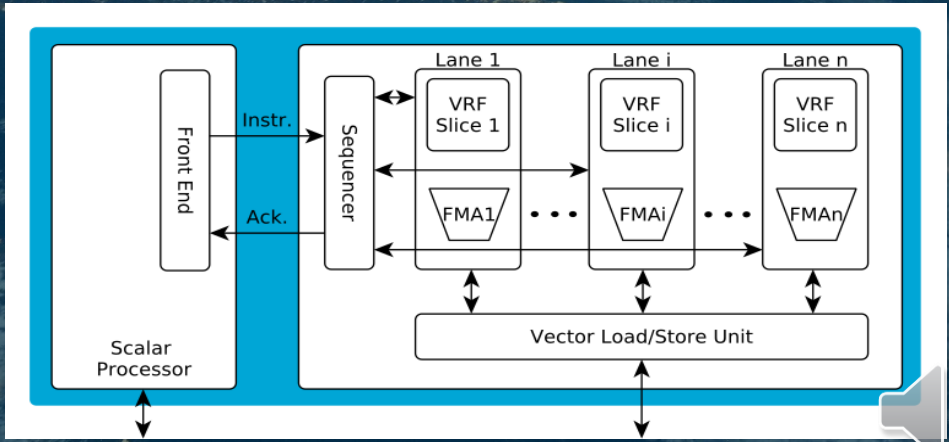
NANOhpm-obc

High Performance Fault Tolerant RISC-V OBC

- Fault Tolerant **NOEL-V processor** @ 80 MHz
  - **RISC-V** 32-bit architecture
  - Single precision FPU / L2 cache
  - Implemented on Microchip Polarfire
- 256 MB DDR3 memory
- 4 Mbit NMV for TM storage (unlimited read/write endurance)
- Redundant 2Gb NAND Flash for mass storage
- Redundant CAN for TM/TC
- 2x High-speed LVDS or RS422/485 channels
- 8x GPIO (with multifunction support UART/SPI/TWI and OBT trigger)
- GNSS receiver on board (GPS / GLONASS / Galileo / BDS / QZSS)
- Compatible with the PC-104 form factor.

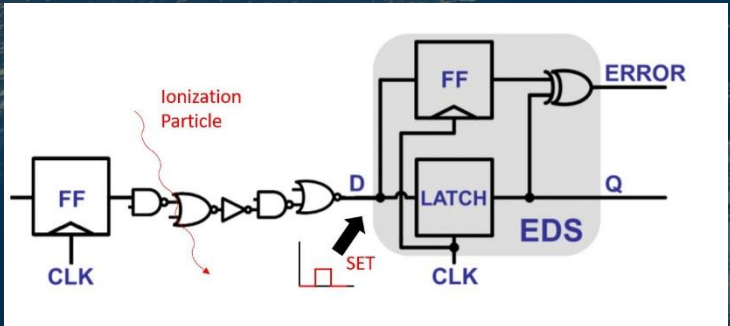
PhD work - Spin-in of RISC-V in Space

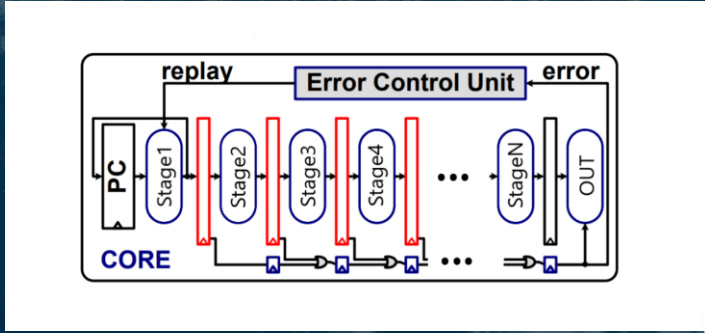
- Stefano Di Mascio, TU Delft
- *Leveraging the Openness and Modularity of RISC-V in Space* https://doi.org/10.2514/1.I010735
- *Open-source IP cores for space: A processor-level perspective on soft errors in the RISC-V era* https://doi.org/10.1016/j.cosrev.2020.100349
- Development of models to estimate the soft error vulnerability
- Feasibility study and preliminary design of a RISC-V Vector Processor
- VHDL implementation of a RISC-V Vector Processor based on the NOEL-V platform
- Matrix multiplications up to 25x faster than baseline processor (HPP64) on Kintex Ultrascale



PhD – Innovative SEE Error Correction

- Karel Appels, KU Leuven / Geel (BE)
- Detection of Single Event Transient (SET) Events in GF-22FDX technology
- Implementation of a self-correcting transparent replay execution pipeline architecture for single-event soft errors applied to a RISC-V processor
- Implementation of a self-tuned adaptive aging detection and mitigation system
- Test chip implementation in Globalfoundries GF-22FDX technology

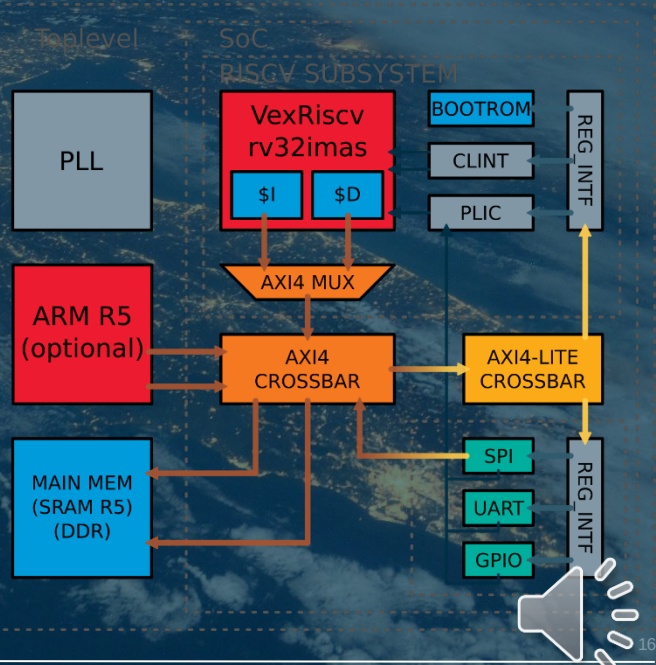




TEC-EDM internal R&D

- Wolfgang Roenninger, YGT
- Implementation of RISC-V on NanoXplore BRAVE NG-LARGE
- Open Source IPs for SoC [HDLs: Spinal, (System)Verilog]:
  - VexRiscv: rv32imas : 6 Stage : SpinalHDL
    https://github.com/SpinalHDL/VexRiscv
    - AXI4 / REG_INTF / Peripherals: Pulp-Platform
      https://github.com/pulp-platform/
    - Platform Interrupt Controller (PLIC): lowRISC
      https://github.com/lowRISC/opentitan
- Goal: Boot Linux image on NG-Large
- Frequency (typical): ~ 20MHz

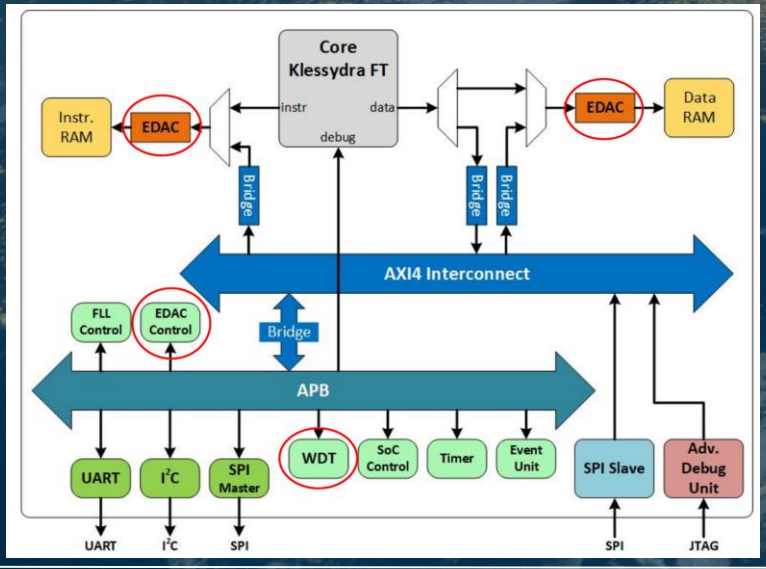
LUT	DFF	CY	RFB	CdC	CB	CS	DSP	RAM	WFG	PLL
13%	8%	13%	0%	0%	4	1%	3%	42%	3%	1

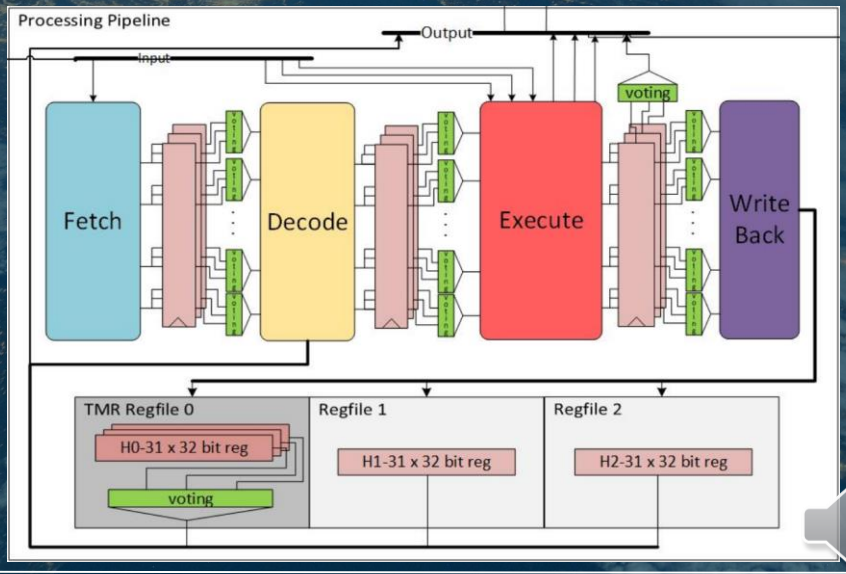


The RISC-V Klessydra Orbital Lab

- Universtity Sapienza, Rome (IT), DSI Aerospace Technology GmbH (DE)
- Based on “Klessydra” PULPino RISC-V RV32I IP core
- Various fault tolerance techniques: interleaved multithreading, TMR voting, ECC…
- Launch cubesat planned (TBC)

https://indico.esa.int/event/323/contributions/5048/attachments/3749/5205/16.20_-_The_RISC-V_Klessydra_Orbital_Lab_project.pdf

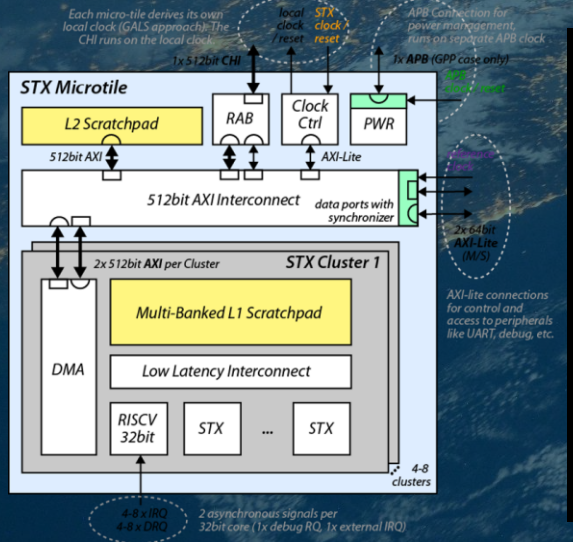


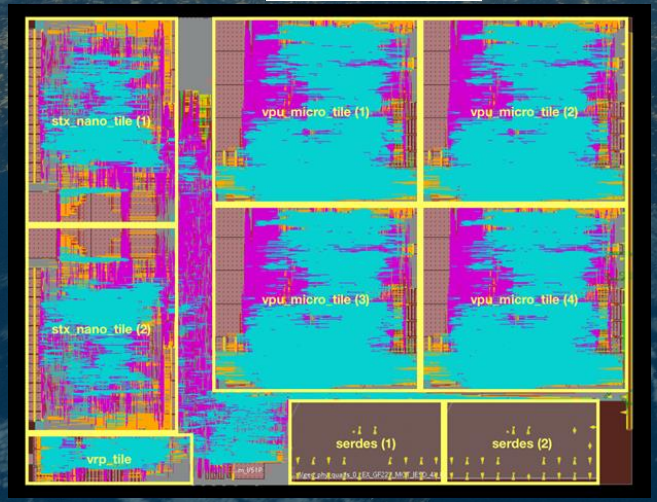


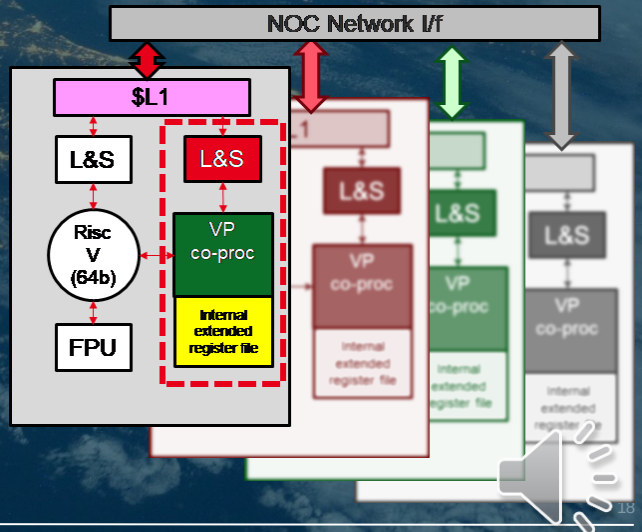
European Processor Initiative (EPI)

- EU Commission Grant 80 M€ https://cordis.europa.eu/project/id/826647 - in progress
- General Purpose Processor (GPP) based on ARM
- RISC-V Accelerators https://www.european-processor-initiative.eu/accelerator/

STX: Stencil Accelerator – EPAC Test chip in GF-22FDX (samples 9/2021) – Variable Precision Accelerator



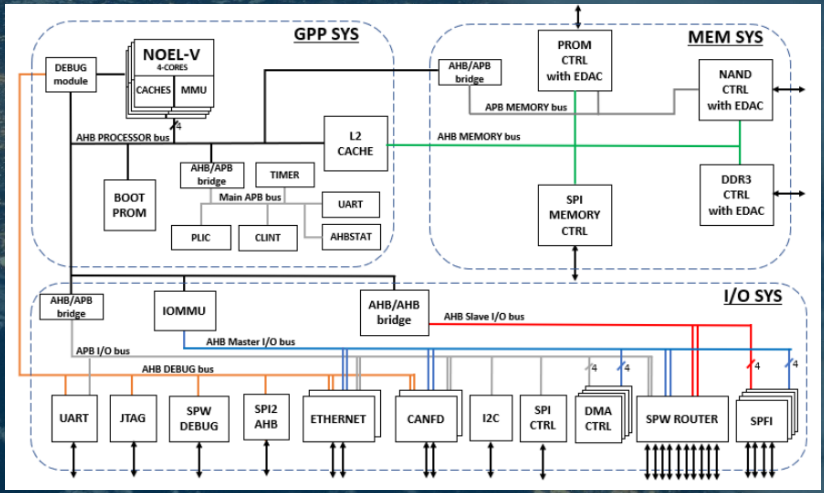




EC projects (1) using NOEL-V

- DeRISC: Dependable Real-time Infrastructure for Safety-critical Computer
  - EC Grant (2.6 M€) https://derisc-project.eu/
  - Implementation of RISC-V Hypervisor Extension
  - Multicore interference aware statistics unit
  - Multicore interference mitigation concepts
  - Hypervisor software XtratuM by FentISS (ES)

De-RISC
Dependable Real-time Infrastructure for Safety-critical Computer



- SELENE: Self-monitored Dependable platform for High-Performance Safety-Critical Systems
  - EC Grant (5 M€), https://www.selene-project.eu
  - HW Platform based on NOEL-V
  - Jailhouse open-source hypervisor (Siemens)
  - European Distributed Deep Learning Library (EDDL)

SELENE

EC projects (2)

RISC-V IP service (Codasip, CZ)

- EC grant (9.5 M€) https://cordis.europa.eu/project/881172

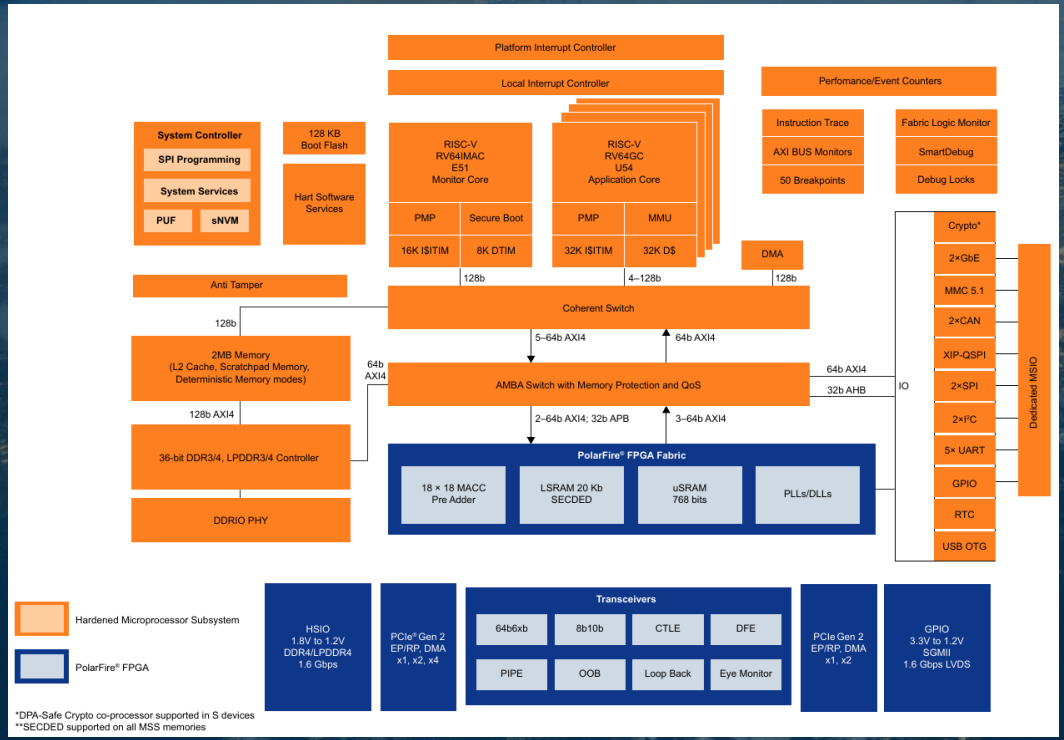
European, extendable, energy-efficient, energetic, embedded, extensible, Processor Ecosystem

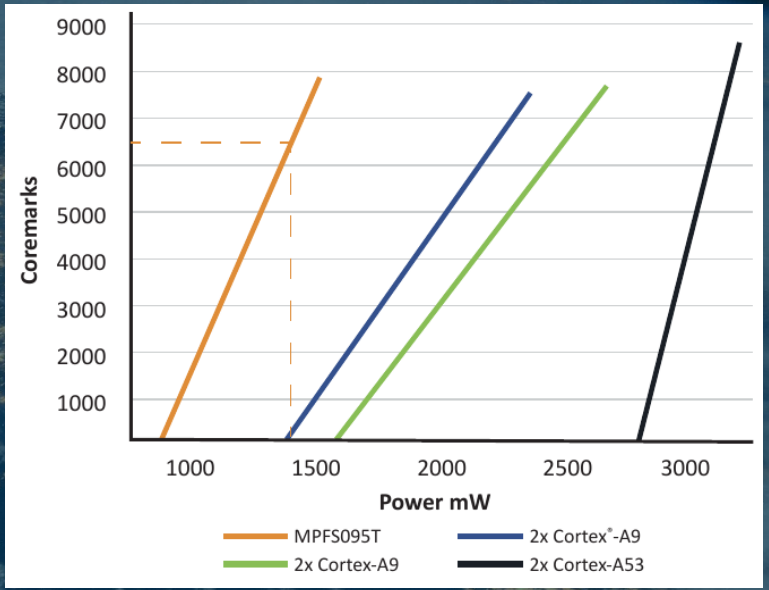
- EC Research Grant (8 M€) : https://eprocessor.eu/ , https://cordis.europa.eu/project/956702
- Development of an open source Out-Of-Order RISC-V IP (Cortus)
- Project started in April 2021
- Not space related … but the IP could become interesting for HPC
- Other Cortus RISC-V IPs have been evaluated already by a space company

Microsemi PolarFire-SOC FPGA (evaluation planned)

https://www.microsemi.com/product-directory/soc-fpgas/5498-polarfire-soc-fpga

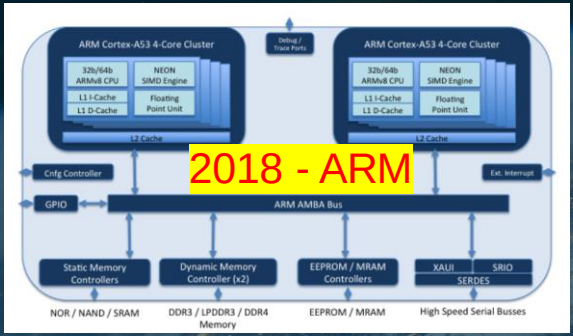
Not a space FPGA – RT to be evaluated



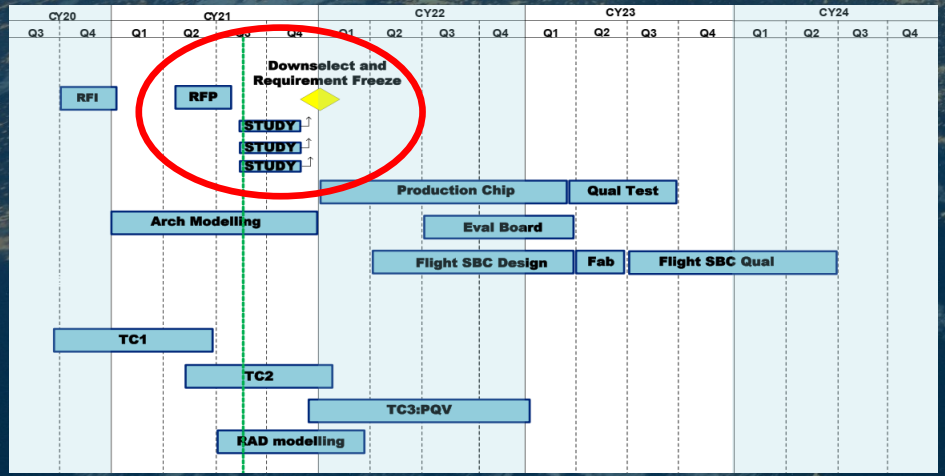


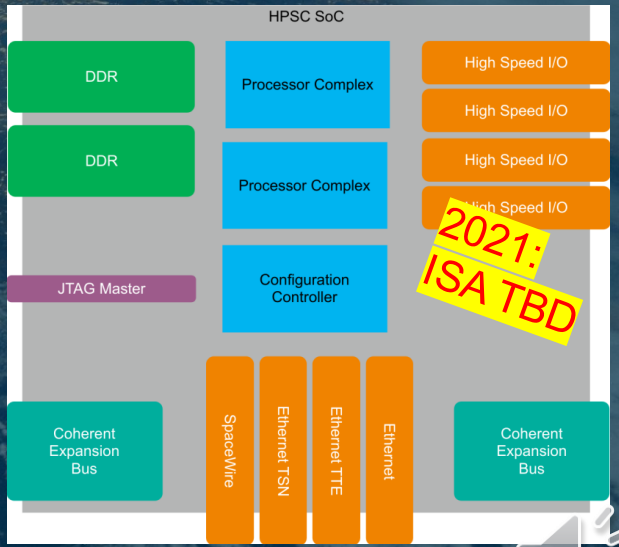
Better Performance / power ratio (source Microsemi)

NASA High Performance Space Computing (HPSC)



- 2018 plans: 32 nm SOI, ARM Cortex A53 [W. Powell, RadHard Electr Techn 2018]
- 2021 refurbishment: 22 nm (or below), ISA is not determined [J. Butler, Space Comp Conf 2021]
- 3 parallel architecture studies → trade-off ARM and RISC-V ?





Microprocessor Roadmap (ESA)

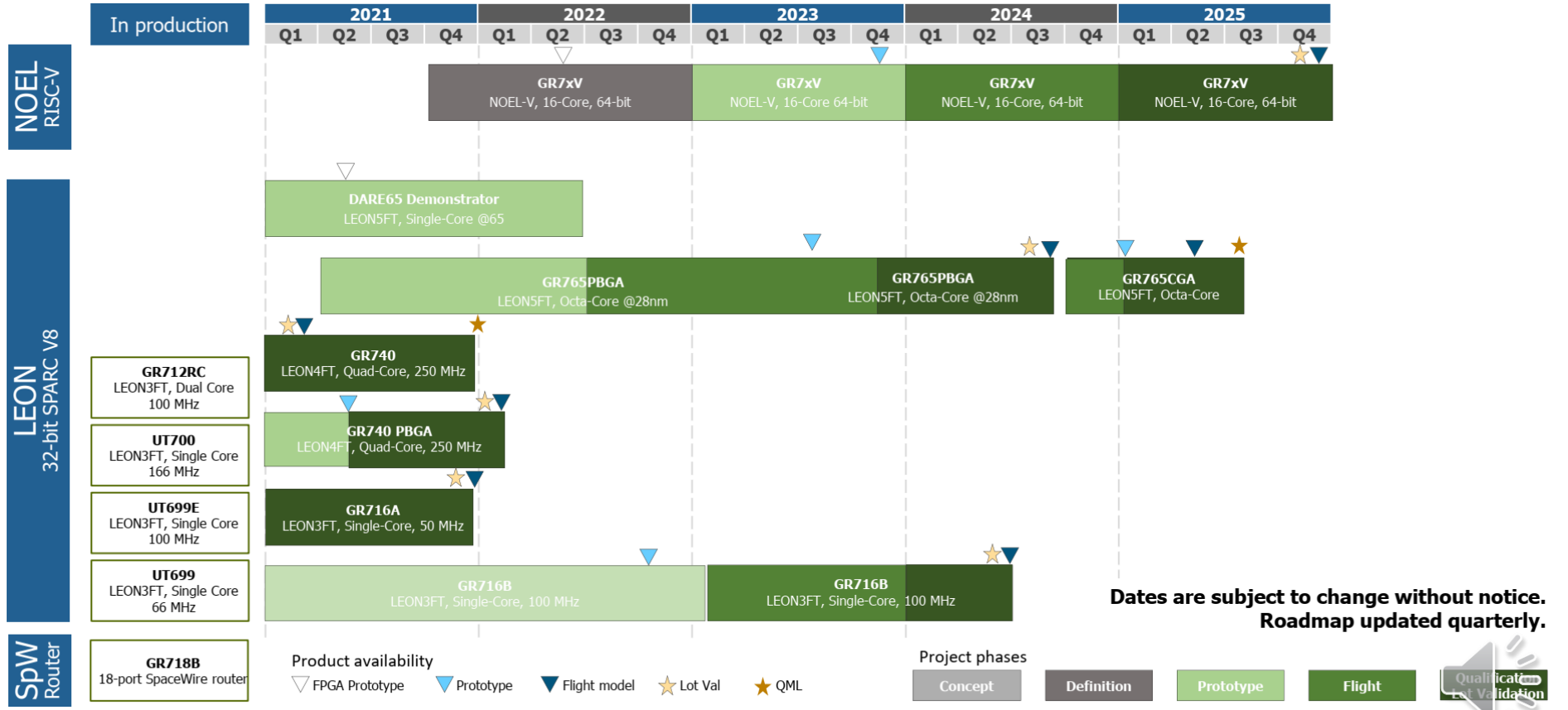
???

Unlike for previous generation microprocessor developments,
ESA leaders do not allocate substantial generic R&D budget any more
→ Proposing a generic ESA roadmap does not make sense

ESA is supporting industry driven roadmaps
… if backed up in optional ESA programmes

Computing Roadmap 2021, November

CAES PIONEERING ADVANCED ELECTRONICS



Dates are subject to change without notice.
Roadmap updated quarterly.

Conclusion

- RISC-V is not a chip or an IP-core by itself – it is an open Instruction Set Architecture (ISA)
- Several embodiments exist, open source and commercial
  - E.g. SiFive (US), Andes (TW), NOEL-V (SE), CORTUS (FR), ChiangShan (CN), Shakti (IN) …
- ISA extensions : official specifications and custom instructions
  - P = Packed SIMD, V = Vector, custom extensions possible – challenge: SW tool chain
- Several activities at ESA, EU R&D and NASA show the growing interest for RISC-V, in space and beyond
- Need to provide a SW Ecosystem: develop and (space-)qualify
  - Operating systems, hypervisor, compilers, simulators, emulators, debug tools
- ESA roadmap? – ESA management does not allocate mandatory budget for microprocessors
  - However, ESA supports industry's product lines, if backed by optional programmes
- Ideal follow-up for the successful SPARC in space applications
- Harmonisation of ISA would be highly desirable
  - Synergy of SW, SW ecosystem and know-how
  - Using RISC-V for HPC processors, SoC-FPGA and microcontrollers