ESA Microprocessor Development

Status and Roadmap

Roland Weigand

European Space Agency

Microelectronics Section

DASIA 2011

Outline

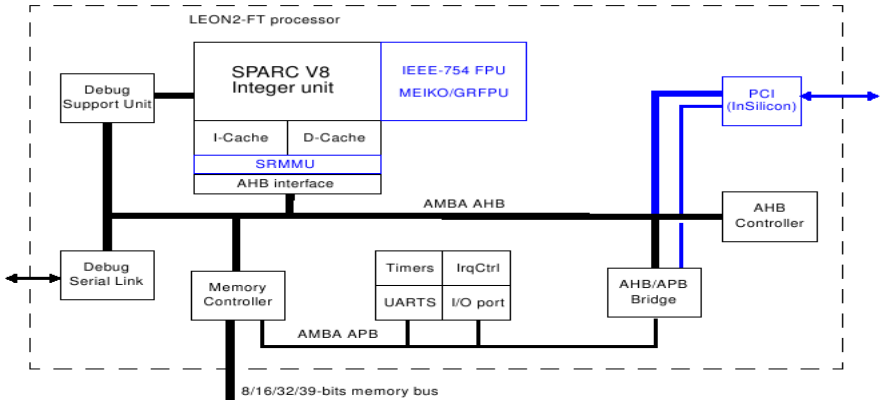
- Microcontrollers
  - Basic requirements
  - Candidate CPU architectures
  - Semiconductor Technology
  - Development activities
- LEON2 based standard components
  - AT7913E status
  - AT697 status
- LEON3 based SCOC3
  - Status
  - SW development
- LEON4 based NGMP development
  - Architecture, features
  - First Silicon Implementation
  - History and Roadmap
  - Related activities

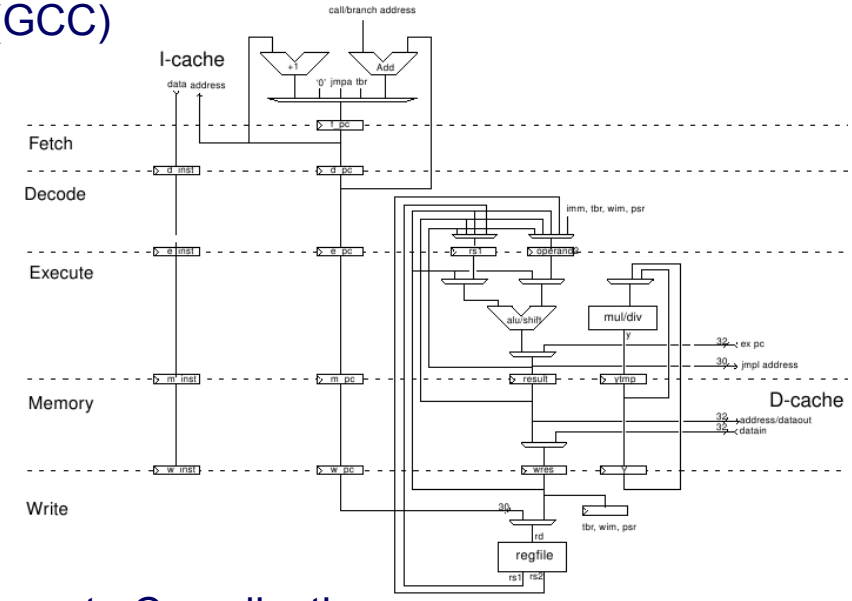
Microcontroller General Requirements

- MESA Roundtable 11/2010: http://microelectronics.esa.int/cgi-bin/mesa.cgi
- Key requirement is to limit the overall system cost
  - Affordable component price, low pin-count (<= 100) and easy-to-assemble package
  - No external RAM (~ 64 kByte on-chip) and – if possible – on-chip NV memory
  - Digital peripherals: I2C, SPI, SPW, CAN, 1553 (?)...
  - Analog peripherals: ADC, DAC, PWM / AWG, oscillator / PLL, voltage regulator
- CPU Core selection (e.g. LEONs, AVR, XAP, ARM, PIC, Opencores...)
  - Predictable CPU, caches are often not desired
  - Availability (and cost) of SW development tools
  - Adequate size of data path: 16 bit (preferred) or 32 bit (code density!)
  - Good code density to operate from embedded memory
  - Source code availability at ESA for support and inspection required
  - Availability as an IP-core for other implementations desired
- Environmental requirements
  - TID (>= 50 krad), SEE tolerance fully user transparent (no SW scrubbing)
  - Low power consumption, single rail supply
  - Space qualified component (flow TBD: QML-Q/V, ESCC, MIL-883)

Microcontroller Core Candidates (LEON2-FT)

- Advantages
  - Available from ESA in full VHDL source code
  - No more licensing restrictions with respect to ASIC technology
  - Amba internal bus ready to connect existing peripheral IP cores
  - V8uC" activity with Sitael to remove caches (separate conference paper)
  - Compiler chain available in open source (GCC)
  - Well known to the space community

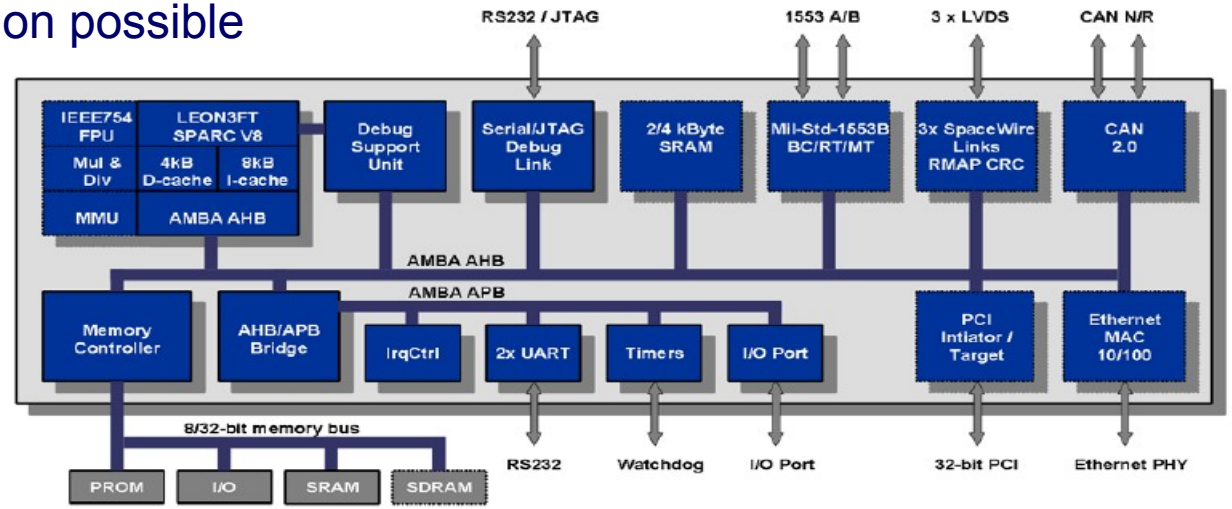




- Drawbacks
  - 32-bit architecture might be oversized for most uC applications
  - Poor code density (register windows, 32-bit addresses)
  - Debug monitor (GRMON) not a free tool

Microcontroller Core Candidates (LEON3-FT)

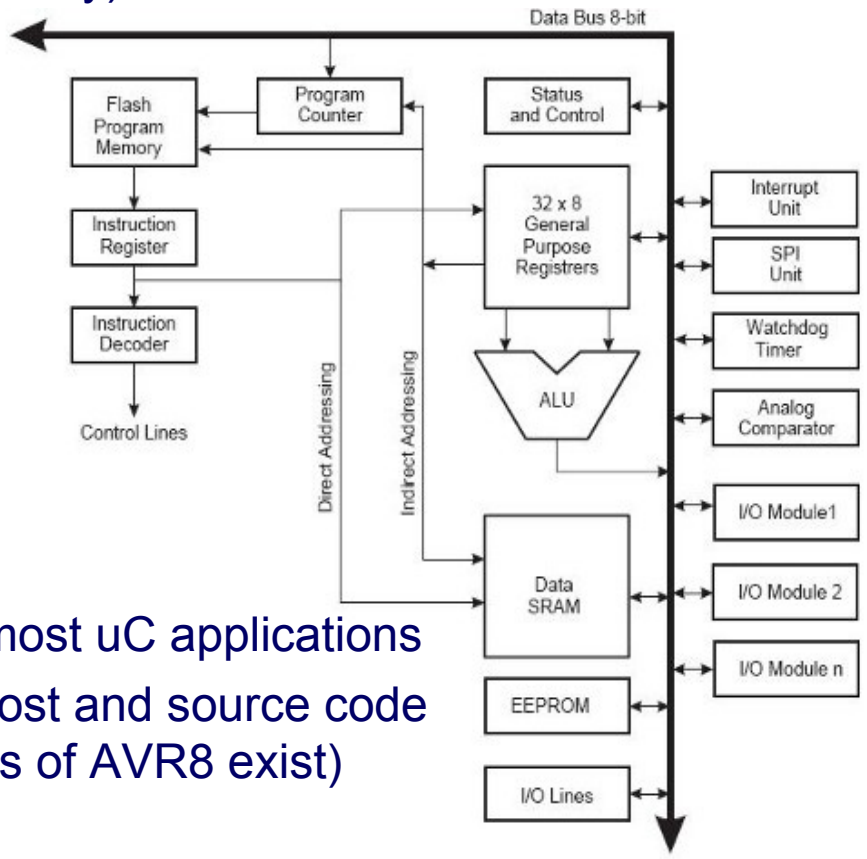
- Advantages
  - European source (Aeroflex Gaisler), excellent support
  - Amba internal bus ready to connect existing peripheral IP cores
  - Compiler chain available in open source (GCC)
  - Cache-less operation possible
  - Well known to the space community
  - Flying on RTAX FPGA devices



- Drawbacks
  - Proprietary IP core, licence conditions, cost, source code availability TBD
  - 32-bit architecture might be oversized for most uC applications
  - Poor code density (register windows, 32-bit addresses)
  - Debug monitor (GRMON) not a free tool

Microcontroller Core Candidates (AVR)

- Advantages
  - One of the leading microcontroller architectures worldwide
  - European source IP core (Atmel Norway)
  - Better code density than LEON2
  - Many tools available from different vendors or open source http://www.bdmicro.com/devtools/

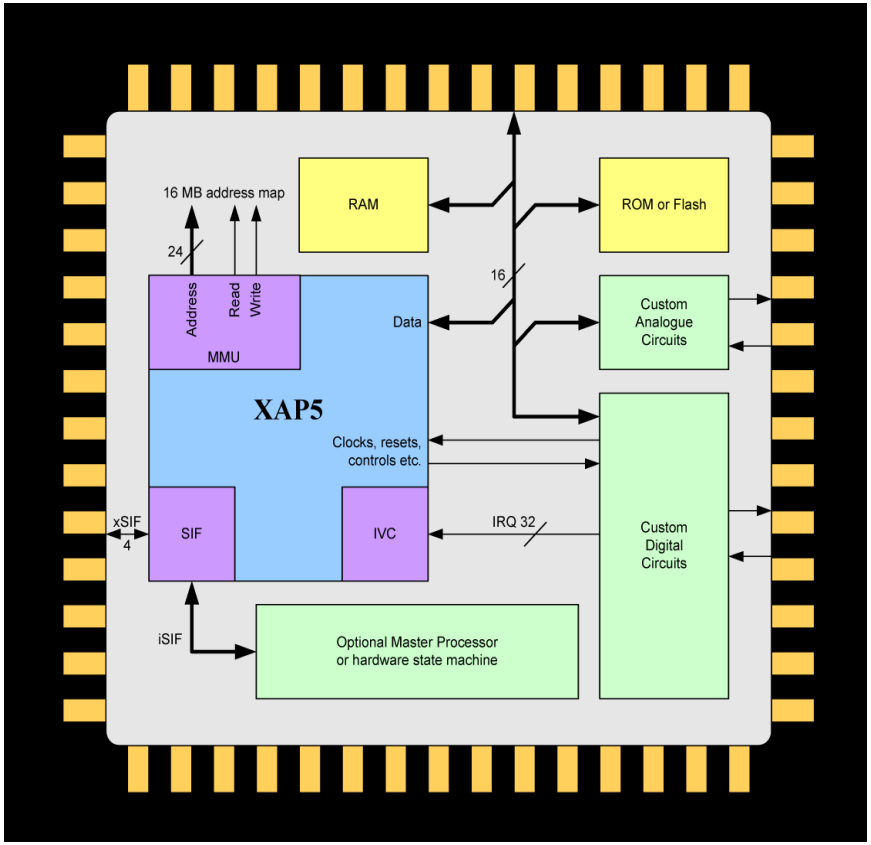


- Drawbacks
  - 8-bit AVR not sufficient
  - 32-bit AVR might be oversized for most uC applications
  - Proprietary IP, licence conditions, cost and source code availability TBD (open source clones of AVR8 exist)
  - On-chip peripheral interface TBD

Microcontroller Core Candidates (XAP)

- Advantages
  - XAP4 16-bit architecture most suitable to requirements
  - 64 kByte addressable memory fits requirements
  - European source IP core (Cambridge Consultants, UK)
  - Very good code density
  - Supplier has shown interest in space activities
  - Evaluated in an ESA study

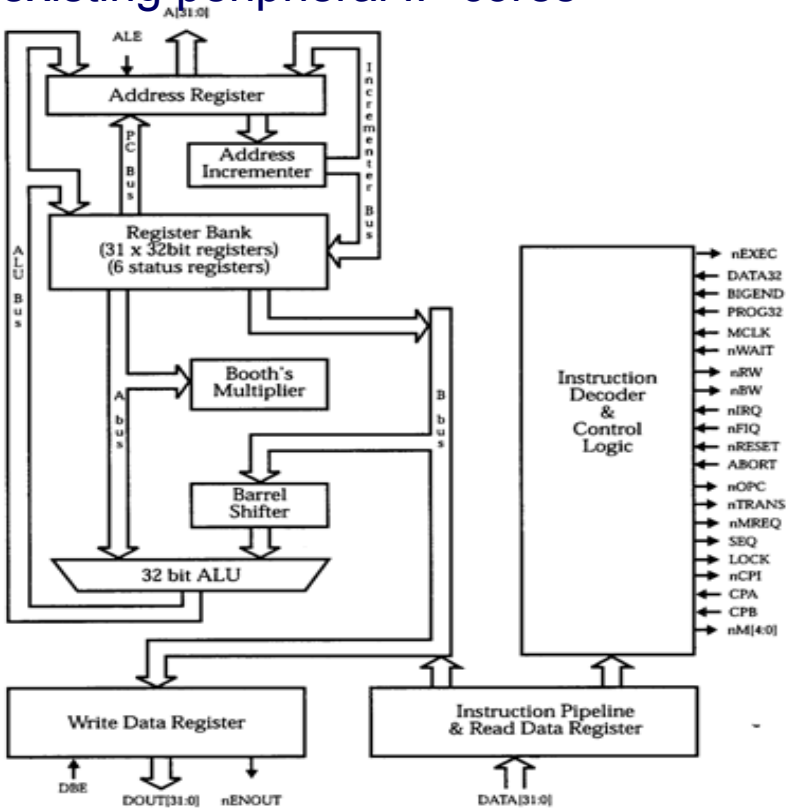
- Drawbacks
  - Closed source Verilog IP core
  - licence conditions and cost TBD
  - Proprietary SW tools
  - On-chip peripheral interface TBD



Microcontroller Core Candidates (ARM)

- Advantages
  - One of the leading embedded microcontroller architectures worldwide
  - European source IP core
  - Amba internal bus ready to connect existing peripheral IP cores
  - ARM has shown interest in radiation hardening activities
  - SW tool chains widely available, commercial and open source

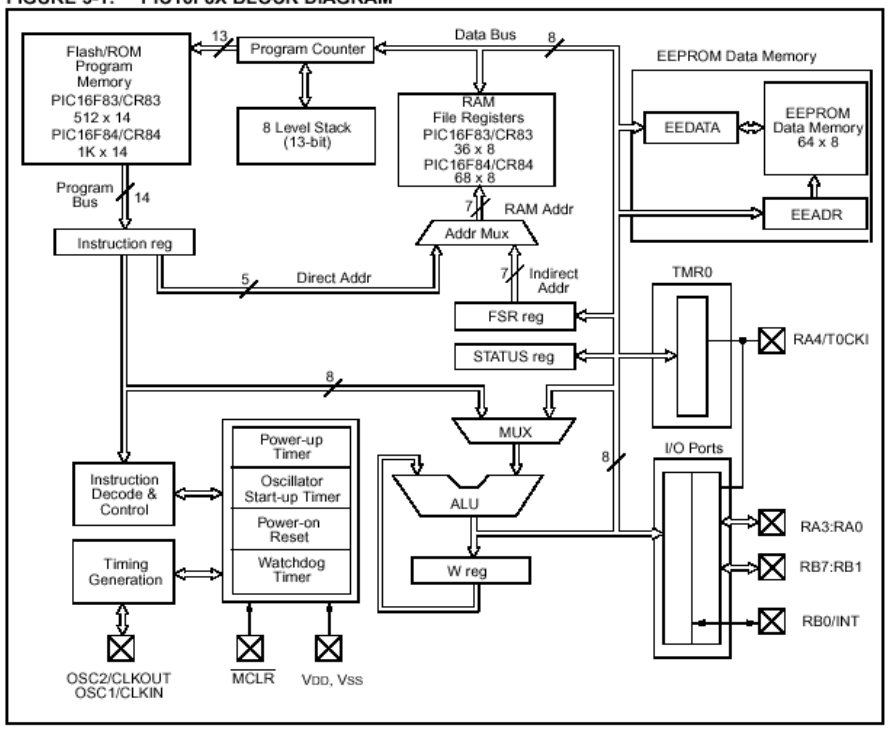
- Drawbacks
  - Code density of 32-bit ARM (Thumb is better)
  - Proprietary IP core
    Source code usually not disclosed



Microcontroller Core Candidates (PIC)

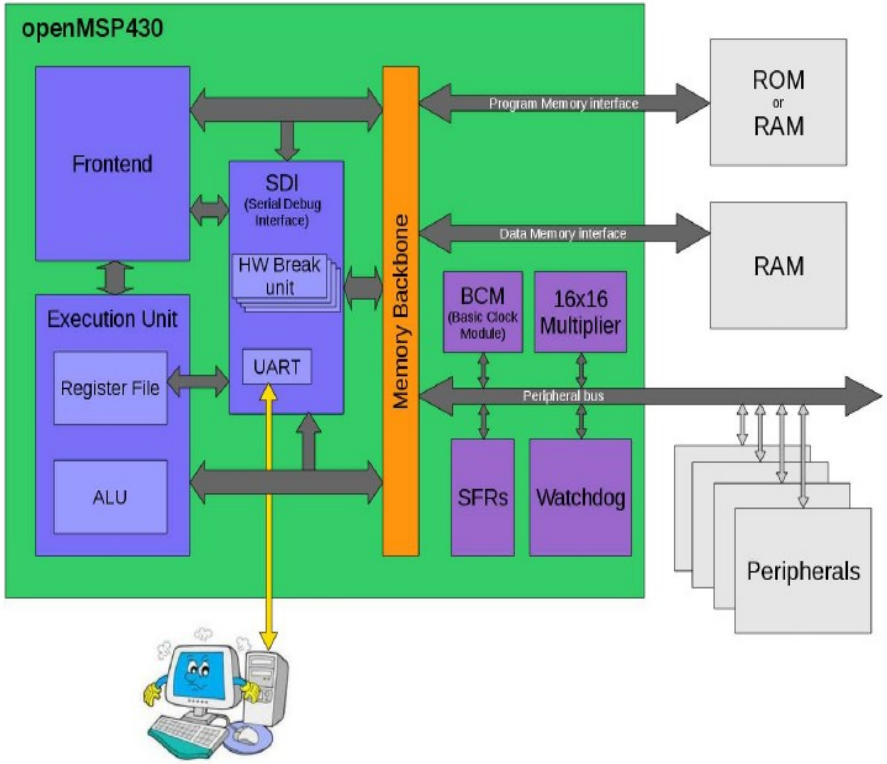
- Advantages
  - Open source IP: http://opencores.org/project,16f84
  - Popular microcontroller
  - Used by ÅAC Microtec in its Nano-RTU
  - Development tools from various sources (free, open, commercial)
  - Used by CNES (Myriade)
- Drawbacks
  - Limited performance (8-bit)
  - Open-source IP maturity is questionable
  - Legal implications of using open-source IP
  - On-chip peripheral interface TBD

FIGURE 3-1: PIC16F8X BLOCK DIAGRAM



Microcontroller Core Candidates (OpenMSP430)

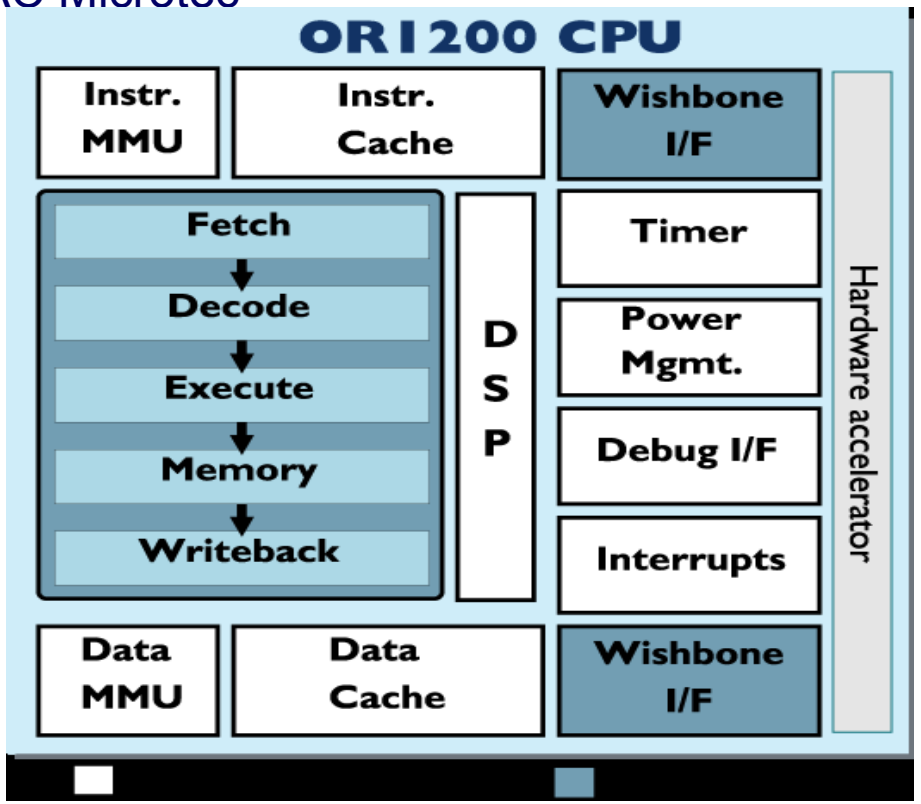
- Advantages
  - Open source Verilog IP (LGPL licence) http://opencores.org/project,openmsp430
  - Compatible with TI MSP430 (follow-up of PDP-11)
  - Many tools available from different vendors or open source
  - 16-bit processor fits requirements
  - 64 kB memory fits requirements



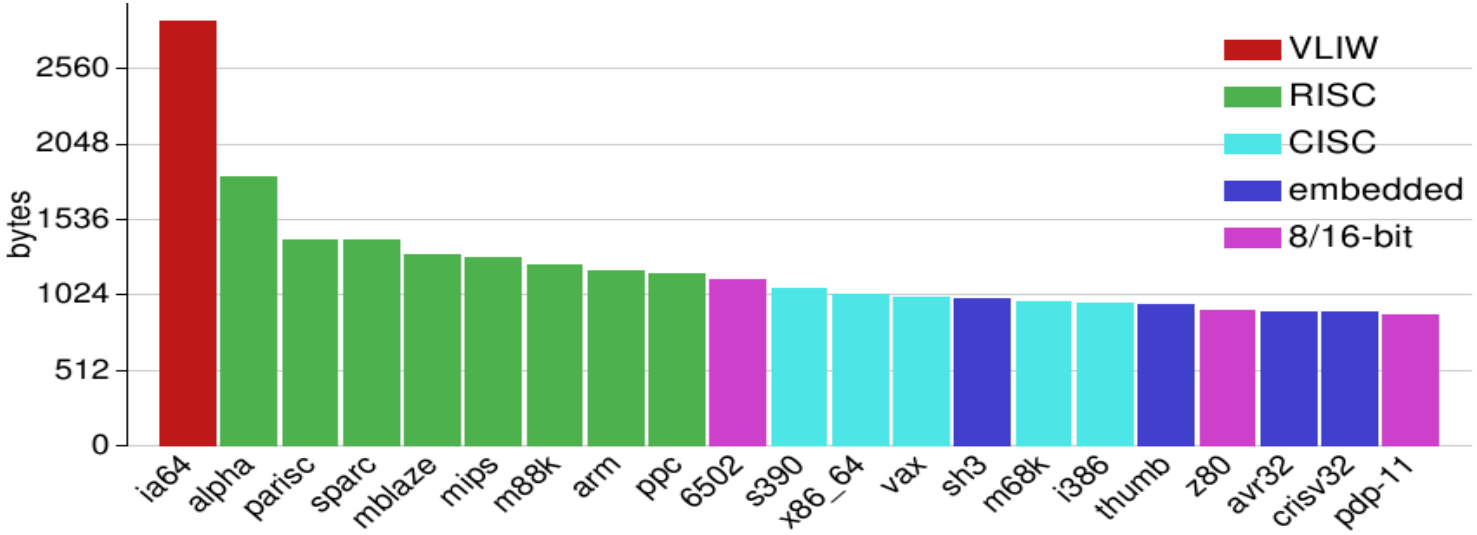
- Drawbacks
  - Maturity of open-source IP TBD
  - Legal implications of using open-source IP TBD
  - On-chip peripheral interface TBD

Microcontroller Core Candidates (OpenRISC1200)

- Advantages
  - Open source IP: http://opencores.org/openrisc,or1200
  - Fault tolerant version exists and due to fly on an US satellite http://opencores.org/newsletter,2010,09,#n5
  - Proposed in an ESA activity by ÅAC Microtec
- Drawbacks
  - Targeting higher performance: 32-bit CPU with 5-stage pipeline, caches, MMU...
  - On-chip peripheral interface TBD
  - Maturity of open-source IP TBD
  - Legal implications of using open-source IP TBD



Microcontroller Core Code Density Comparison



[V.M. Weaver, S.A. McKee, Code Density Concerns for New Architectures, ICCD09]
Code size of a given set of applications compiled for various architectures

- No extreme differences of code size, but
  - PDP-11 (= OpenMSP430?) and AVR32 have higher code density
  - SPARC, ARM are less optimal
- To be re-done with candidate CPU's and space-specific applications
- Comparison in an ESA study for power-control applications
  - Identified XAP4 and OpenMSP430 (both 16-bit) as optimal
  - LEON2 (32-bit) and 8032 (8-bit) have much higher code size

Microcontroller Core Candidates (Summary)

- Some candidates are more likely to be discarded
  - ARM (cost of source code access, hardening to be done)
  - PIC, AVR8 (lack of performance)
  - OpenRISC (overdimensioned, questionable maturity)
  - LEON3-FT (code density, cost of source code access TBD)
  - LEON2-FT (code density, no cache-less operation possible)
- Remaining candidates need additional clarification / assessment
  - AVR32, XAP4: Licensing conditions, source code availability and cost
  - LEON2-V8uC: Maturity of the IP core, code density remains a problem
  - OpenMSP430: IPR associated to the architecture
- Additional investigation required on all candidates
  - Performance versus power consumption
  - Code density, gate count
  - Integration with peripheral IP cores
  - SW tool chains (availability, quality, cost)
  - Non-technical (licensing, cost, support)

Semiconductor Technologies for Microcontrollers (1)

- Requirements
  - Mixed signal capability
  - Integration of a large amount of RAM
  - SEU hardened standard cell library
  - Non-volatile memory (NVM) desirable
  - High-voltage (5 – 15V) IO's desirable
  - Space qualification (process capability or wafer lot qualification)
- DARE-UMC 180 nm
  - Mixed signal capability available
  - Area and power consuming library, limitiations in memory compiler
  - 90 nm could bring improvement, but funding currently on-hold
- Atmel 180 nm
  - No analog design kits currently available
  - Opening to mixed signal announced (P. Sauvage, ESCCON 2011 https://escies.org/GetFile?rsrcid=49199)

Semiconductor Technologies for Microcontrollers (2)

- LFoundry 150 nm
  - Mixed signal, 5V IO and NVM available
  - ESCC Space process capability study with DLR and Tesat http://www.dlr.de/qp/en/desktopdefault.aspx/tabid-3091/4699_read-6881/
  - Radiation hardened standard cell library currently not available
  - Switch to 150 nm announced by Atmel
- Ramon Chips (Tower 180 nm)
  - SEU hardened library available for 180 nm, 130 nm in preparation
  - Mixed signal capability
  - Device qualification possible (MIL-STD-883)
  - Cooperation agreement between ESA and Israel
  - Embedded NVM TBD
  - Export licence and commercial availability to be clarified
- XFAB 180 nm
  - Mixed signal, 5V IO and NVM available
  - Radiation hardened standard cell library currently not available
  - No space experience so far, but radiation evaluation and the development of a rad-hard library proposed in an ESA activity ==> this is considered as a long term activity

Microcontroller Development Activities at ESA

- V8UC development with Sitael – ongoing, to be closed by the end of 2011
  - Cache-less version of LEON2FT – separate presentation at this conference
- Microcontroller-2015 (ref. # T701-317ED, TRP workplan 2011 - 2013)
  - Open competition, to be released after further internal investigation
- Process Portable Mixed-Signal Micro-controller peripherals
  - Network Partnering Initiative (NPI) with University of Seville (proposed, TBC)
- Qualification of Microcontroller planned under ECI3/4 (not yet approved)
- Radiation hardened Digital Power Controller (ETCA)
  - Artes 5.2 with ETCA, feasibility study done, follow-up to be decided
    http://microelectronics.esa.int/conferences/mesa2010/08_S2_1200_ETCA_Marc_Fossion.pdf
- HBRISC3 – Hardened Bi-RISC processor (SABCA)
  - Cacheless, fully deterministic, linear program flow, dual FPU
  - Dedicated to hard real-time motor control
  - HBRISC2 developed in early 2000's, used in Vega
  - HBRISC3 developed for the Ariane 5 ME thrust vector control (TVC) unit
  - Standard component “Control Loop Processor” -- currently no funding
    http://microelectronics.esa.int/conferences/mesa2010/05_S2_1100_SABCA_Marco_Ruiz.pdf
- Motion Control Chip (Aeroflex Gaisler, ÅAC Microtec, CSEM)
  - TRP activity – separate presentation at this conference

Microcontroller – Conclusion (1)

- WHICH Processor IP?

- WHICH Semiconductor technology?

Additional investigation at ESA required

Microcontroller – Conclusion (2)

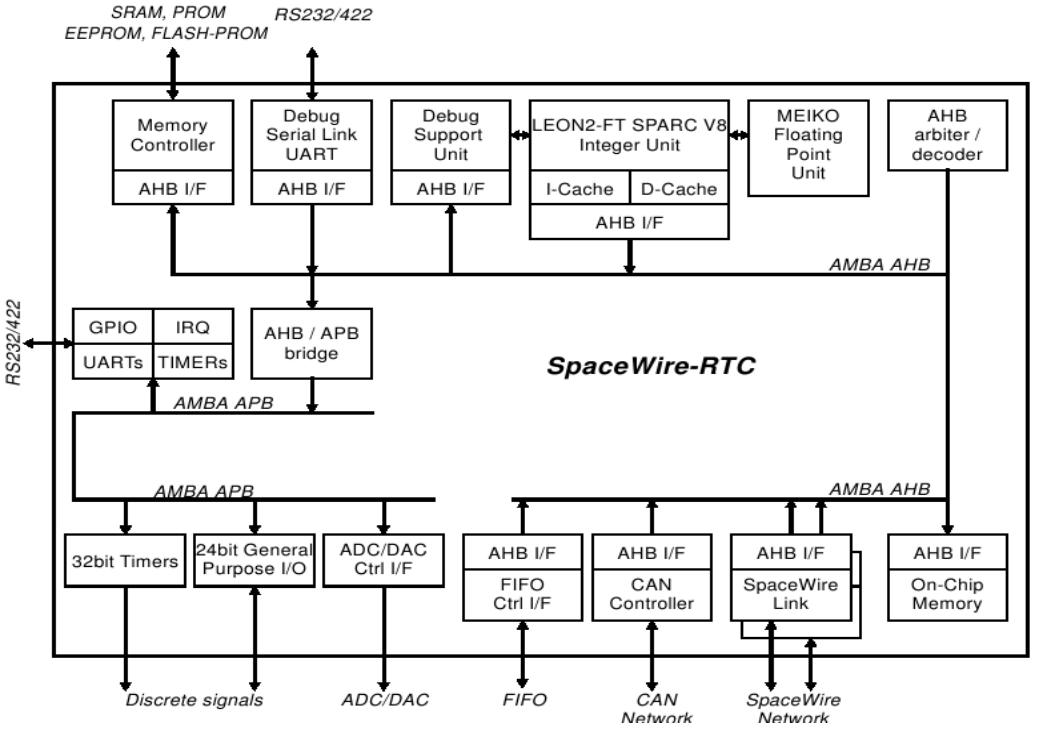
possible answers...

- WHICH Processor IP?
  - Preferably ESA or open source IP or (LEON2FT, V8UC, OpenMSP)
  - Commercial IP (AVR, LEON3FT, XAP4), provided that source code is delivered and an agreement is reached on conditions and cost (access, maintenance, technical support)

- WHICH Semiconductor technology?
  - Ramon Chips 180 attractive solution
    - commercial availability to be clarified
  - DARE 180 as a back-up
  - Atmel and XFAB possible long term solutions
    - pending qualification and development of rad-hard library

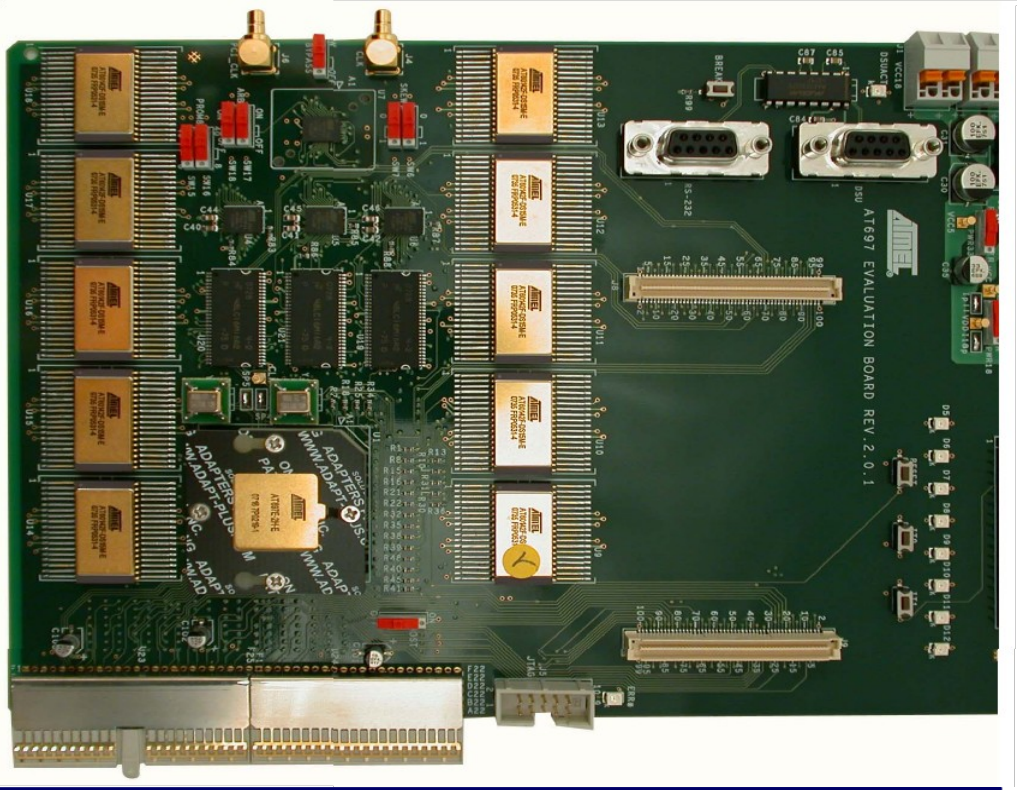
LEON2FT based Microprocessors - AT7913E

- "Spacewire Remote Terminal Controller"
  - Established on Atmel catalog, brief data sheet and SMD available
    http://www.atmel.com/dyn/products/product_card.asp?part_id=4595
  - Full user manual not yet available from Atmel, but provided at ESA site:
    http://microelectronics.esa.int/components/AT7913E_UserManual-2-4.pdf
  - Californium SEU testing performed at ESA
    Heavy Ion test campaign planned with Atmel
  - First missions:
    BepiColombo, SolarOrbiter



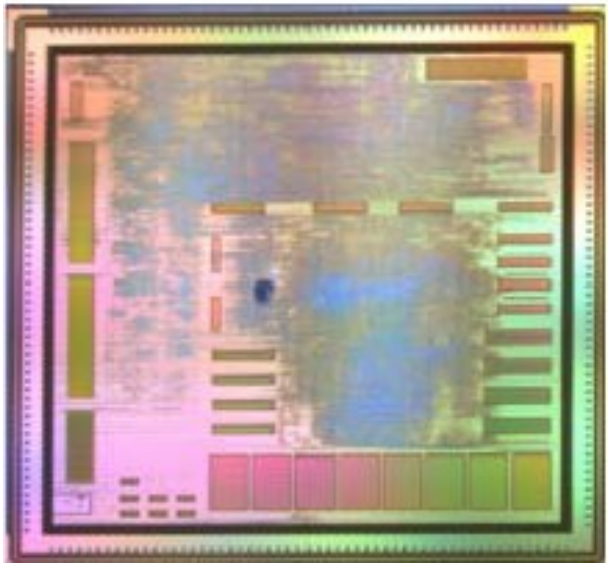
LEON2FT based Microprocessors - AT697

- Standard microprocessor based on LEON2FT with PCI 2.2 interface
  - Established on Atmel catalog:
    AT697E: http://www.atmel.com/dyn/products/product_card.asp?part_id=3178
    AT697F: http://www.atmel.com/dyn/products/product_card.asp?part_id=4599
  - Electrical Characterisation and SEU testing completed
  - Preliminary “Advance Information” data sheets available
  - Final release data sheets at internal review (ESA/Atmel) to be published soon
  - Evaluation boards available
  - ESCC evaluation/qualification: to be completed this summer
  - Selected by numerous projects
    Orders booked since 2009:
    626 EM (TSC695 ~ 1300)
    376 FM (TSC695 ~ 2900)
  - Backlog decreasing
  - Packages LGA349, MQFP256
    MCGA not available any more

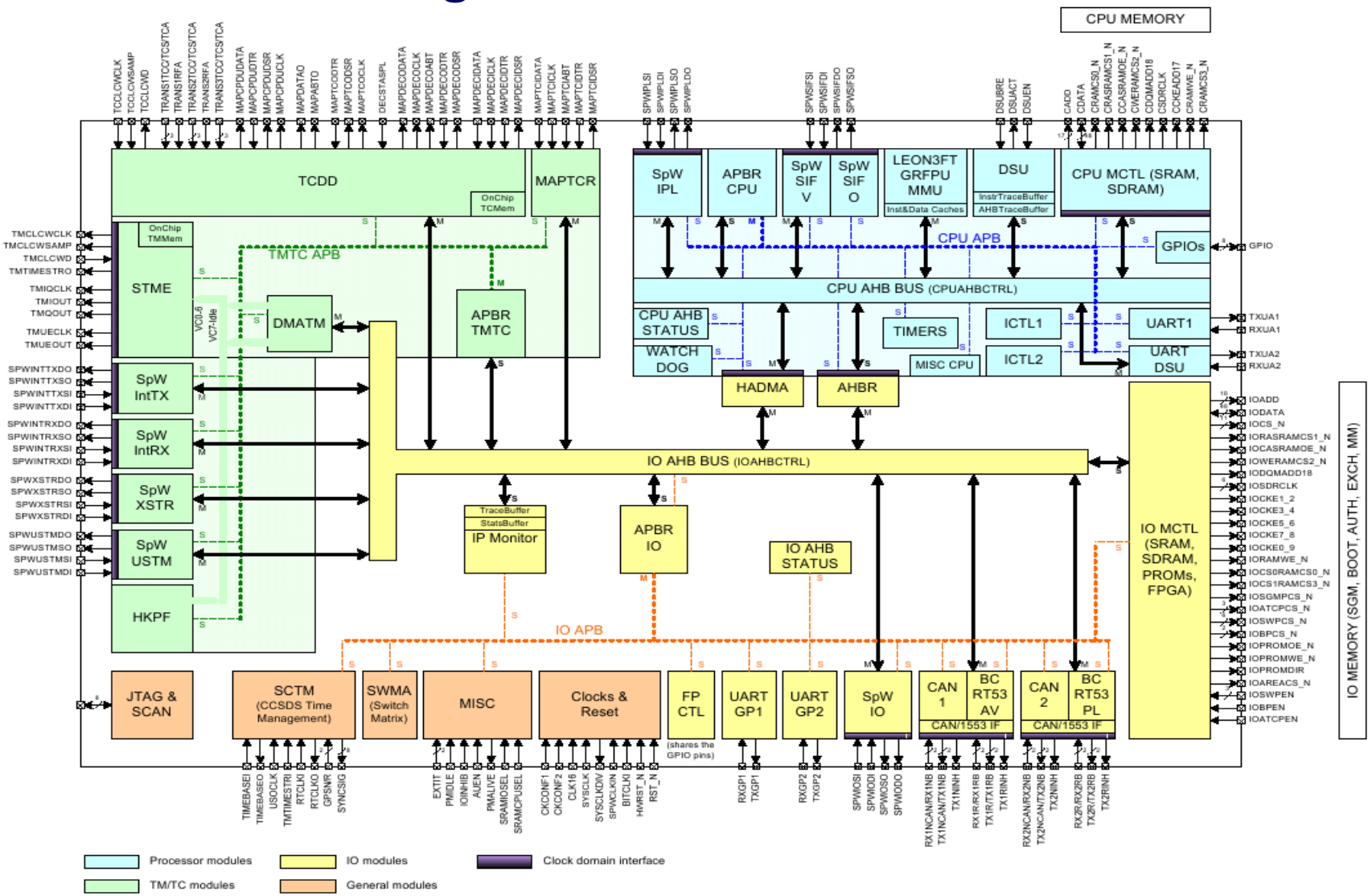


LEON3FT based Microprocessors - SCOC3

- Spacecraft Controller On-a Chip
  http://www.astrium.eads.net/node.php?articleid=5360
  - Electrical Characterisation completed
  - Initial SW development by Astrium progressing
  - SEU testing to be performed
  - First missions: SEOSAT and ASTROTERRA (SPOT 6/7)
  - Follow-up activities (ITTs to be released soon)
    - On-board computer for planetary landers (MREP)
    - SCOC3 SW support (BSP/drivers under Edisoft RTEMS 4.8.0 and ECSS software standards (TRP)
  - Comprehensive data-sheet/user manual available
  - To be established as standard component, commercialisation commitment from Astrium, but no EM parts are available from Atmel
  - FPGA-based Evaluation board (STARKIT) developed under CNES contract (separate paper at this conference)
  - Package: LGA472 with 6-sigma columns (currently assembled in the US, to be transferred to Europe)



SCOC3 block diagram



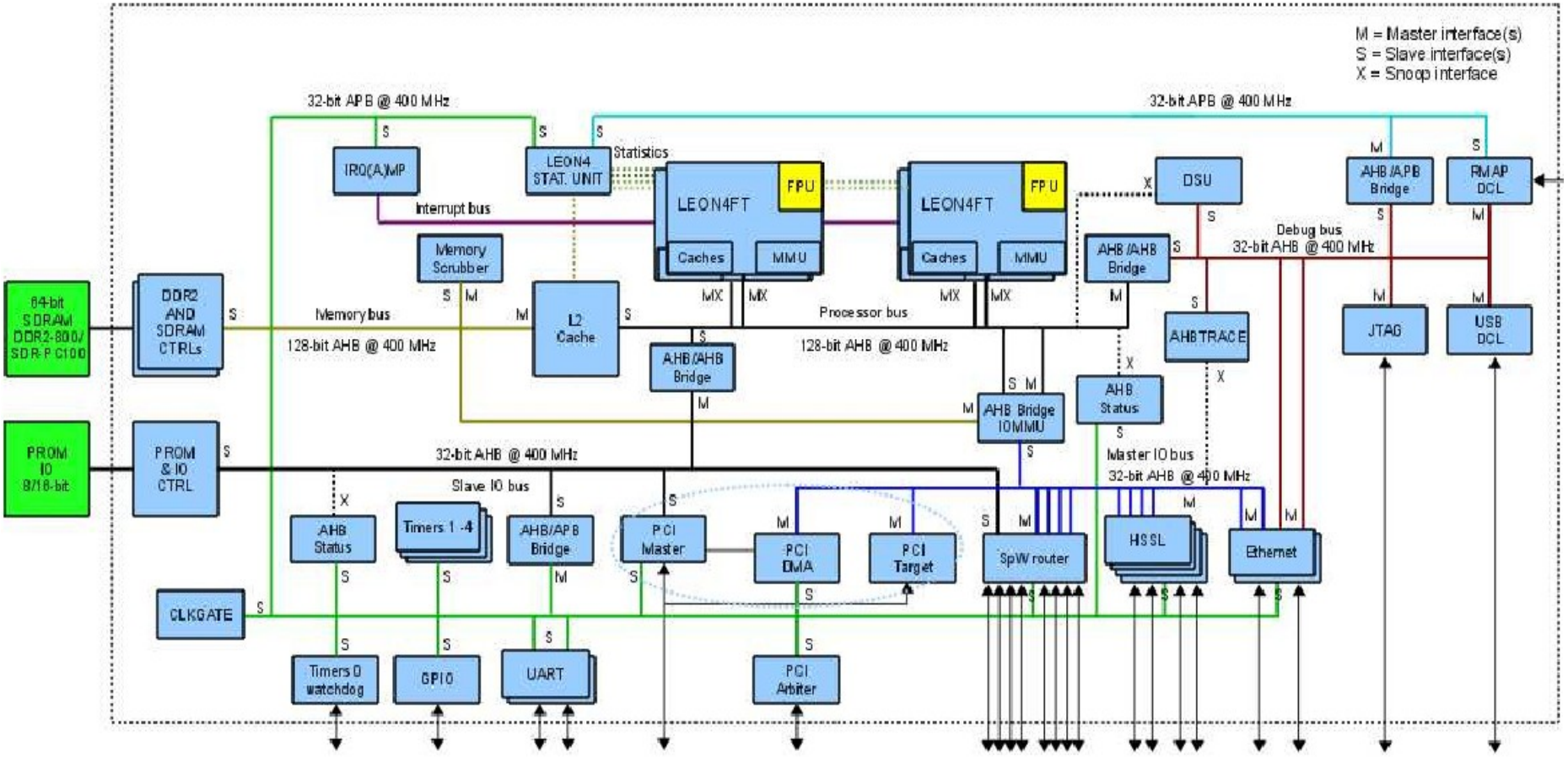
Next Generation Microprocessor (history)

- Preliminary study with the GINA project based on LEON3-SMP [DASIA 2006]
  - ALR Pouponnot: “A Giga INstruction Architecture (GINA)” ftp://ftp.estec.esa.nl/pub/wm/wme/Web/Gina2006.pdf
- Microprocessor roundtables 09/2006 and 11/2009
  - http://conferences.esa.int/01C25/Microprocessors (access: cpulink/cpu4space)
  - http://microelectronics.esa.int/cgi-bin/mpsa.cgi
- NGMP development under TRP contract kicked off in June 2009
  - PDR (verified VHDL-RTL) achieved in December 2010
  - Preliminary Datasheet and Verification Report available http://microelectronics.esa.int/ngmp/ngmp.htm
  - FPGA prototypes on various boards available to the user community
  - Activity includes development of SW environment (BSP, compiler, GRMON)
  - Design is ready for synthesis in target technology
  - Currently on hold because ST 65 nm space libraries not available

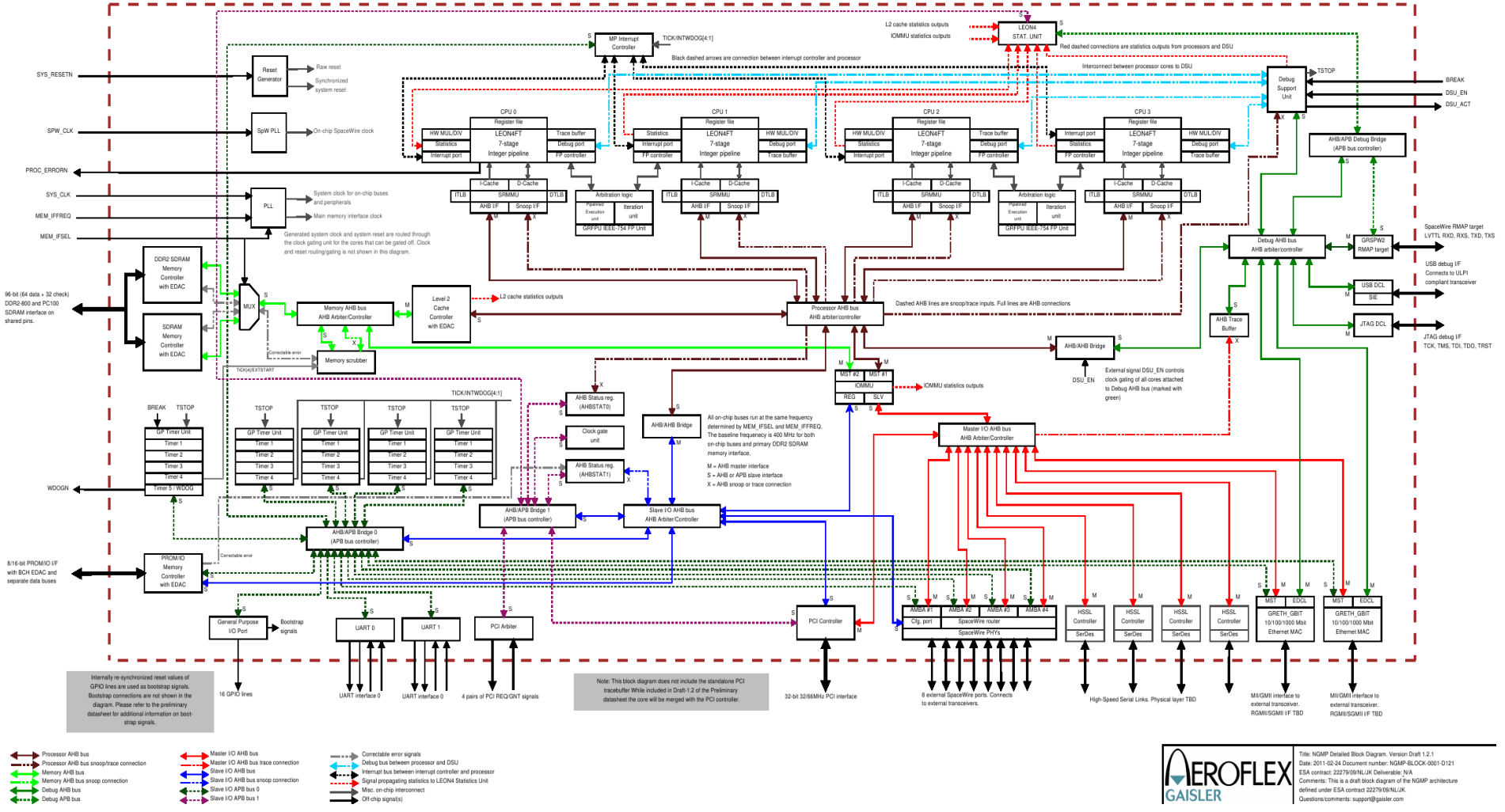
Next Generation Microprocessor (features)

- Key features of the NGMP architecture
  - Upgrade from LEON3 to LEON4
    - L2 cache, 128-bit AHB processor bus, Branch prediction
  - 4 CPU cores with two shared FPUs (baseline)
  - Multiple AHB bus structure to decouple IO and debug transfer
  - Full MMU protection for processor and DMA IO peripherals
  - Timer and interrupt infrastructure supporting AMP configurations
  - Enhanced debug features
    - DSU, trace buffers on PCI/AHB, performance counters
  - Debug link via Ethernet, JTAG, USB or RMAP
  - 64-bit DDR2 / SDRAM / PROM memory interface with background scrubbing unit
  - High-Speed-Serial link interfaces (based on ST HSSL, details TBD)
  - Spacewire router with 8 external Spacewire ports and 4 internal AHB DMA ports
  - PCI 2.3 32-bit 66 MHz link
  - 2 Ethernet links
  - UARTs
  - GPIOs

Next Generation Microprocessor (block diagram)



Next Generation Microprocessor (detailed block diagram)



Next Generation Microprocessor (roadmap)

- Manufacture and test of prototypes in (non rad-hard) commercial technology
  - TRP contract kicked off in April 2011, planned duration is 1 year
  - Target technology eASIC Nextreme-2 (45 nm structured ASIC)
  - Implementation at target speed (goal 400 MHz)
  - Evaluation boards will be available to the user community
- Next phase: Proto-FM in target technology
  - Budget approved in TRP work-plan 2011 – 2013 (T701-302ED)
  - Includes radiation and functional validation
  - On-hold: ST 65 nm space library not yet available
- Final phase: FM in target technology
  - Manufacturing of flight models with bugfixes and user feedback
  - Currently no funding (ECI...?)
- Related SW activities (TRP 2011 - 2013)
  - System Impact of Distributed Multicore Systems (Hypervisor), ongoing
  - Development Environment for Future Leon Multi-core (T702-302SW)
  - Emulators of future NGMP multicore processors (T702-304SW)
  - Schedulability analysis techniques/tools for cached/multicore processors (T702-308SW)

Conclusion / Outlook

- ERC32 is a successful processor – and a mature product
- AT697 is almost ready, and already becoming a success story
  - Atmel has full order books
  - Logistic bottleneck improving, but yet to be fully recovered
  - Documentation and support to be worked on
- SCOC3 in overall a successful development
  - Commercialisation as standard ASIC to be consolidated
  - Radiation testing to be performed
  - Europeanisation of the 6-sigma columns
- NGMP is progressing very well (on schedule)
  - Key challenge is availability of the ST 65 nm space ASIC technology
  - Backup (e.g. DARE 90 or Ramon 130) uncertain (funding!), possible performance degradation
- Microcontroller: 8032 is obsolete, a new microcontroller is key challenge for the coming years
  - Mixed signal ASIC technology ??? - Mixed signal peripheral development
  - Selection of processor IP (technical and non-technical criteria)
  - ESA internal consolidation of main baselines before ITT
- Development of companion chips should be undertaken, for example:
  - Spacecraft Management Unit (SMU) Core ASIC as companion chip to NGMP or AT697
    - GSTP activity in preparation with RUAG Sweden