# Advanced GPS Galileo ASIC (AGGA-4) - Enabling Next Generation of Navigation Receivers

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# Introduction

Currently Astrium GmbH together with ESA/ESTEC is involved in the development of the AGGA-4 (Advanced GPS/GALILEO ASIC) which is a GNSS baseband ASIC capable of processing modernized GPS and Galileo Signals.

The ASIC is manufactured in the radiation hardened 180 nm process ATC18RHA from Atmel. The chip has been signed off in November 2011, the prototypes are planned to be delivered in Q2 2012 and the first flight components are planned in Q4 2012.

This abstract gives an overview of the AGGA4 architecture, the technical considerations performed during the architecture definition and the lessons learnt during the ASIC backend design.

# The AGGA-4 Chip Architecture

The AGGA-4 due to its flexibility is not only able to process modernized GPS and Galileo signals but also other GNSS systems like Glonass, Compass, etc. In addition, the ASIC also incorporates a processor, space-specific communication interfaces and other support functions (e.g. FFT, CRC) that simplify the GNSS receiver board design, while at the same time enhances the capabilities.
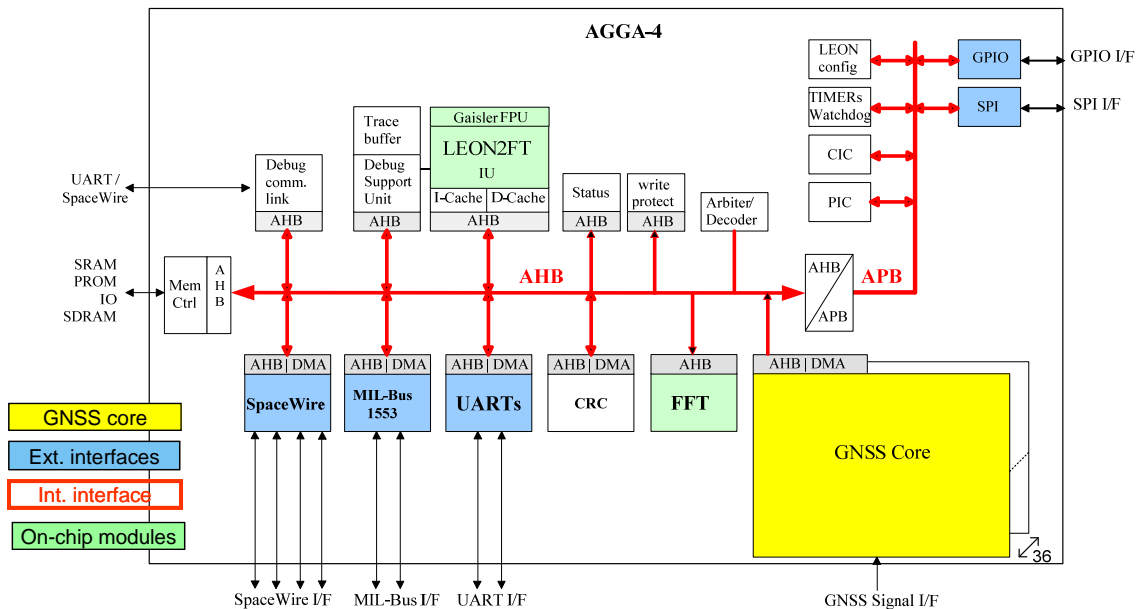


Figure 1: Overview of AGGA-4 architecture.

As shown in Figure 1, the AGGA-4 includes the LEON-2 Fault Tolerant processor together with the Gaisler Research Floating Point Unit (GRFPU), on-chip AMBA APB and AHB busses. The GNSS baseband processor and the on-board interfaces (UART, SpaceWire, MIL-1553) have direct memory access (DMA) capability to exchange data with the external SRAM memory. A hard-coded 128 point 32-bit fixed-point FFT unit allows frequency estimation during acquisition.

The following external interfaces are available in the ASIC:
- Four DMA capable SpaceWire interfaces with a maximum data rate of 90 Mbps per link.
- DMA capable Mil-Std-1553 interface
- Two DMA capable UARTs
- SPI (both master and slave capability) for configuring and monitoring the RF front-ends
- 32 bit GPIO (General Purpose Input Output)

The main capabilities of the GNSS core in the AGGA-4 are as follows:
- Interfacing with up to 4 RF Front-ends
- Digital Beam-forming unit
- 36 single frequency double code GNSS channels with aiding functionality (code and carrier aiding for autonomous NCO update)
- Flexible primary code generators (LFSR and memory based)
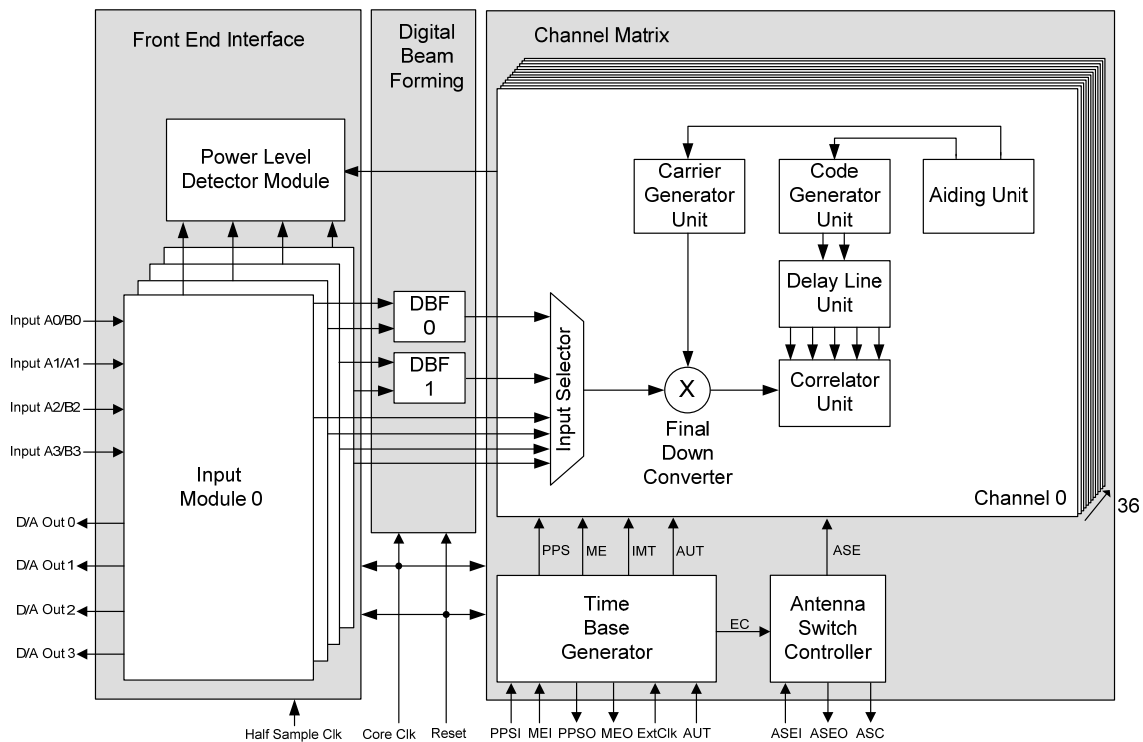- Support of Binary Offset Carrier and secondary codes



**Figure 2: AGGA-4 GNSS Core.**

## ASIC Design Considerations

A big challenge for the AGGA4 design was to confine the whole functionality within the area constraints of the ASIC technology, allowing for a maximum of about 6 million gates (including memories and pad cells).

Various implementation options were traded off during the design phase, to stay within the available gate limit. The following paragraphs discuss the major considerations performed during the ASIC development.

The use of 100% SEU hardened flip-flops, as initially planned, resulted in an excessive area and power consumption of the chip. Therefore, the functionality of all the registers in the design was analysed with respect to bit-error tolerance. As a result about 20 % of the total flip-flops in the design are non-hardened ones. These are present mainly in the data path where bit-errors can be tolerated.

The architecture of the GNSS base-band channels was optimised in order to reduce the number of gates per channel. One embedded SRAM core of 1280x8 bits was added to each channel to store the primary spreading code of Galileo signals. This memory can also store most of the GPS spreading codes. This allowed simplification of the complex LFSR implementation, AGGA4 requires only a 2x14 bit LFSR per channel to generate the very long GPS L2CL code. Furthermore, the semi-codeless tracking capability for GPS military signals, formerly implemented in AGGA2, was not retained for AGGA4.

The ASIC also includes clock gating capabilities allowing complete deactivation of an unused channel and thereby reducing the power consumption.

Due the large size of this design, achieving a high operating frequency was very challenging. As most of the critical paths were found in the LEON2 processor, its configuration was slightly adapted compared to the reference configuration used in the Atmel AT697 chip. The register file (RF), instead of using duplicated two-port SRAM cores and EDAC, was implemented with SEU-hardened flip-flops, saving the RF-EDAC and avoiding a falling-edge triggered path. In the multi-set cache controller, the replacement strategy was changed from Least-Recently-Used (LRU) to Random, avoiding the storage of and comparison with the allocation history. Nevertheless, routing congestion was observed, the timing remained challenging, sometimes degraded by hold-fix, voltage drop and cross-talk issues. Backend design steps (like placement optimisation, routing by hand, etc.) had to be repeated iteratively until the timing closure was achieved.

Early during the design phase, it was decided to perform FPGA based verification for the design. This helped in identifying functional problems. The ASIC design itself was checked for formal equivalence and also simulations with the final netlist were performed. Moreover, the different verification flows were performed by three different teams.