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80S32 Validation Board Specification

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1 INTRODUCTION

1.1 Background

"An 8-bit microcontroller for space usage has been developed under ESA contract, and prototypes have been delivered in 2002. The component is manufactured in a space qualified technology, however, in order to release it as a standard component, a functional and performance validation has to be done. "

1.2 Purpose and scope

The purpose of this document is to present the specification for the board to be used for functional and performance validation of the 80S32 microcontroller. This board may also be used as a prototyping board, which will aid users designing and working with 80S32 microcontroller.

1.3 Reference documents

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1.4 Acronyms and abbreviations

Clk	Clock
DC	Direct Current
DIP	Dual In-line Package
FPGA	Field Programmable Gate Array
I/O	Input/Output
MHz	Megahertz. 10^6 hertz
MQFP	Metric Quad Flat Pack
NC	Not Connected/No Connection
NV SRAM	Non-Volatile Static Random Access Memory
PCB	Printed Circuit Board
PIO	Parallel Input Output
QFP	Quad Flat Pack
ROM	Read Only Memory
RS-232	One standard (protocol) for serial transmission
RxD	Received data
SMD	Surface Mounted Device
SRAM	Static Random Access Memory
TC	Telecommand
TM	Telemetry
TxD	Transmitted data
µC	Microcontroller
USART	Universal Synchronous Asynchronous Receiver Transmitter
V_{CC}	Voltage at the Common Collector. Positive operating voltage, connected to positive power supply.
VCCA	Vcc connection of the microcontroller's core voltage supply
VCCB	Vcc connection of the microcontroller's I/O voltage supply
V_{CCINT}	Power supply for the internal core logic of the FPGA
V_{CCO}	Power supply for the output drivers of the FPGA
VME	Verso Modulo Europa. Scalable backplane bus interface. Original specification IEEE 1014-1987.
V_{SS}	Voltage for Substrate and Sources. Negative operating voltage, connected to negative power supply or to
VSSA	Ground connection of the microcontroller's core supply
VSSB	Ground connection of the microcontroller's I/O supply

1.5 Naming convention

Active low signals are presented with '/' before the signal name, for example /CE is active low chip enable signal.

2 ARCHITECTURE DESCRIPTION

The board consists of the microcontroller itself, on-board memories and the user interface. In addition, the board offers possibility to install Xilinx Virtex Series FPGA, which can be used as a help for validating the microcontroller. Therefore microcontroller can either independently run a program by accessing the on-board memories and/or the FPGA can be used for connecting additional logic to the microcontroller. It's user's choice whether or not the on-board memories are disabled during the use of a FPGA. The physical implementation of the board is to be made in such way that the microcontroller can be run independently with or without the FPGA.

The on-board program memory for the microcontroller is in-system programmable via the RS-232 connection.
Also the FPGA can be configured while installed in-system. Configuration will happen via the MultiLINX cable using the Boundary Scan connections of the FPGA. There is a ribbon cable connector for the MultiLINX cable on board.

Most of the selections, such as disabling on-board memories etc., are made with different kind of switches.

2.1 Block Diagram

The simplified block diagram is in figure 2.1. More detailed block diagram is presented in ANNEX A. There are four main blocks in the evaluation board: *80S32 Microcontroller, On-Board memory, FPGA-Module* and *User Interface*.

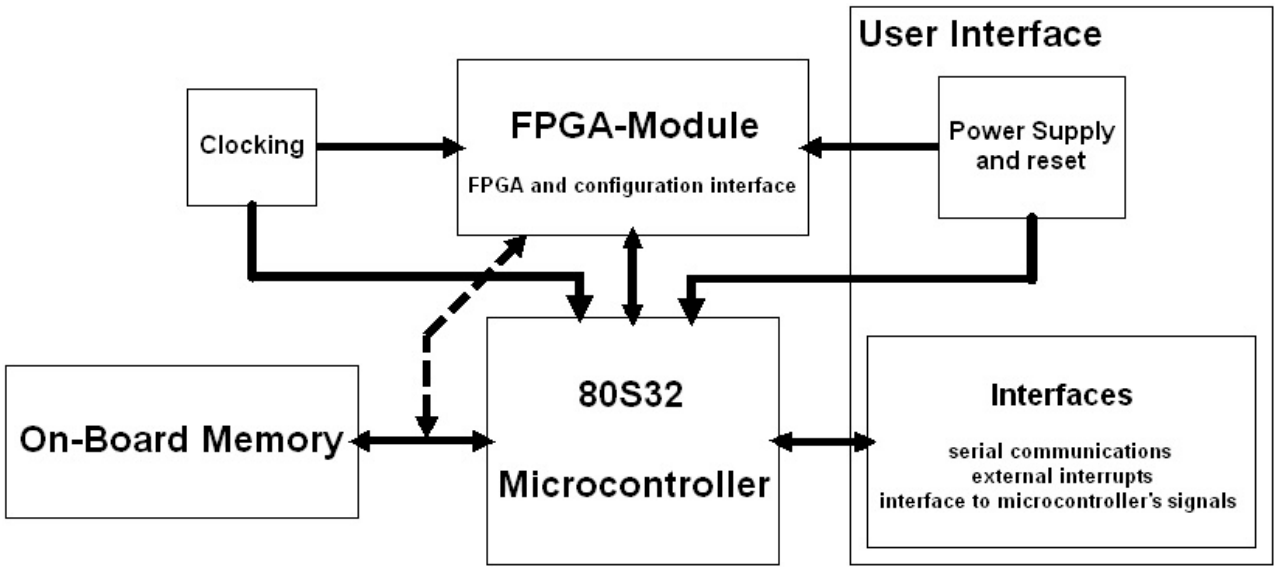


Figure 2.1 Evaluation board block diagram

2.2 Microcontroller

The microcontroller itself is Intel 8051-based microcontroller, type 80S32. The package of the microcontroller is 100-lead MQFP Flat, as shown in ANNEX C.
Also a socket for the microcontroller is provided, in order to easily replace the tested device.
In addition to microcontroller and it's socket, there are also following features available on the board:

- In every data and address line there is 0Ω SMD-resistor allowing post-placement of serial component. These should be placed between μC and the 26-pin interface connectors.
- One (1) clock divider circuit (model: ICS542).
- One (1) clock oscillator for clock divider's input clock ICLK.
- One (1) 5V MicroMonitor (model: DS1814C-5) for supervisory of the microcontroller's operating voltage and resetting the microcontroller.

All Input/Output buffers of the microcontroller are implemented with internal pull-up resistor except the 4 pins that can be used as SXVAL signal. Those 4 pins are pins 61, 47, 70 and 64 for extra USART1, 2, 3 and 4 respectively. The reason is that the inactive level of this signal is different in PacketWire mode (low inactive) than in TTC-B-01 mode (high inactive). When needed, these pins shall be externally pull high or low.[1][6]

Summary of the microcontroller as well as package and electrical characteristics can be found in ANNEX C.

2.2.1 CLOCKS

80S32 is specified for the maximum clock frequency of 20MHz[6], but analysis has been made with 25MHz frequency [1]. The power consumption estimation made in [1] has been made at 10MHz. Evaluation board offers an opportunity to use the microcontroller with various frequencies up to 22.1184MHz on-board, or user-defined frequency with external clock input. First the idea was to provide few MHz above and below the specified frequency. Nevertheless, because of the serial communications, the frequency is selected to be what is. The different clock frequencies gained from 22.1184MHz with the clock divider enable the use of standard bit rates for serial communication. There is a 4-pin DIP-14 -size socket for the clock oscillator, so it is easy to change the oscillator component, if needed. In previous 'Demonstrator Breadboard' [2] clock frequency of 1.8432MHz was used. Also the bit rate of 9600bps was used in serial communications. In order to have backward compatibility, the clock frequency was chosen to be 22.1184MHz. Refer to chapter 2.1.1.6 for information about serial communications of the evaluation board.

In addition to clock oscillator there is also a clock divider circuit (ICS542) implemented on the board. These together are used to provide different frequencies to the microcontroller's clock input.

There is also connector for external clock source. In addition to these, there are six DIP-switches, which are used to select between different clocking choices.
One of the switches is used for enable or disable the divider. When the divider is disabled it's output pins (CLK1, CLK2) are tri-stated. One of the switches is used for bypass the divider. In this way the frequency of the on-board clock is fed straight to the clock input of the microcontroller. One of the switches is used for select between external or on-board clock source. Therefore there is also a possibility to provide clock input for the FPGA from the clock divider, while using external clock source for the microcontroller. Three remaining switches are used for selecting the clock divider's output frequency. Since there are two outputs on the divider circuit, one of these switches is used to select one between the outputs. Two of the switches are used to select the actual output frequencies. With these two switches it is also possible to shut down the entire clock divider circuit.

On-board clock frequency can also be connected to FPGA's global clock inputs (GCK[3:0]). Clock buffer (ICS553) is provided in order to drive all four GCKs and microcontroller's clock input. It should be noted, that all four outputs of the clock buffer should have identical loads [13]. Since there will be some differs in loading, skew between the outputs will increase. Nevertheless, there are Delay-Locked Loops associated with each clock input buffers on the FPGA. These can help eliminating the skew [12] in clock's of the FPGA.

Figure 2.2 is to clarify the clocking scheme and table 2.1 gives the switch settings for different frequencies.

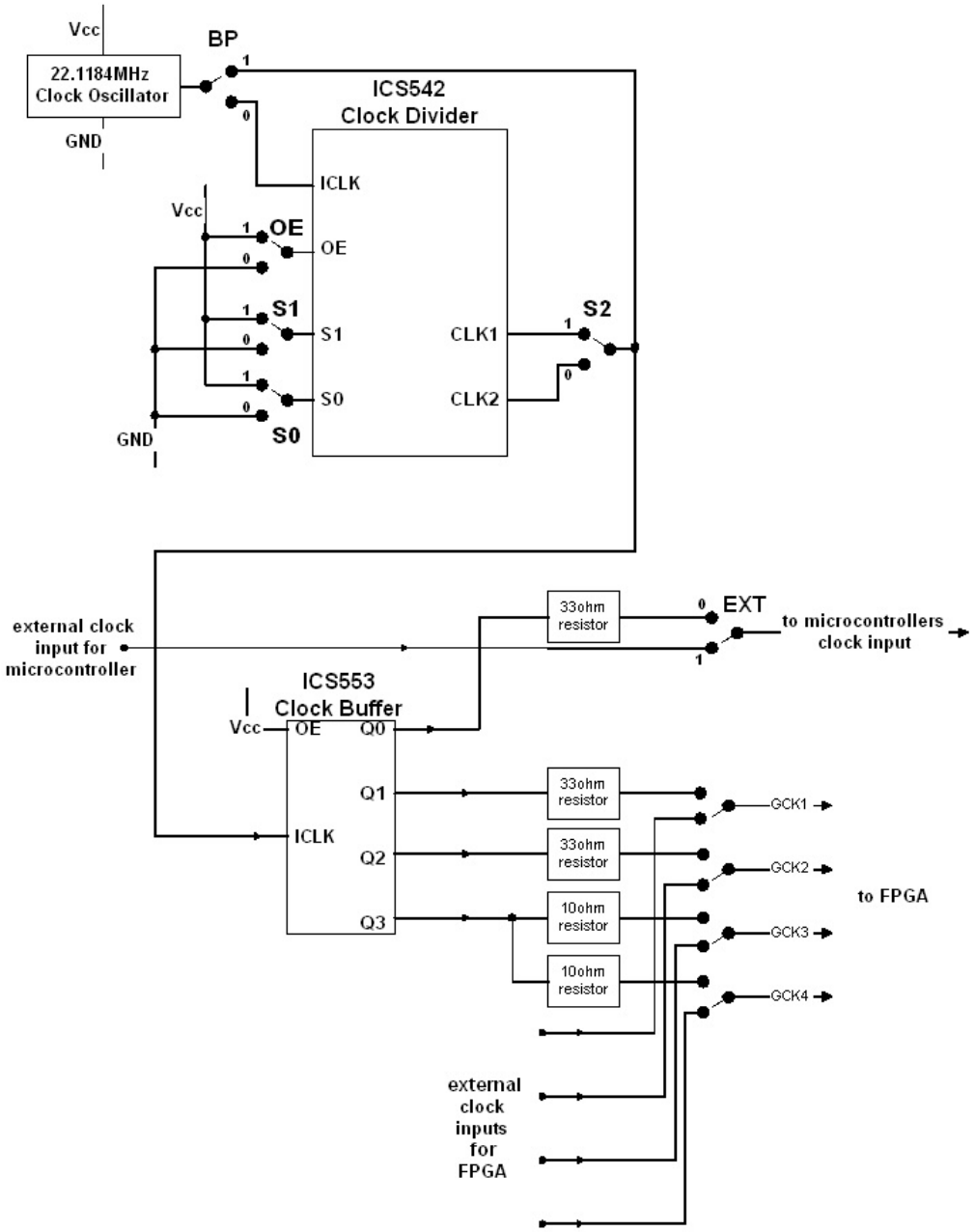


Figure 2.2 Clock generation and distribution

Clock Divider division factor	µC Clock Frequency (MHz)	Switch positions (X = don't care)						Comment
		EXT	BP	OE	S2	S1	S0	
-	**0…**	1	X	X	X	X	X	External clock input
-	**-**	X	X	0	X	X	X	Clock divider disabled
-	**-**	X	X	X	X	0	0	Clock divider power down
16	**1.3824**	0	0	1	0	1	0	
12	**1.8432**	0	0	1	0	0	1	
8	**2.7648**	0	0	1	1	1	0	
6	**3.6864**	0	0	1	1	0	1	
4	**5.5296**	0	0	1	0	1	1	
2	**11.0592**	0	0	1	1	1	1	
1	**22.1184**	0	1	X	X	X	X	Bypassing the clock divider

Table 2.1 Switch settings for frequency selection (with 22.1184MHz clock oscillator frequency)

2.3 User Interface

The part of the board, which is dedicated to different kind of displays, connectors and buttons is called the user interface. In practice, it consists everything else except microcontroller, clock oscillator, memories and FPGA-module.

The following features are included in the user interface:

- Displays and decoders for the parallel I/O lines
- Connectors (excluding power connections) to interface microcontroller's signals
- Buttons and switches
- Power connections and regulations for FPGA

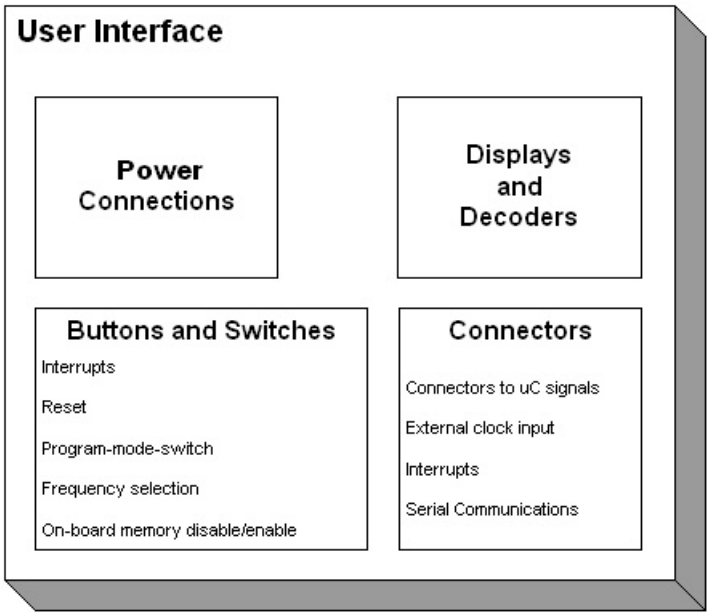


Figure 2.3 User interface

2.3.1 DISPLAYS AND DECODERS

There are no actual displays provided on the board. Nevertheless there are sockets for standard 7-segment displays and 'HexTo7-segment'decoders, as explained hereafter:

- Eight (8) 'HexTo7-segment' decoder/driver/latch circuits (e.g. model: DM9368).
  Each of the displays are used to display 4 bits of the parallel I/O (PIO). Every decoder is to be placed in a 16-lead DIP socket, so user has freedom to choose whether or not to install and/or use the circuits.
- Eight (8) red colored common cathode 7-segment displays (model: TDSR316).
  Color of the example model presented here is red, since red displays have best-fitting (and the lowest) forward voltage per segment when considering their compatibility with the selected decoder circuits. Nevertheless, there are no big differencies between the standard 7-segment displays, so it's no crucial which color user chooses.

There is also one (1) green led for power-on information.

2.3.2 CONNECTORS

- Five (5) DB9/F connectors for serial communication. Refer to chapter 2.3.7 for more information about the serial communication interface of the evaluation board.
- One (1) 5-pin male connector for interfacing external interrupts of the microcontroller.
- Four (4) 26-pin ribbon cable connectors for interfacing all the signals of the microcontroller, excluding MODE_TEST on pin 96 (pulled to V_{SS}).
  Every connector has connection to VCCA, VSSA, VCCB, VSSB and CLK. In addition to VCCA, VSSA, VCCB, VSSB and CLK signals, there are 82 signals in the microcontroller.

Therefore there is one unconnected pin on these four connectors $(82 + 4 \times 5 = 102 \quad 4 \times 26 = 104)$.

NOTE: Connectors are to be located as near as reasonably possible to the microcontroller.

- One (1) BNC connector (PCB mounted, right angle) for external clock input for microcontroller.

Connections between the microcontroller and the interface connectors are shown in ANNEX G.

2.3.3 BUTTONS AND SWITCHES

- Five (5) push-buttons for external interrupts of the microcontroller. Every interrupt button accompanies RC-lowpass filter in order to decrease the bouncing caused by the buttons.
- One (1) push-button to reset the microcontroller.
- One (1) switch to select the start-up mode of the microcontroller.
  From now on, this switch is called as *program-mode-switch*. This switch connects the EA-pin of the microcontroller either to V_{CC} (EA='1') or V_{SS} (EA='0') through a 10kΩ resistor. Therefore, with this switch is made a selection between "programming mode" and "normal mode". Refer to chapter 2.4.3 about the programming and the modes.
- Six (6) DIP-switches to select the desired clocking scheme for the microcontroller. Refer to chapter 2.2.1 about clock frequency selections.
- Two (2) switches to enable/disable the on-board memories – one for program memory flashes and one for data/program memory SRAMs.

2.3.4 POWER CONNECTIONS

The input voltage for the board is +5V DC. One male connector is provided for the input voltage. There is also alternative connector, which enables user to feed different voltages to different parts of the board as shown in figure 2.4 and in table 2.2. This enables user to do ones own setup for voltage and current monitoring, for example for the microcontroller's power consumption measurements.

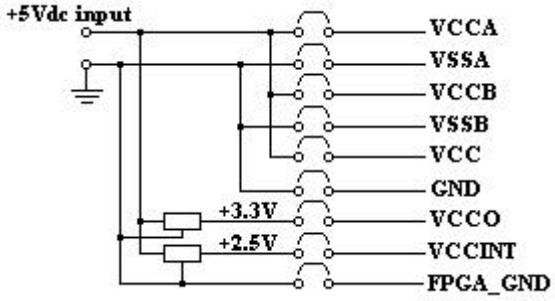


Figure 2.4 Power connections

Node name	Description	Voltage referenced to ground

VCCA	Microcontroller's core supply voltage.	5.0V
VSSA	Microcontroller's core supply ground.	0.0V
VCCB	Microcontroller's I/O supply voltage.	5.0V
VSSB	Microcontroller's I/O supply ground.	0.0V
V_{CCO}	Supply voltage for the output drivers of the FPGA.	3.3V
V_{CCINT}	Supply voltage for the internal core logic of the FPGA.	2.5V
FPGA_GND	FPGA ground	0.0V
V_{CC}	Supply voltage for all other circuitry of the board.	5.0V
GND	Ground reference for all other circuitry of the board.	0.0V

Table 2.2 Supply voltages and grounds of the evaluation board

There are also +3.3V (V_{CCO}) and +2.5V (V_{CCINT}) voltage regulators for the FPGA.
Connecting voltages for FPGA using the alternative power connection shown in figure 2.4 will bypass these regulators.

2.3.5 POWER DISSIPATION

2.3.5.1 Microcontroller

The estimated power consumption for the microcontroller at 10MHz was about 235mW in [1]. When using the same formulae the power consumption at 25MHz is about 400mW.

2.3.5.2 FPGA

Power consumption of the FPGA is highly dependent of the used configuration. By the time of board specification only very rough estimation was done with the information about 79 I/O signals and the clock frequency. Users should check the power needs of their design and apply separate power supply if needed. Xilinx provides a tool for power estimations and it can be found at http://www.xilinx.com/support/techsup/powerest/index.htm (3/2003).
Regulators for V_{CCO} (3.3V) and V_{CCINT} (2.5V) was selected so, that they both can output approximately 2W of power. In addition, configuration with the MultiLINX cable will need approximately additional 2W, when power is drained from the board. During the configuration the input/output power needed from V_{CCO} is minimal, so V_{CCO}-regulator is suitable for that too. It is also possible to use external power source for the MultiLINX cable as presented in chapter 2.5.2.

The power estimation was done for XCV800 FPGA in HQ-240 package. No CLB Logic, Block SelectRAM or Clock Delay Locked Loop Power was selected. This estimation is only based on FPGA's internal functions and 79 I/Os. Internal (V_{CCINT}) logic yields for the power of 155mW. Outputs were driven at 25MHz with LVTTL_24 I/O-standard and on 25% toggle rate. Driving the microcontroller's 79 inputs yields for 61mW for the V_{CCO}. In addition to this, there are also memories, decoders and RS-232 driver on the signal lines. The memory circuits can be driven only one at the time, while all the other memory circuits are disabled. This yields for about 120mW power consumption for V_{CCO}. When assuming that all 32 RAM circuits and 16 ROM circuits are driven at the same time, V_{CCO} power consumption is nearly 1W.
When using inputs instead of outputs V_{CCINT}-power need rises only by few mW. It should be noted that features, which were not tested (CLB Logic, SelectRAM or Clock Delay Locked Loop) affects

on the V_{CCINT} power and not on V_{CCO}, so the estimation for 2W power need for V_{CCINT} is very rough. 2W power need for V_{CCO} was based on the power need of MultiLINX configuration.

2.3.5.3 Flash

The maximum current of each flash memory circuit is specified as 40mA [7]. The current includes the DC operation current as well as frequency dependent component at 6MHz. The frequency component is typically less than 2mA/MHz. Since it takes at least 3 clock cycles to read program (or data) memory, the frequency is not an issue here (when working within the specification of the microcontroller). Therefore the power needs for flash is specified here as (5V x 0.040A) 200mW.

2.3.5.4 SRAM

Absolute maximum power dissipation for each of the SRAMs is specified as 1W [8]. Nevertheless, the specified operating supply current is specified as a maximum of 55mA, with V_{CC}=5.5V, I_{OUT}=0mA and with minimum read cycle time of 55ns. This yields for power of 275mW. Though in normal operation the power would possibly never rise near the maximum power dissipation of 1W, it is used within this specification.

Since only one memory circuit can be active (read or write access) at a time, the power need for memories are specified with memory type, which has higher power consumption. Therefore the power consumption for the memories is specified as 1W.

2.3.5.5 Other circuitry

The total dissipated power for all the other on-board circuitry is shown in table 2.3. It should be noted that when using standard displays and decoders power consumption might rise quite significantly, since one display or decoder circuit might have maximum power dissipation of hundreds of milliwatts.

Device	Dissipated power in watts (with margins)
80S32	0.500
Memory	1.000
Clock Oscillator	0.125
Clock Divider	0.055
MAX240 (UART transceiver)	0.500
Additional Circuitry (Such as multiplexers, 5V MicroMonitor, etc…)	0.200
FPGA	2 + 2 = 4.000
TOTAL	**6.380**

Table 2.3 Power need of the evaluation board (with some margins)

NOTE: MultiLINX cable will require approximately 500mA to 600mA at 3.3V(≈ 2W) from V_{CCO}-regulator, if the cable's power supply connection is connected to the board. This means that MultiLINX cable is powered by the supply connection from the board, but it's also possible to use external power source for the cable.

2.3.6 REGULATORS FOR FPGA

V_{CCO}-regulator is fixed 3.3V low-dropout regulator model LM1117-3.3. In order to guarantee proper working of the V_{CCINT}-regulator, in the name of output current and power, it is model LM317AS. The maximum output current of LM1117 is 800mA so LM317 was selected to give some "margin" for the current, power and the ambient temperature. V_{CCINT}-regulator LM317AS will also need two additional resistors to adjust the output voltage. Both regulators should also have filtering capacitors as presented in [9] and [10]. Information about the regulators is shown in table 2.4 and calculations regarding the regulators can be found in ANNEX B.

	V_{OUT}	**P_L**	**I_L**	
Device	**Output voltage**	**Maximum load power dissipation**	**Maximum load current**	**Package**
LM1117SX-3.3 3.3V Fixed Regulator for V_{CCO}	3.3V	2W	0.610A	TO-263
LM317AS Regulator for V_{CCINT}	2.5V (Two additional resistors needed.)	2W	0.800A	TO-263

Table 2.4 Regulators for FPGA's V_{CCO} and V_{CCINT}.

With TO-263 packages the PCB's copper can be used as a heatsink. The tab of the package is to be soldered to the copper, with no solder mask over the copper area. Adequate copper areas are 0.5 in^2 for V_{CCO}-regulator and 1 in^2 for V_{CCIN}-regulator.[9,10]

2.3.7 SERIAL COMMUNICATIONS

80S32 has one UART for RS-232 communication and 4 extra USARTs, which support three different serial modes: RS-232, PacketWire and TTC-B-01.

There are total of five DB9/F (female) connectors on the evaluation board. These connectors are connected via RS-232 transceiver circuit to microcontroller's UART and to four extra USARTs. Connector CON_S1 for extra USART1 acts as a PacketWire receiver and connector CON_S2 for extra USART2 acts as a PacketWire transmitter during the bootstrap routine. Therefore programming of the program memory during the bootstrap routine is made via these extra USARTs 1 and 2. For signal level conversion, there is one RS-232 transceiver with 5 transmitters and 5 receivers (model: MAX240) on the board.
Only three pins on the DB9-connectors are used. Pin 2 acts as a reception line and pin 3 as a transmission line. Pin 7 is connected to ground. Figure 2.5 and table 2.5 illustrate the connections of the serial communication lines.

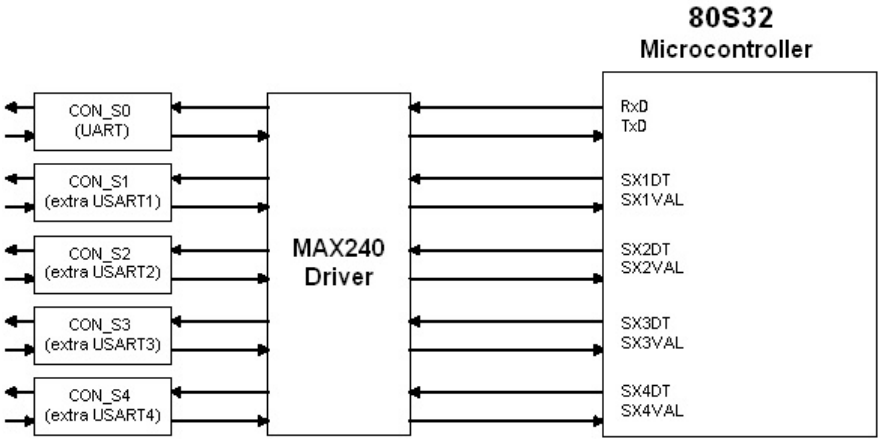


Figure 2.5 Serial communication interface

Pin Number	CON_S0 (UART)	CON_S1 (extra USART1)	CON_S2 (extra USART2)	CON_S3 (extra USART3)	CON_S4 (extra USART4)
1	NC	NC	NC	NC	NC
2	RxD	SX1DT	SX2DT	SX3DT	SX4DT
3	TxD	SX1VAL	SX2VAL	SX3VAL	SX4VAL
4	NC	NC	NC	NC	NC
5	NC	NC	NC	NC	NC
6	NC	NC	NC	NC	NC
7	GND	GND	GND	GND	GND
8	NC	NC	NC	NC	NC
9	NC	NC	NC	NC	NC

Table 2.5 Serial communication signal connections in DB9 connectors

As displayed in table 2.5, extra USARTs clock signals (SXnCLK) are not connected to DB9-connectors, since program download doesn't need CLK. Nevertheless, all UART and USART signals (P30_RXD, P31_TXD, P25_SX1DT, P26_SX1VAL, P27_SX1CLK, P13_SX2DT, P14_SX2VAL, P15_SX2CLK, SX3DT, SX3VAL, SX3CLK, SX4DT, SX4VAL, SX4CLK) are connected to 26-pin connectors, located next to the microcontroller.

Transmission rate of serial communication is obtained using the formula:

$$BitRate = \frac{f_{CLK}}{16 \times SXFREQ}$$

where SXFREQ is a 16-bit register, and it can have values $0 \ldots 2^{16}$.[1]

When solving for f_{CLK}:

$$f_{CLK} = 16 \times SXFREQ \times BitRate$$

For reliable serial communication, the clock frequency of the microcontroller should be as close to the frequency obtained from the previous formula. When using 22.1184MHz frequency and loading SXFREQ with the decimal value '12', we have the rate exactly 115 200bps, which is usually the highest bit rate used with PC's serial port. Because of the on-board frequency divider, we can easily change the bit rate by choosing some other (lower) frequency. Of course it is also possible to change the value of SXFREQ register by programming. Bit rates with their corresponding frequencies are shown in table 2.6, with different values loaded to SXFREQ register.

Bit Rate (bps)	7 200	9 600	14 400	19 200	28 800	57 600	115 200
SXFREQ @ 1.3824 MHz	12	9	6	(4.5)	3	(1.5)	(0.75)
SXFREQ @ 1.8432 MHz	16	12	8	6	4	2	1
SXFREQ @ 2.7648 MHz	24	18	12	9	6	3	(1.5)
SXFREQ @ 3.6864 MHz	32	24	16	12	8	4	2
SXFREQ @ 5.5296 MHz	48	36	24	18	12	6	3
SXFREQ @ 11.0592 MHz	96	72	48	36	24	12	6
SXFREQ @ 16.128 MHz	140	105	70	(52.5)	35	(17.5)	(8.75)
SXFREQ @ 18.432 MHz	160	120	80	60	40	20	10
SXFREQ @ 22.1184 MHz	192	144	96	72	48	24	12

Table 2.6 SXFREQ values and corresponding bit rates with different frequencies

2.4 On-Board Memory

Microcontroller 80S32 (µC) has capabilities to access up to 8MByte of external program memory (ROM) and up to 16MByte of external data memory (RAM), which can also be used as a program memory.
The following figure 2.6 and this chapter will present the on-board memory configuration.

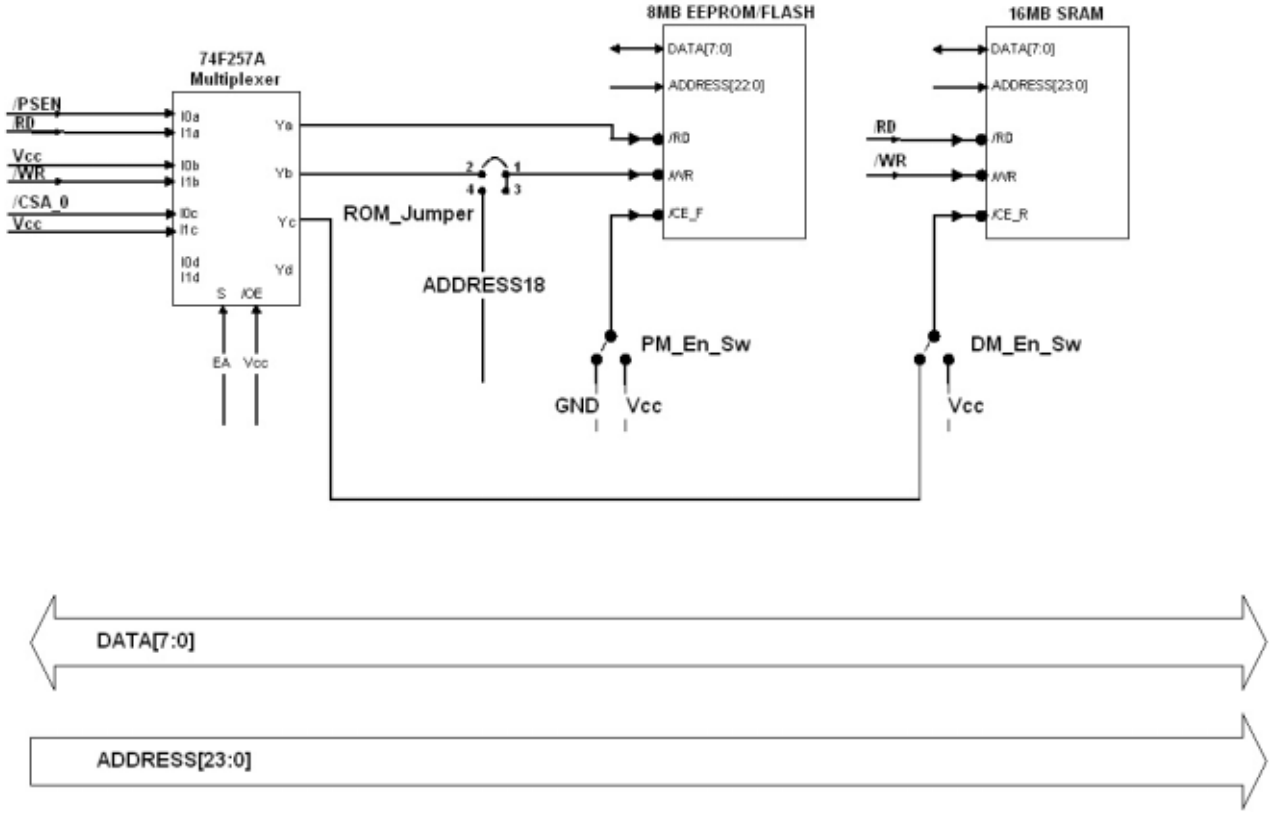


Figure 2.6 On-board memory configuration

(There was trouble finding bigger single chip memories with 5V operating voltage and 8-bit databus. Therefore the selected memory components were the size of 512K x 8 bits, and when the total memory area was covered the amount of memory circuits became quite high.)

2.4.1 PROGRAM MEMORY

8MByte program memory area is made of 16 flash memory circuits. The circuits are AMIC Technology's A29040 Series "512K x 8 Bit CMOS 5.0 Volt-only Uniform Sector Flash Memory". Memories are pinout- and software-compatible with single-power-supply Flash standard and have 55 ns access time. Memories are in Plastic DIP-package, so it is also possible to install some other (PROM/FLASH) memory, if desired. Note, that the memory interface is designed for 512Kbit memories, so every pin-compatible memory up to that size can be installed. For some EPROM circuits of same size (e.g. 27C040) ROM_Jumper, shown in figure 2.6, must be set to the right position as explained in table 2.7. Nevertheless, programming interface is provided for flash only.

Memory type	Jumper setting
Flash	1 – 2
EPROM (with A18 in pin 31)	3 – 4

Table 2.7 Jumper setting for the program memory

The 8MByte flash module is made of 16 flash circuits as stated above - and as shown in figure 2.8. In addition there are also 4-to-16 (1-of-16) Decoder/Multiplexer (74F154) for chip selection.

Decoder has typical propagation delay of 5.5ns. Total typical access delay for flash module is therefore (5.5+55) 60.5ns. In addition to that, multiplexer for /RD and /WR -signals has a typical propagation delay of 4.3ns, giving total access delay for flash memory access (60.5+4.3) 64.8ns.
Entire program (flash) memory module can be disabled (or enabled) with program-memory-enable-switch (PM_En_Sw).

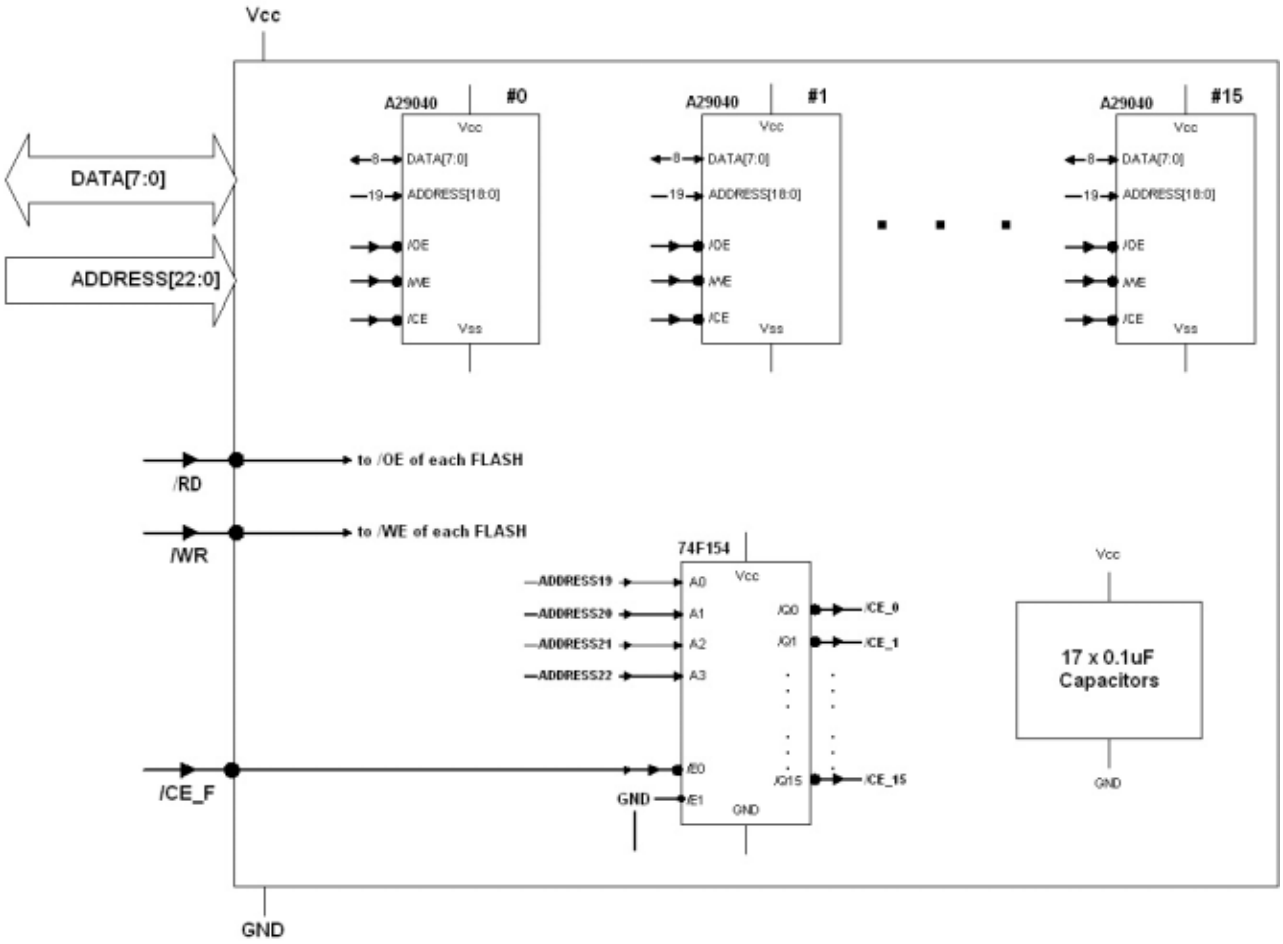


Figure 2.8 Flash memory module

2.4.2 DATA/PROGRAM MEMORY

Part of the data memory area can also be used as a program memory, as presented in [2]. Therefore it is now on called *data/program memory*.
Data/program memory area is physically implemented using 32 SRAMs size of 512Kbits x8. Two 74F154 decoders and one 74F04 inverter are used to create 5-to-32 decoder for SRAM chip selections. SRAM module is shown in figure 2.9 and 5-to-32 decoder is shown in figure 2.10.

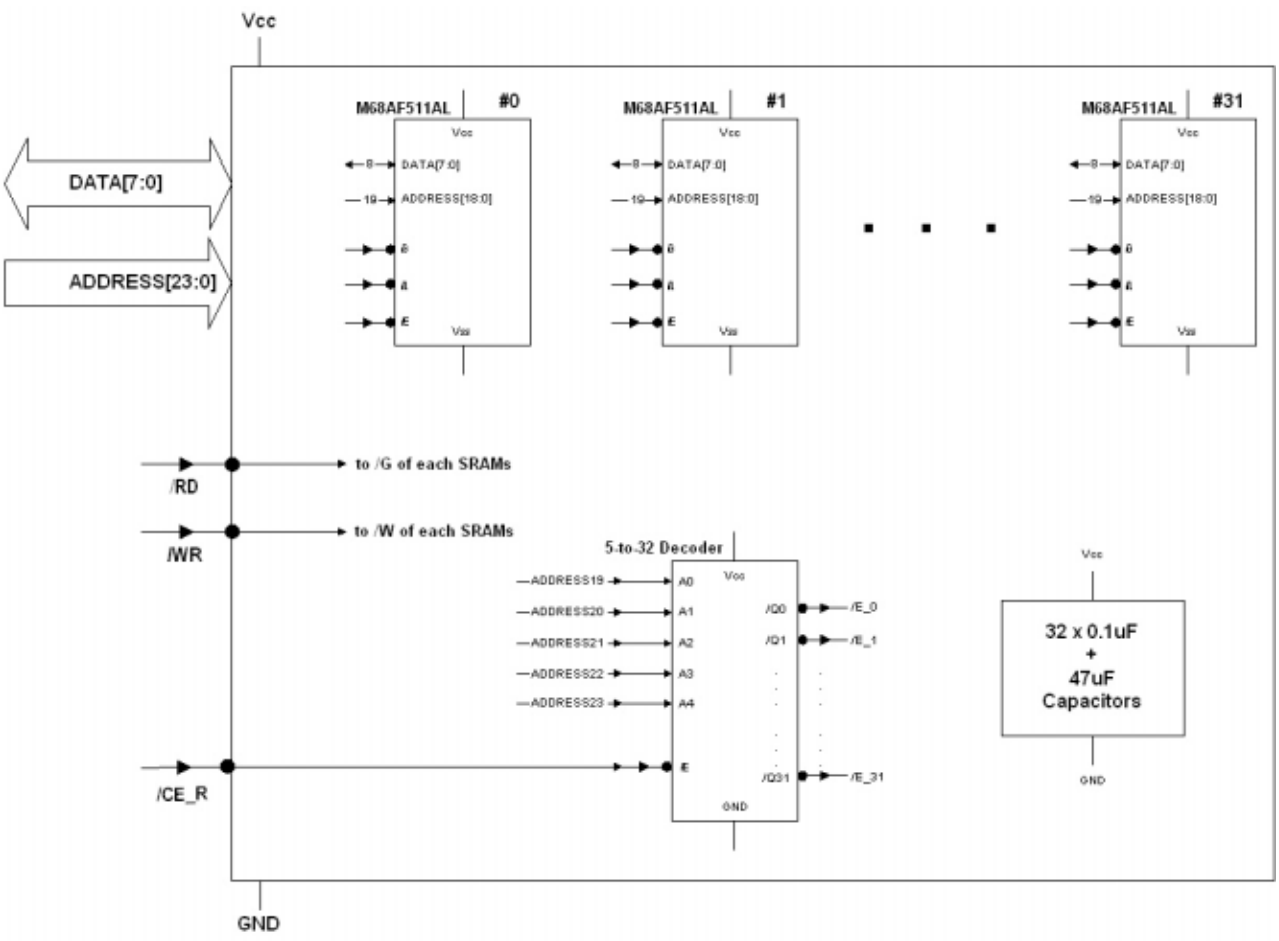


Figure 2.9 SRAM memory module

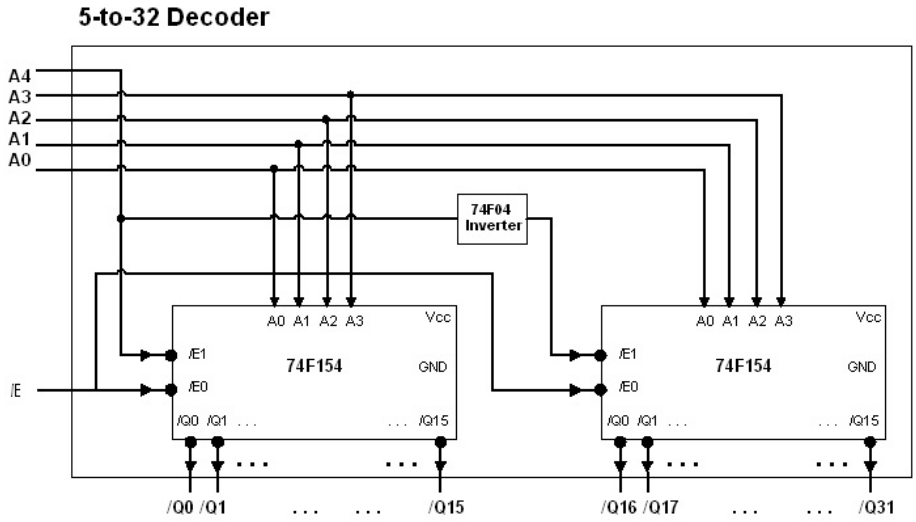


Figure 2.10 5-to-32 Decoder

Memory circuits are ST Microelectronics ‘M68AF511AL55NC6 "4 Mbit (512K x8), 5V Asynchronous SRAM" in TSOP-32 Type II package. Memory is pin-compatible with many other memory circuits with same (or smaller) size, but it should be noted that the memory circuits are surface mounted. SRAMs have 55ns access time. Typical propagation delays for decoders, inverter and multiplexer for /CE_R signals are 5.5, 3.5 and 4.3ns respectively. Therefore, total access time is (55+5.5+3.5+4.3) 67.3ns when using the upper 8MByte of data/program memory and (55+5.5+4.3) 64.9ns when using the lower 8MByte of data/program memory. This is due the inverter in 5-to-32 decoder (see figure 2.10).
It is also possible to disable (or enable) the entire data/program memory module with data-memory-enable-switch (DM_En_Sw).

2.4.3 MEMORY AND PROGRAM USAGE

The “modes” of the memory- and program-usage are determined with the EA-signal of the microcontroller, as explained in [6] and in the following chapter.
After reset, if EA=’1’ program shall be executed from the internal bootstrap or if EA=’0’ program shall be executed from external ROM - in this case from the program memory flash. Internal bootstrap will provide the downloading of the program into the memory. After download, EA is configured as an output at logic level ‘0’.
EA-signal is connected to a multiplexer (74F257A), which is used for connecting the right signals to /WR and /RD inputs of the program memory and enable input (/CE_R) for data/program memory, as showed in figure 2.6.

Before power-up the selection between the states is made with a program-mode-switch, which connects the EA-signal to ‘0’ (gnd) or to ‘1’ (Vcc via 10kΩ resistor. We shall now call these modes as “programming mode” (EA=’1’) and “normal mode” (EA=’0’).

2.4.3.1 Programming mode

EA = ‘1’

Program memory:
Program memory area (up to 8MByte) is accessed with /RD and /WR signals as accessing the normal external data/program memory (RAM). Therefore after the program download, the program memory shall consist the desired program and the program will stay in memory until it is reprogrammed.

Data memory:
Data/program memory area is disabled during the programming. After programming EA is configured as output at logic level ‘0’, and data/program memory is available.

2.4.3.2 Normal mode

EA = ‘0’

Program memory:
Program memory area (up to 8MByte) is accessed with /PSEN signal as accessing the normal external program memory (ROM).

Data memory:

Data/program memory area from 0 to 16MByte is accessed with /CSA_0, /RD and /WR signals.

2.4.3.3 In conclusion

When the program-mode-switch is turned to ‘programming’-state (EA='1'), the program memory is programmed with the help of microcontroller's internal bootstrap routine via the serial communication. During the programming the data/program memory area is disabled. After program download, the downloaded program is started (the last command in the bootstrap routine) and all of the data/program memory area, as well as the program memory area, is accessible. Before resetting or powering-up the board program-mode-switch should be in the desired position – ‘programming’ or ‘not programming’.

There is also possibility to disable the on-board memories with switches – PM_En_Sw for program memory and DM_En_Sw for data/program memory. Therefore the microcontroller can be used without external memories while using only the FPGA – if so desired. Partial assembly is possible by leaving some of the memory circuits for the higher memory space uninstalled. Memory circuits will function when all the memory circuits are not installed, as long as decoders for chip enable signals are present.

2.5 FPGA-Module

The FPGA is used for alternative program run for evaluation/debugging of the microcontroller.

2.5.1 CONNECTIONS TO MICROCONTROLLER

FPGA interfaces to all the functional signals of the microcontroller - total number of 79 I/O-signals. One 96-pin (32x3) VME-type connector is also connected to FGPA, in order to have interface to the board and furthermore to microcontroller via the FGPA. 79 pins of the 96-pin connector are connected to FPGA, enabling also straight-through connection via FGPA to signals connected to the microcontroller. 96-pin connector does not make evaluation board VME-compliant, connector is only same kind as used with VME-boards. Basic idea of this connection is illustrated in figure 2.11.

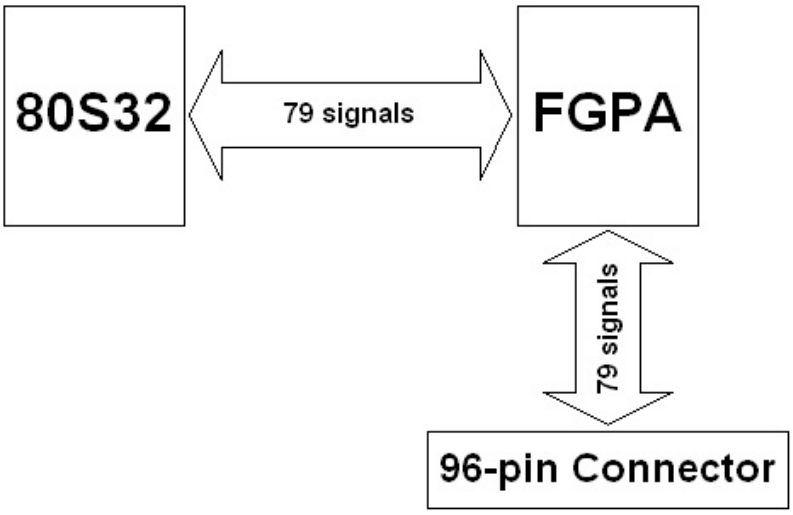


Figure 2.11 Connection between the microcontroller, FPGA and interface connector

FPGA-module includes following features:

- Designed for Xilinx's Virtex FPGAs.
- Socket for 240-pin Plastic Quad Flat Pack or High Heat Dissipation Quad Flat Pack (QFP).
- Footprint-compatible up to XCV300 (in Plastic QFP) or XCV800 (in High Heat Dissipation QFP) with maximum I/O of 166.
- FPGA will interface to all the microcontroller's functional signals presented in table 2.8. Connections are made using LVTTL I/O-standard on FPGA, which is 5V Tolerant I/O (as explained in ANNEX D) with 3.3V output and does not need external reference voltage [3].
- One (1) 96-pin connector for interfacing to FPGA. (See chapter 2.5.1)
- Four (4) BNC connectors (PCB mounted, right angle) for external clock inputs to Global Clock Inputs GCK0, GCK1, GCK2, GCK3, as shown in figure 2.2.
- Four (4) DIP-switches for selecting between external clock source or microcontroller's clock for the FPGA's Global Clock Inputs, as shown in figure 2.2.
- One (1) green led for power-on information.
- 14-pin ribbon cable connector for configurating the FPGA via MultiLINX cable using Boundary Scan connections.
- Three (3) jumpers for selecting the boundary scan modes for configuration.
- One (1) switch to enable/disable FPGA. This switch will keep FPGA waiting the start-up phase, by connecting FPGA's INIT-pin low. When INIT is low, all input/output blocks (IOBs) are tri-stated.

Name	Input/Output	Description	Number of signals
CLK	I	Main system clock	1
/RESET	I	Active low reset	1
ADR[15:0]	O	Address bus for external memory access	16

EXTAD23	O	Bit 23 of the address bus in case of address expansion. Also used for memory protection.[6]	1
DATA[7:0]	I/O	Bi-directional data bus for external memory access	8
/PSE	O	External ROM read signal (active low)	1
/RD	O	External RAM read signal (active low)	1
/WR	O	External RAM write signal (active low)	1
EA	I/O	External Access : after reset EA is used to determine if program shall be executed from the internal bootstrap (EA = '1') or from external ROM (EA = '0'). After program downloading EA is configured as an output at logic level '0'. EA shall be pull to VSS or VCC through a 10 Kohms resistor.	1
SX3DT	I/O	Serial port 3 data line	1
SX3VAL	I/O	Serial port 3 data or validity line	1
SX3CLK	I/O	Serial port 3 clock line	1
SX4DT	I/O	Serial port 4 data line	1
SX4VAL	I/O	Serial port 4 data or validity line	1
SX4CLK	I/O	Serial port 4 clock line	1
P0[7:0]	I/O	Parallel port or alternative function (see table 2.7)	8
P1[7:0]	I/O	Parallel port or alternative function (see table 2.7)	8
P2[7:0]	I/O	Parallel port or alternative function (see table 2.7)	8
P3[7:0]	I/O	Parallel port or alternative function (see table 2.7)	8
CSA[2:0]	O	Chip selects for RAM space	3
CSB[2:0]	O	Chip selects for RAM space	3
INT[3:0]	I	External interrupts (Note: INT4 on port3[7], see table 2.7)	4
		TOTAL NUMBER OF CONNECTED SIGNALS	**79**

Table 2.8 Signals of the microcontroller connected to the FPGA

Most of the parallel port pins of the microcontroller are shared with an alternative function, as listed in table 2.9.

Name	Port	Description
EXTAD22	P0[1]	Bit 22 of the address bus in case of address expansion
EXTAD21	P0[2]	Bit 21 of the address bus in case of address expansion
EXTAD20	P0[3]	Bit 20 of the address bus in case of address expansion
EXTAD19	P0[4]	Bit 19 of the address bus in case of address expansion
EXTAD18	P0[5]	Bit 18 of the address bus in case of address expansion

EXTAD17	P0[6]	Bit 17 of the address bus for address expansion
EXTAD16	P0[7]	Bit 16 of the address bus for address expansion
T2EX	P1[0]	Timer 2 external input
T2CAPT	P1[1]	Timer 2 capture signal
SX2DT	P1[3]	Serial port 2 data line
SX2VAL	P1[4]	Serial port 2 data or validity line
SX2CLK	P1[5]	Serial port 2 clock line
TIMER0_IRQ	P1[6]	Timer0 interrupt(cf. RD1)
TIMER1_IRQ	P1[7]	Timer1 interrupt(cf. RD1)
TIMER2_IRQ	P2[0]	Timer2 interrupt(cf. RD1)
SX1DT	P2[5]	Serial port 1 data line
SX1VAL	P2[6]	Serial port 1 data or validity line
SX1CLK	P2[7]	Serial port 1 clock line
Rxd	P3[0]	Serial port 0 data input
Txd	P3[1]	Serial port 0 data output
T0EX	P3[4]	Timer 0 external input
T1EX	P3[5]	Timer 1 external input
INT4	P3[7]	External interrupt 4 input, active low, configurable as rising/falling edge sensitive or high/low level sensitive

Table 2.9 Alternative port functions of the microcontroller [6]

Since FPGA is connected to all the functional signals of the microcontroller as shown in table 2.8, it can also access the on-board memories. User should be careful not to corrupt the memory contents while using the FPGA.

2.5.2 FPGA CONFIGURATION

FPGA is (re)configurated with MultiLINX cable using the Boundary Scan (JTAG) mode.

The Boundary Scan interface of the FPGA device is always active [4].
As said in [3]: "If the Virtex device is configured on power-up, it is recommended to tie the mode pins to one of the boundary scan configuration mode settings; 101 (M2=1, M1=0, M0=1: contains no pull-ups on I/Os) or 001 (M2=0, M1=0, M0=1: contains pull-ups on I/Os)." Therefore there are jumpers on each mode pin for setting the desired configuration mode.
Boundary Scan modes select the optional pull-ups and prevent configuration in any other modes [4].
Prior to reconfiguration the /PROGRAM pin must be pulled high. Configuration sequence is initiated when the /PROGRAM pin is asserted low. This also resets the TAP controller. In other

words, reconfiguration of the device is possible by toggling the TAP and entering the CFG_IN instruction after pulsing the /PROGRAM pin (low) or issuing the shut-down sequence [4].

More detailed information about configurating the Virtex devices refer to Virtex Datasheet and application notes XAPP139 (Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary Scan), XAPP138 (Virtex FPGA Series Configuration and Readback), XAPP168 (Getting Started with the MultiLINX Cable) and "Quick Start Guide for Parallel Cable IV, MultiPRO and MultiLINX".

The MultiLINX cable is connected to the on board connector as shown in figure 2.12.

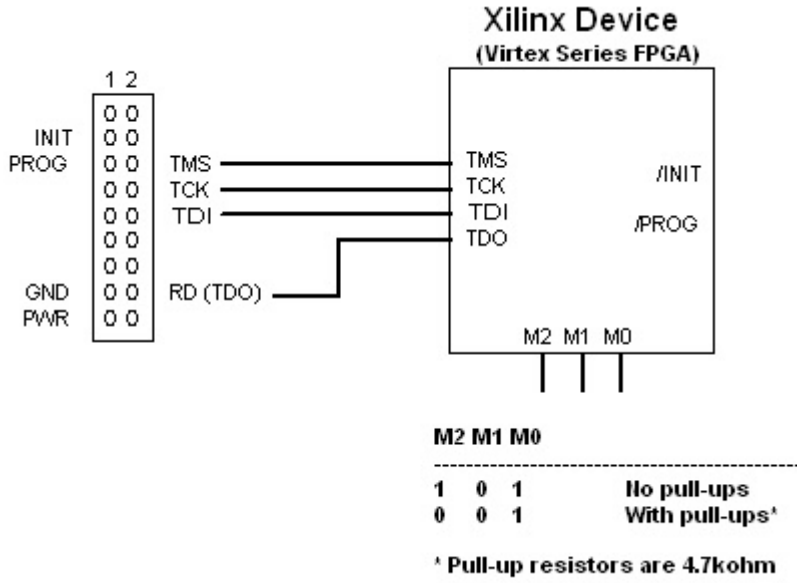


Figure 2.12 MultiLINX connection

Power and Ground leads may also be connected to the separate power supply. It should be noted, that when using the power supply, ground should be common between the target system and the cable. MultiLINX cable requires 3.3V voltage and approximately 500-600mA current.[5]

3 COMPONENTS

3.1 Component List

Opt. = Optional, not installed on board.

Part Type	Quantity	Description	Package
USER INTERFACE			
Displays and Decoders:			
DM9368	8	'HexTo7-segment' decoder/driver/latch circuits **opt.**	PDIP-16
	8	Sockets for DM9368 circuits **opt.**	DIP-16
TDSR316	8	Red-coloured common cathode 7-segment displays **opt.**	Refer to Datasheet
	1	Green Led	
Connectors:			
DB9/F	5	D-type female connector	DB9/F
5-pin male connector	1	Connector for external interrupts	5 pins
26-pin ribbon cable connector	4	Microcontroller interface/debug connector	
BNC Connector	1	External clock input for microcontroller. PCB mount right angle BNC connector	Refer to datasheet
Buttons and switches:			
Push-button	5	Button for External interrupts of the microcontroller	
Push-button	1	Reset button the microcontroller reset	
Switch	1	Program-mode-switch	
DIP-switch	6	Microcontroller clock frequency selector	
Switch	2	Enable/disable switches for on-board memories (PM_En_Sw, DM_En_Sw)	
Jumper	1	ROM_Jumper, for Flash/EPROM selection	
Power connections:			
2-pin power connector	1	+5V dc-input voltage for the board	
	1	Voltage connections for different circuitry	
LM1117SX-3.3	1	Voltage regulator for V_{CCO} (+3.3V)	TO-263
LM317AS	1	Voltage regulator for V_{CCINT} (+2.5V)	TO-263
MICROCONTROLLER:			
80S32	1	ADV 80S32 Microcontroller	MQFP-100 Flat

ZIF-socket	1	ZIF-socket for MQFP-100	
0R	32	Place for post-placement of serial component	0805
DIP-14 socket	1	Socket for clock oscillator	DIP-14
ICS542	1	Clock divider	SOIC-8
ICS553	1	Low Skew 1 to 4 Clock Buffer	SOIC-8
DS1814C-5	1	5 V MicroMonitor, voltage supervisory and reset	SOT-23-5
MAX240CMH	1	RS-232 transceiver	Plastic FP-44
MEMORY:			
DIP-32 Socket	16	Sockets for flash circuits	DIP-32
A29040-55	16	512K x 8 Bit 5.0 Volt-only Flash, 55ns access time	PDIP-32
M68AF511AL55NC6	32	512K x8 5V Asynchronous SRAM, 55ns access time	TSOP-32 Type II
74F257A	1	Quad 2-line to 1-line selector/ multiplexer, non-inverting (3-State)	SO-16
N74F154D	3	1-of-16 decoder/demultiplexer	SO-24
N74F04D	1	Hex Inverter	SO-14
FPGA-MODULE:			
	1	Virtex Series FPGA$^{opt.}$	Plastic or High Heat Dissipation QFP
	1	Socket for 240-pin Plastic/High Heat Dissipation QFP	
96-pin connector	1	External interface to the FPGA	96-pin (32 pins in 3 rows) VME connector
BNC connector	4	External clock inputs for Global Clock Inputs. PCB mount right angle BNC connector	Refer to datasheet
DIP-switch	4	Clock source selector for FPGA	
Green led	2	V_{CCO} and V_{CCINT} power leds	
14-pin ribbon cable connector	1	Configuration connector for MultiLINX cable	
Jumper	3	Boundary Scan Configuration mode select	
Switch	1	FPGA enable/disable.	

Table 3.1 Component list of the specified components

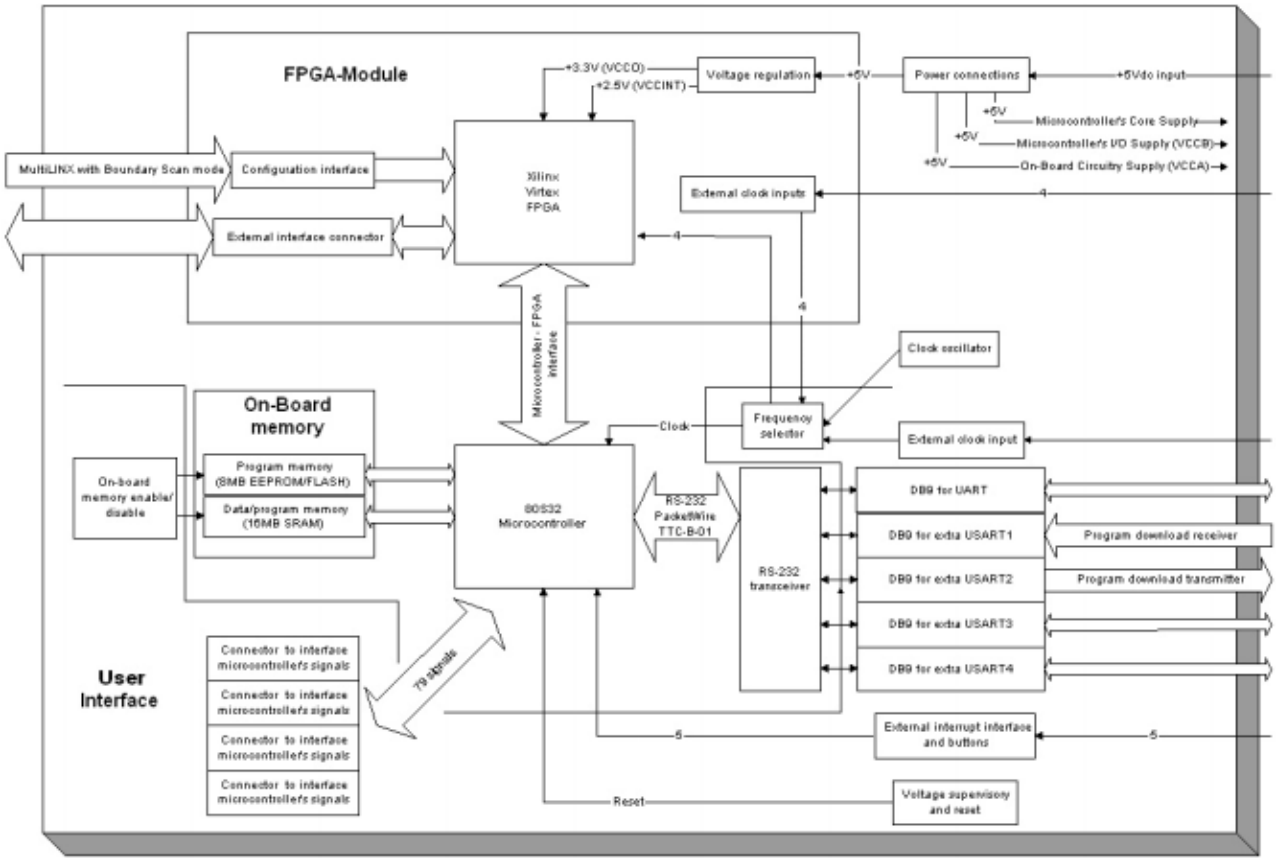
3.2 Links to component information

Part Type	Manufacturer	WWW-link

DM9368	Fairchild Semiconductor	http://www.fairchildsemi.com/pf/DM/DM9368.html
TDSR316	Vishay Semiconductors	http://www.vishay.com/docs/83125/83125.pdf
DB9/F		http://www.pin-outs.com/datasheet_11.html
LM1117SX-3.3	National Semiconductor	http://www.national.com/pf/LM/LM1117.html
LM317AS	National Semiconductor	http://www.national.com/pf/LM/LM317.html
80S32	ADV Engineering	For datasheet contact TOS-ESM at ESTEC (ESA).
BNC connector		http://www.dixel.co.il/astron/spec/k-05.pdf
ICS542	Integrated Circuit Systems, Inc.	http://www.icst.com/products/summary/ics542.htm
ICS553	Integrated Circuit Systems, Inc.	http://www.icst.com/products/summary/ics553.htm
DS1814C-5	Maxim Integrated Products, Inc.	http://www.maxim-ic.com/quick_view2.cfm/qv_pk/2788/ln/en
MAX240CMH	Maxim Integrated Products, Inc.	http://www.maxim-ic.com/quick_view2.cfm/qv_pk/1798/ln/en
A29040-55	AMIC Technology, Inc.	http://www.amictechnology.com/pdf/A29040A.pdf
M68AF511AL55NC6	ST Microelectronics	http://us.st.com/stonline/books/pdf/docs/7992.pdf
74F257A	Philips Semiconductors	http://www.philipslogic.com/products/fast/pdf/74f257a.pdf
N74F154D	Philips Semiconductors	http://www.philipslogic.com/products/fast/pdf/74f154.pdf
N74F04D	Philips Semiconductors	http://www.philipslogic.com/products/fast/pdf/74f04.pdf
Virtex Series FPGA	Xilinx, Inc.	http://www.xilinx.com/xlnx/xil_prodcat_product.jsp?title=ss_vir
96-pin connector		http://www.interfacebus.com/Design_VME_Connectors.html

Table 3.2 Manufacturers and links to datasheets of the specified components

4 ANNEX A – DETAILED BLOCK DIAGRAM



5 ANNEX B - REGULATOR POWER DISSIPATION [9,10]

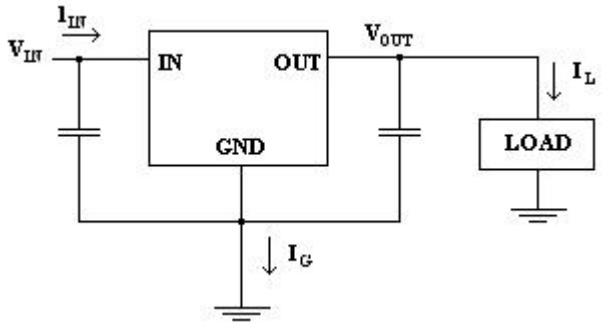
The power dissipation of the regulators can be obtained, as expressed in [9] with the equation:

$$P_D = (V_{IN} - V_{OUT})I_L + V_{IN} I_G$$

Equation can also be written as the difference between input and output powers:

$$7\,P_D = P_{IN} - P_{OUT} = V_{IN} I_{IN} - V_{OUT} I_L$$

where $I_{IN} = I_L + I_G$, as shown in figure below.



Power dissipation diagram of the regulator

The maximum allowable temperature rise (T_R(max)) and junction-to-air thermal resistance (θ_{JA}) can be calculated as shown in the following equations:

$$T_R(\max) = T_J(\max) - T_A(\max)$$

and

$$\theta_{JA} = \frac{T_R(\max)}{P_D} = \frac{T_J(\max) - T_A(\max)}{P_D}$$

where

$T_J(max)$	is the maximum allowable junction temperature (in this case 125°C)
$T_A(max)$	is the maximum allowable ambient temperature
P_D	is power dissipation of the regulator

	V_{OUT}	P_L	I_L	P_D	$\theta_{JA(25)}$	$\theta_{JA(50)}$	
Device	**Output voltage**	**Maximum load power dissipation**	**Maximum load current**	**Maximum regulator power dissipation**	**Junction-to-air thermal resistance at 25°C**	**Junction-to-air thermal resistance at 50°C**	**Package**

LM1117SX-3.3 3.3V Fixed Regulator for V_{CCO}	3.3V	2W	0,610A	1.09W	109°C/W	68.8°C/W	TO-263
LM317AS Regulator for V_{CCINT}	2.5V (Two additional resistors needed.)	2W	0,800A	2.0W	50°C/W	37.5°C/W	TO-263

Regulators for FPGA's V_{CCO} and V_{CCINT}

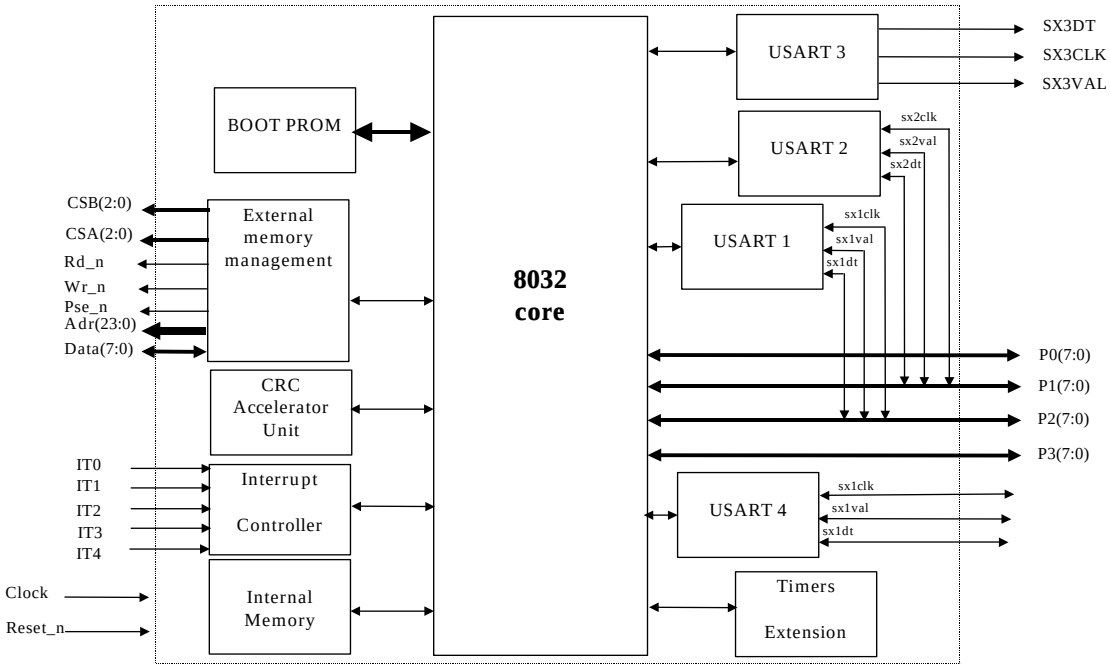
6 ANNEX C – 80S32 FEATURES AND CHARACTERISTICS

6.1 Specific features:

Page 20 from 'Final Report – Microcontroller for On-Board Data Handling' by P. Mercier, ADV Engineering (09.11.2001).

The 80S32 is a high performance microcontroller. It is fully compatible with the well-known 80C32/80C52 device and the technology combines high execution speed with high level of integration. Some features have been added to the 80C32 device and the performance has been increased by a factor of 3 that means a processing power of about 3 MIPS at 20 MHz. This device is powerful enough to handle the requirements of embedded on board applications.

- 512 bytes on-chip memory ;
- Full 64 Kbytes addressing range for program and data, with expansion up to 16 Mbytes for data and 8 Mbytes for program;
- De-multiplexed Address / Data bus ;
- Memory protection for both internal and external memory;
- Program downloading and program execution from RAM capabilities;
- Fives serial interfaces:
  - One RS232 UART;
  - Four extra configurable USARTs (RS232, PacketWire and TTC-B-01 compatible);
  - two 64 bytes FIFO that can be associated to one of the extra USART and used as emission or reception buffer;
- Three 16-bit counters / timers with extended time count duration;
- Five external interrupts with two priority levels;
- A CRC calculation acceleration unit compatible with CCSDS TM and TC packets;
- Latch-up immune. Total dose > 50Krads. SEU > 20Mev and greater than 100 Mev for hardened Flip-Flops.



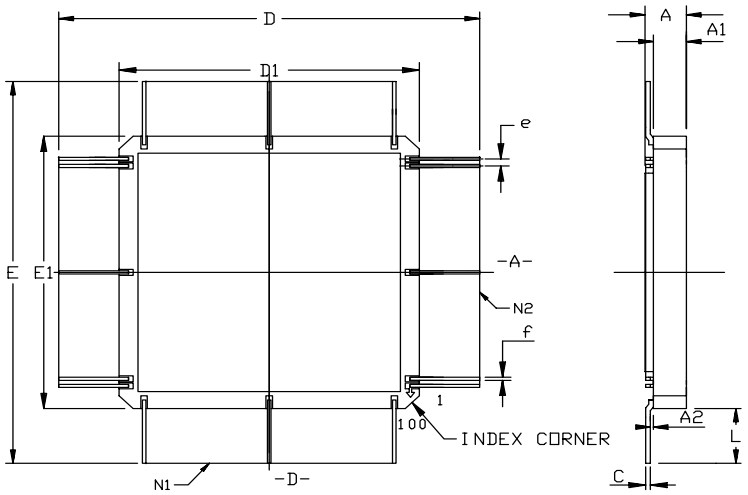
6.2 Package dimensions:

Page 74 from ‘ADV80S32 Datasheet v2.5’ (22.05.2001).

TEMIC Semiconductors

Mechanical Data

100 LEAD MQFP FLAT



	Min	Max	Min	Max
A	2.21	2.67	.087	.105
C	0.15	0.20	.006	.008
D	33.80	35.30	1.331	1.390
D1	18.80	19.30	.740	.760
E	33.80	35.30	1.331	1.390
E1	18.80	19.30	.740	.760
e	0.635 BSC		.025 BSC	
f	0.254 REF		.010 REF	
A1	1.83	2.24	.072	.088
A2	0.203 REF		.008 REF	
L	7.50	8.00	.295	.315
N1	25		25	
N2	25		25	

PACKAGE CODE : U68
INTERNAL CODE : KU
MHS S.A.

REV : A DATE : 01-03-00

6.3 Electrical Characteristics:

Pages 77-81 from ‘ADV80S32 Datasheet v2.5’ (22.05.2001).

6.3.1 MAXIMUM RATINGS

Parameter	**Min**	**Max**	**Unit**

Supply Voltage	-0.5	7.0	V
Input Voltage	Vss - 0.3	Vcc + 0.3	V
Operating Temperature	-55	+125	°C
Storage Temperature	-65	+150	°C

6.3.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ.	Max	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.2	-	Vcc	V
VIL	Input Low Voltage	-0.3	0	0.8	V
T_{Clock}	Clock period	50			ns
	Duty cycle			45	%

6.3.3 DC PARAMETERS (MIN, MAX VALUES).

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
VOH	Output high voltage	Vcc = 4.5 v, I_{OH} = 6 or 3 mA	3.9	-	-	V
VOL	Output low voltage	Vcc = 4.5 v, Iol = -6 or 3 mA	-	-	0.4	V
IIX	Input leakage current		-10.0		+10.0	µA

6.3.4 AC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max	Unit
t1	Clock rising edge to Pse_n/Rd_n low time for program memory accesses			19	ns

t2	Clock rising edge to Address valid time for program memory accesses			28	ns
t3	Clock rising edge to Pse_n / Rd_n high time for program memory accesses			18	ns
t4	Clock rising edge to Address invalid time for program memory accesses			28	ns
t5	Data set-up time for non-protected program memory accesses	2			ns
t6	Data hold time for non-protected program memory accesses	1			ns
t7	Clock falling edge to ExtAd23 high time			16	ns
t8	Data set-up time for protected program memory accesses	8			ns
t9	Data hold time for protected program memory accesses	0			ns
t10	Protection code set-up time for protected program memory accesses	1			ns
t11	Protection code hold time for protected program memory accesses	0			ns
t12	Clock rising edge to Rd_n low time for data memory accesses			19	ns
t13	Clock rising edge to Address valid time for data memory accesses			27	ns
t14	Clock rising edge to Rd_n high time for data memory accesses			18	ns
t15	Clock rising edge to Address invalid time for data memory accesses			27	ns
t16	Data set-up time for non-protected data memory accesses	2			ns
t17	Data hold time for non-protected data memory accesses	0			ns
t18	Data set-up time for protected date memory accesses	6			ns
t19	Data hold time for protected data memory accesses	0			ns
t20	Protection code set-up time for protected data memory accesses	1			ns
t21	Clock rising edge to Wr_n low time for data memory accesses			19	ns

t22	Clock rising edge to Wr_n high time for data memory accesses			19	ns

PacketWire transfer timings :

T23	SXVAL assertion to SXCLK rising (reception mode)	1			T_{Clock}
T24	SXCLK period (reception mode)	4			T_{Clock}
T25	SXCLK falling to SXVAL deassertion (reception mode)	0			T_{Clock}
T26	SXDT Set-up Time (reception mode)	-1			ns
T27	SXDT hold time (reception mode)	2			ns
t28	SXVAL assertion to SXCLK rising (transmission mode)		0.5 T_{trans} + 1 T_{Clock}		T_{trans}
t29 T_{trans}	SXCLK period (transmission mode)	16			T_{Clock}
t30	SXVAL assertion to SXDT valid (transmission mode)		0.5 T_{trans} + 1 T_{Clock}		
t31	SXCLK falling to SXDT valid (transmission mode)		0		T_{Clock}
t32	SXCLK falling to SXVAL deassertion (transmission mode)		0		T_{trans}

T_{trans} is the transmission period defined with the SXFREQ registers

TTC-B-01 transfer timings :

t33	SXVAL falling to SXDT valid : ➢ transmission – master mode ➢ transmission – slave mode		 1 3		T_{Clock}
t34	SXVAL falling to SXCLK falling : ➢ master mode, ➢ slave mode	 2	 7		 T_{trans} T_{Clock}
t35	SXDT set-up time ➢ transmission mode ➢ reception mode	 3			 T_{Clock}
t36	SXDT hold time ➢ transmission mode ➢ reception mode	 1 1		 4	 T_{Clock} T_{Clock}
t37 = Ttrans	SXCLK period ➢ master mode, ➢ slave mode	 4			 T_{Clock}

t38	SXCLK rising to SXVAL rising : ➢ master mode, ➢ slave mode	 2	 0.5		 T_{trans} T_{Clock}
t39	Minimum time between 2 transfers: ➢ master mode, ➢ slave mode	 2	 1		 T_{trans} T_{Clock}
t40	Intermediate gap : ➢ master mode, ➢ slave mode	 2	 8,5		 T_{trans} T_{Clock}

T_{trans} is the transmission period defined with the SXFREQ registers

7 ANNEX D – FPGA AND 5V I/O

Usually some coupling would be needed in order to connect circuits using different voltage levels. Virtex series FPGA can be used with different I/O standards, as explained in [11]. Some of those standards are 5V tolerant, such as LVTTL, which uses 3.3V voltage level. Compatibility between Virtex and 5V systems are shown in the following table.

Driving Device	Receiving Device	5V Compatible
Virtex	5V TTL	Yes
5V TTL	Virtex	Yes
Virtex	5V CMOS	Yes, provided that outputs are tri-stated and external pull-up resistor to 5V is included as explained in [].
5V CMOS	Virtex	Yes

Virtex series FPGA 5V I/O compatibility [11]

Since the voltage levels of the microcontroller are as shown in ANNEX C, or in [6], there is no need for any extra glue logic or pull-ups between FPGA and microcontroller.

8 ANNEX E – SWITCHES, BUTTONS AND JUMPERS

NAME		'0' or Open	'1' or Close	DESCRIPTION
SW1		FPGA enabled	FPGA disabled	FPGA enable/disable
SW2			µC reset	µC reset push-button
SW3			µC interrupt on INT4	µC interrupt push-button, INT4
SW4			µC interrupt on INT3	µC interrupt push-button, INT3
SW5			µC interrupt on INT2	µC interrupt push-button, INT2
SW6			µC interrupt on INT1	µC interrupt push-button, INT1
SW7			µC interrupt on INT0	µC interrupt push-button, INT0
SW8	DM_En_Sw		Data memory disabled	Data memory enable/disable
SW9	PM_En_Sw	Program memory enabled	Program memory disabled	Program memory enable/disable
SW10a		On-board clock source	Èxternal clock source	"External clock / on-board clock" – selection for GCK0
SW10b		On-board clock source	Èxternal clock source	"External clock / on-board clock" – selection for GCK1
SW10c		On-board clock source	Èxternal clock source	"External clock / on-board clock" – selection for GCK2
SW10d		On-board clock source	Èxternal clock source	"External clock / on-board clock" – selection for GCK3
SW11a	BP		By-pass clock divider	Clock divider by-pass
SW11b	S2	CLK2	CLK	Clock divider CLK/CLK2 –selection
SW11c	EXT	On-board clock source	Èxternal clock source	µC "external clock / on-board clock" – selection
SW12a	S1	S1 = '0'	S1 = '1'	Clock divider S1 input
SW12b	S0	S0 = '0'	S0 = '1'	Clock divider S0 input
SW12c	OE	Output disable	Output enable	Clock divider output enable
SW13		EA = '0'	EA = '1'	Program mode switch

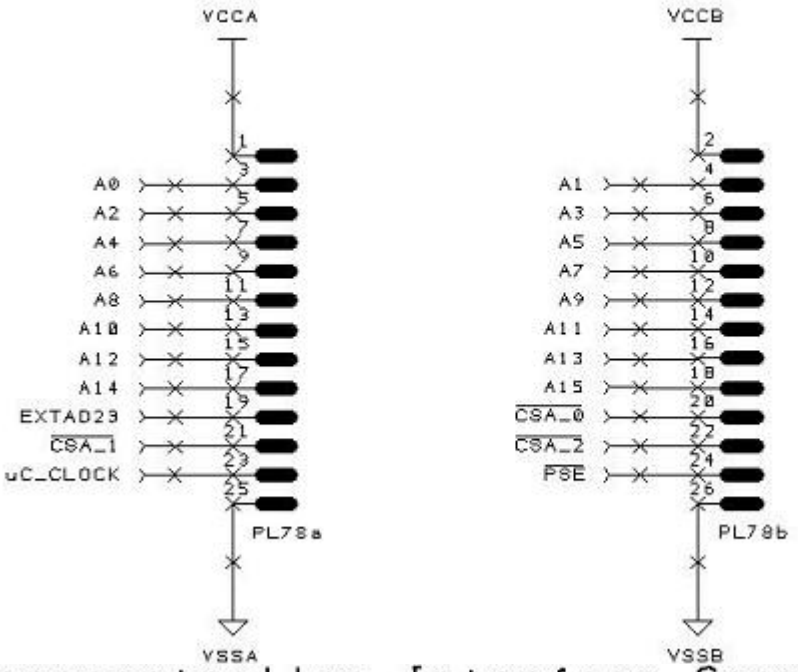
NAME				DESCRIPTION
J1		UNSET: M0 = '1'	SET: M0 = '0'	Configuration mode select, M0
J2		UNSET: M1 = '1'	SET: M1 = '0'	Configuration mode select, M1
J3		UNSET: M2 = '1'	SET: M2 = '0'	Configuration mode select, M2
J4	ROM_Jumper	1-2: FLASH	3-4: EPROM	FLASH/EPROM –selection

9 ANNEX F – CONNECTOR OVERVIEW

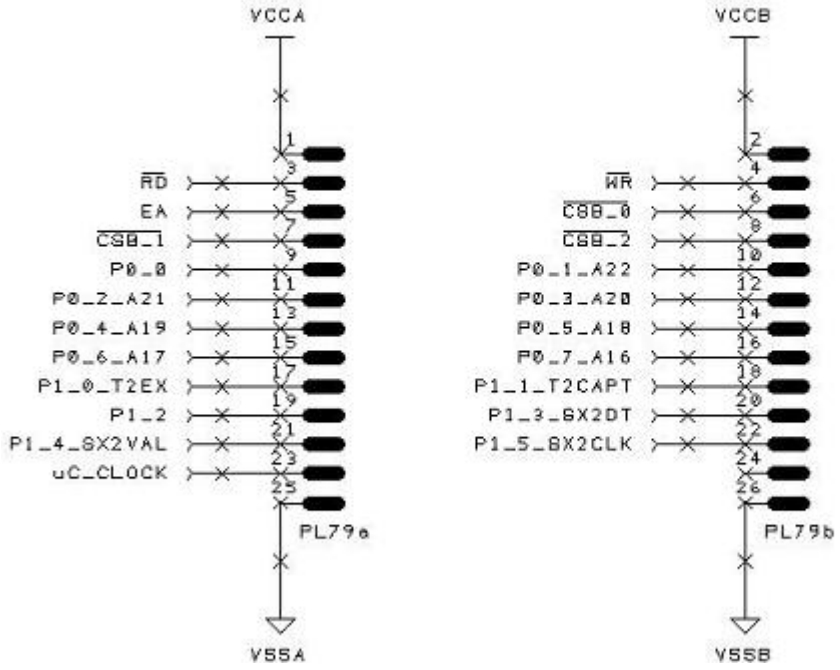
NAME	DESCRIPTION
Vin	+5Vdc input
CONN1	Alternative voltage input for different blocks (2x9 pins)
CONN2	FPGA external interface (96-pin VME-type connector)
CONNJTAG	MultiLINX cable connector
CONN4	µC external interrupt connector
CONN5	26-pin µC interface connector
CONN6	26-pin µC interface connector
CONN7	26-pin µC interface connector
CONN8	26-pin µC interface connector
CONN9	µC external clock source (BNC connector)
CONN10	GCK0 external clock source (BNC connector)
CONN11	GCK1 external clock source (BNC connector)
CONN12	GCK2 external clock source (BNC connector)
CONN13	GCK3 external clock source (BNC connector)
CONS0	DB9/F UART connector
CONS1	DB9/F extra USART1 connector
CONS2	DB9/F extra USART2 connector
CONS3	DB9/F extra USART3 connector
CONS4	DB9/F extra USART4 connector

10 ANNEX G – MICROCONTROLLER INTERFACE CONNECTORS

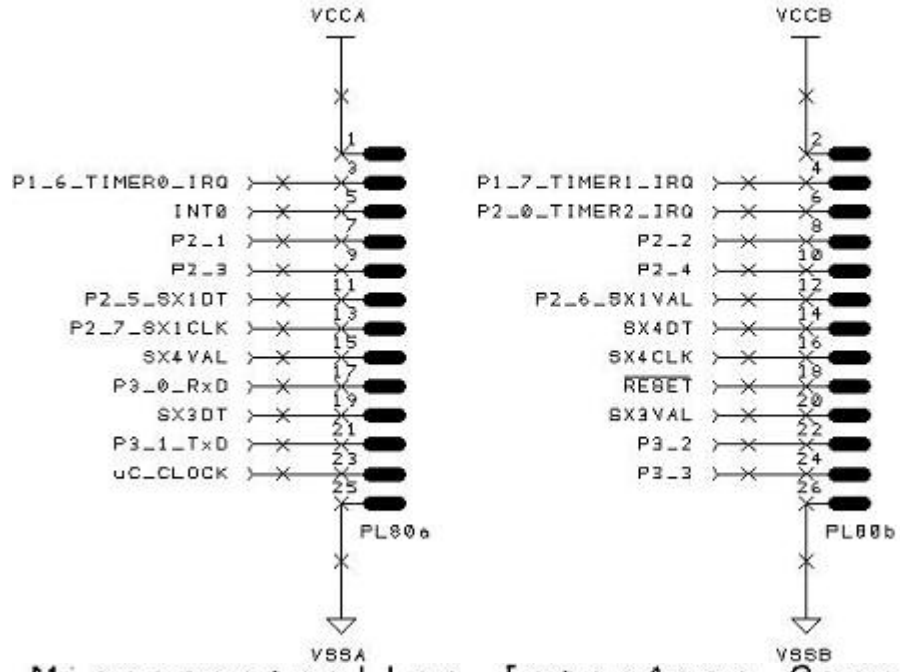
Microcontroller Interface Connector #1



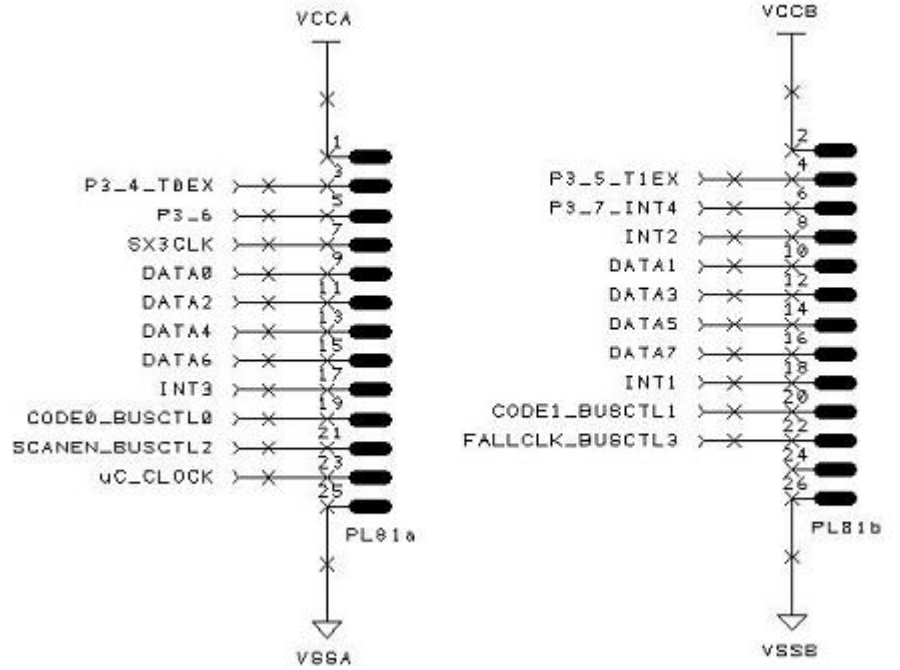
Microcontroller Interface Connector #2



Microcontroller Interface Connector #3



Microcontroller Interface Connector #4



11 ANNEX H – FPGA EXTERNAL INTERFACE CONNECTOR

96-pin VME-type connector (32 pins in 3 rows)			
	a	**b**	**c**
1		FPGA_238 *	FPGA_237 *
2	FPGA_236 r	FPGA_235 *	FPGA_234 *
3	FPGA_232 R	FPGA_231 *	FPGA_230 r
4	FPGA_229 r	FPGA_228 *	FPGA_224 *
5	FPGA_223 *	FPGA_222 r	FPGA_221 *
6	FPGA_220 *	FPGA_218 R	FPGA_217 *
7	FPGA_216 *	FPGA_215 r	FPGA_209 *
8	FPGA_208	FPGA_207 *	FPGA_206 *
9	FPGA_GND	FPGA_205 R	GND
10	FPGA_203 *	FPGA_202 *	FPGA_201 r
11	FPGA_GND	FPGA_200 *	FPGA_199 *
12	FPGA_195 *	FPGA_194 r	FPGA_193 r
13	FPGA_192 *	FPGA_191 R	FPGA_189 *
14	FPGA_188 *	FPGA_187 r	FPGA_186 *
15	FPGA_GND	FPGA_176 *	FPGA_175 r
16	FPGA_174 *	FPGA_173 *	FPGA_171 R
17	FPGA_GND	FPGA_170 *	FPGA_169 r
18	FPGA_168 r	FPGA_167 (D1) *	FPGA_163 (D2) *
19	FPGA_GND	FPGA_162 *	FPGA_161 r
20	FPGA_160 *	FPGA_159 *	FPGA_157 R
21	FPGA_156 (D3) *	FPGA_155 *	FPGA_154 r
22	FPGA_153 *	FPGA_152 *	FPGA_149 *
23	FPGA_147 r	FPGA_GND	FPGA_146 *
24	FPGA_145 (D4) *	FPGA_144 R	FPGA_142 *
25	FPGA_141 *	FPGA_140 r	FPGA_139 *
26	FPGA_138 (D5) *	FPGA_134 (D6) *	FPGA_133 r
27	FPGA_132 r	FPGA_131 *	FPGA_130 R
28	FPGA_128 *	FPGA_127 *	FPGA_126 r
29	FPGA_125 *	FPGA_124 (D7) *	
30			
31			
32	V_{CCINT}	V_{CCO}	V_{CC}

* General purpose I/O.

r Device-dependent V_{REF}, remains I/O on smaller devices.

R V_{REF}

Within each bank, if input reference voltage is not required , all V_{REF} pins are general I/O.

12 ANNEX I – FPGA CONFIGURATION CONNECTOR

14-pin ribbon cable connector	
1	Not connected
2	Not connected
3	Not connected
4	Not connected
5	Not connected
6	TMS
7	Not connected
8	TCK
9	Not connected
10	TDI
11	Ground connected to FPGA_GND.
12	TDO
13	+3.3V supply for cable. Connected to V_{CCO}. Leave unconnected when using external power supply.
14	Not connected

13 ANNEX J – FPGA BYPASS CAPACITORS

"The function of the bypass capacitor is to provide local energy storage. This local energy storage must be available over a broad frequency range. Very small capacitors with low series inductance are used to provide fast current for the high frequency transitions. Larger, slower capacitors continue to supply current after the high-frequency capacitors energy is expended. Current FPGA technology requires capacitance in three frequency ranges, referred to as high, medium, and low. These frequencies span from the 1KHz range to the 500MHz range—the switching knee frequency. The knee frequency is related to the edge rates of logic transitions and may be approximated by taking the reciprocal of twice the signal rise time."[14]

Device	System Gates	CLB Array	Logic Cells	Max. Available I/O	Block RAM Bits	Max. SelectRAM+™ Bits
XCV50	57 906	16x24	1 728	180	32 768	24 576
XCV100	108 904	20x30	2 700	180	40 960	28 400
XCV150	164 674	24x36	3 888	260	49 152	55 296
XCV200	236 666	28x42	5 292	284	57 344	75 264
XCV300	322 970	32x48	6 912	316	65 536	98 304
XCV400	468 252	40x60	10 800	404	81 920	153 600
XCV600	661 111	48x72	15 552	512	98 304	221 184
XCV800	888 439	56x84	21 168	512	114 688	301 056

Table 13.1 Virtex FPGA Family Members [12]

	Device	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800
Package	**PQ240**	*	*	*	*	*			
	HQ240						*	*	*

Table 13.2 PQ240 and HQ240 package assignments [12]

All device/package choices presented in table 13.2 have maximum of 166 user I/O (excluding dedicated clock pins). Virtex Family FPGA in PQ240 or HQ240 package has 98 General Purpose I/O pins, 16 V_{CCO} pins, 12 V_{CCINT} pins, 32 GND pins, 7 V_{REF} and/or I/O pins at 8 banks (= 56 pins) and 26 other special purpose and/or general I/O pins. Refer to [12] for more specific data.

13.1 Core Voltage (V_{CCINT}) Bypass Capacitors

13.1.1 HIGH-FREQUENCY CAPACITORS

"In order to keep the V_{CCINT} variation (noise) small, the bypass capacitance must be much larger than the FPGA equivalent capacitance. The high-frequency bypass capacitance should be a factor of 25 to 100 times bigger than the FPGA equivalent capacitance."[14]

Generally small capacitors with low series inductance providing fast current for high-frequency transitions. Meaning usually 0.1µF to 0.001µF ceramic SMD capacitor.

Capacitors should be placed as close to the V_{CC}/GND pins as possible – usually this means placing the component underside of the board, if possible.

Minimum size of each high-frequency V_{CCINT} bybass-capacitor (C_{BI}) can be calculated with the formula:[14]

$$C_{BI} = \frac{S \times \frac{P}{V^2 f}}{N_P}$$

where

S	is the scale factor corresponding the variation in V_{CCINT} (e.g. S=50 for 2% or 100 for 1% variation)
P	is the power consumption of the FPGA in watts
V	is V_{CCINT} in volts
f	is the operating frequency in hertz
N_P	is the number of V_{CCINT} pins

13.1.2 MIDDLE-FREQUENCY CAPACITORS

Larger, slower capacitors continue to supply current after the high-frequency capacitors energy is expended. Usually 47 to 100µF tantalum capacitors, or if not available also low-inductance aluminum electrolytic may be used.

There should be at least one middle-frequency capacitor for every 1500 CLBs in the device. When using XCV50…XCV800 FPGAs, four 47-100µF tantalums or aluminum electrolytic should be adeguate.

13.1.3 LOW-FREQUENCY CAPACITORS

At least one 470µF to 3300µF low-frequency capacitor for every four FPGAs may be mounted anywhere on the board.[14]

13.2 I/O Power Supply (V_{CCO}) Bypass Capacitors

13.2.1 HIGH-FREQUENCY CAPACITORS

The size of the FPGA's equivalent switched capacitance is determined by the driven loads. Since different I/O banks often operate at different voltages, their bypassing networks should be designed independently.[14]

Minimum size of each high-frequency V_{CCO} bybass-capacitor (C_{BI}) can be calculated with the formula:[14]

$$C_{BI} = \frac{S \times N_L \times C_L}{N_P}$$

where

S is the scale factor corresponding the variation in V_{CCO} (e.g. S=50 for 2% or 100 for 1% variation)

N_L is the number of outputs to be driven in an I/O bank (all I/Os)

C_L is the load on each output in farads

N_P is number of V_{CCO} pins in a bank

13.2.2 MIDDLE-FREQUENCY CAPACITORS

For every one to four V_{CCO} banks a middle-frequency capacitor of value 47 to 100µF should be present. Tantalum capacitor is preferred. If tantalum is not available, a low-inductance aluminium electrolytic type may be used.[14]

For example, when using all the eight banks of the XCV800, two to eight 47-100µF tantalums or aluminium electrolytic should be used.

13.2.3 LOW-FREQUENCY CAPACITORS

At least one 470µF to 3300µF low-frequency capacitor, should be used for each voltage level. One capacitor can be used for up to four devices.

13.3 Summary

The amount and size of the bypass capacitors depends various factors, for example the loading of the FPGA, as previously presented in this annex. Two following tables show example setup for the capacitors, when using Virtex FPGA up to XCV800.

BYPASS CAPACITORS FOR V_{CCINT}				
Size	**Amount**	**Preferred Type**	**Location**	**Purpose**
100nF	12	Ceramic SMD	As close to the V_{CCINT}/GND pins as possible	High Freguency Bypass
47-100µF	4	Tantalum or low-inductance aluminum electrolytic	Close to the V_{CCINT}/GND pins	Medium Frequency Bypass
470-3300µF	1		Anywhere on the board	Low Frequency Bypass

BYPASS CAPACITORS FOR V_{CCO}				
Size	**Amount**	**Preferred Type**	**Location**	**Purpose**
4nF	16	Ceramic SMD	As close to the V_{CCO}/GND pins as possible	High Freguency Bypass

47-100µF	2-8	Tantalum or low-inductance aluminum electrolytic	Close to the V_{CCO}/GND pins	Medium Frequency Bypass
470-3300µF	1		Anywhere on the board	Low Frequency Bypass