Software

More processing power - Driving requirements

- Autonomy
  - Task based commanding / resource management rather than timeline "remote control"
  - E.g. planetary rovers – drive from A → B, look out for interesting objects on the way (based on intelligent pattern recognition)
  - Going from fail-safe to fail-operational FDIR strategy.
- Vision based sensors & GNC for platform
  - Planetary rovers (Exomars)
  - Decent modules, landing site targeting,
- Science instruments (EOP) will generate 100++ times more data than can be downlinked.
  - Downlink of L1/L2-products instead of raw data
  - Focus will be on Near Real Time data.
  - Significant on-board processing increase required.
- Adaptive hardware
  - µ-controllers integrated with electromechanical systems
  - E.g. self-calibrating / Compensate for wear & tear
  - Software defined radio

More processing power - Driving requirements

- Autonomy
  - Task based commanding / resource management rather than timeline "remote control"
  - E… …cts o…
  - G…
- Visio…
  - F…
  - D…
- Scie… …han can …
  - D…
  - F…
  - S…
- Adap…
  - µ…
  - E…
  - Software defined radio

Processing power versus mission goals

- Current baseline is 2 x LEON-II
- Requirements
  - traversed distance shall reach science target up to 100 m within 1 SOL with better than 5 m accuracy.
- Current predicted performance
  - 70 m distance within 1 SOL with 10 m accuracy.
  - Path following accuracy is reduced due to limited visual odometry performance.
- Significant higher computing power / watts / € would greatly increase the science return.

General purpose computer – single or Multicore

- Software requirements on the hardware:
  - The Computer architecture and instruction set must be compatible with commercial processors
    - Allow to use commercial development tools as compilers, operating systems, design tools, code, automatic code generation
    - allow for functional test and validation on commercial computers (native compilation)
  - Linear addressing scheme
  - Pre-developed BSP, boot-up prom including self-test programs
  - Non-intrusive On-chip debugging capabilities
  - Allow heterogeneous applications share the same computer resource by providing application isolation capabilities. (MMU support – Time & Space Partitioning).

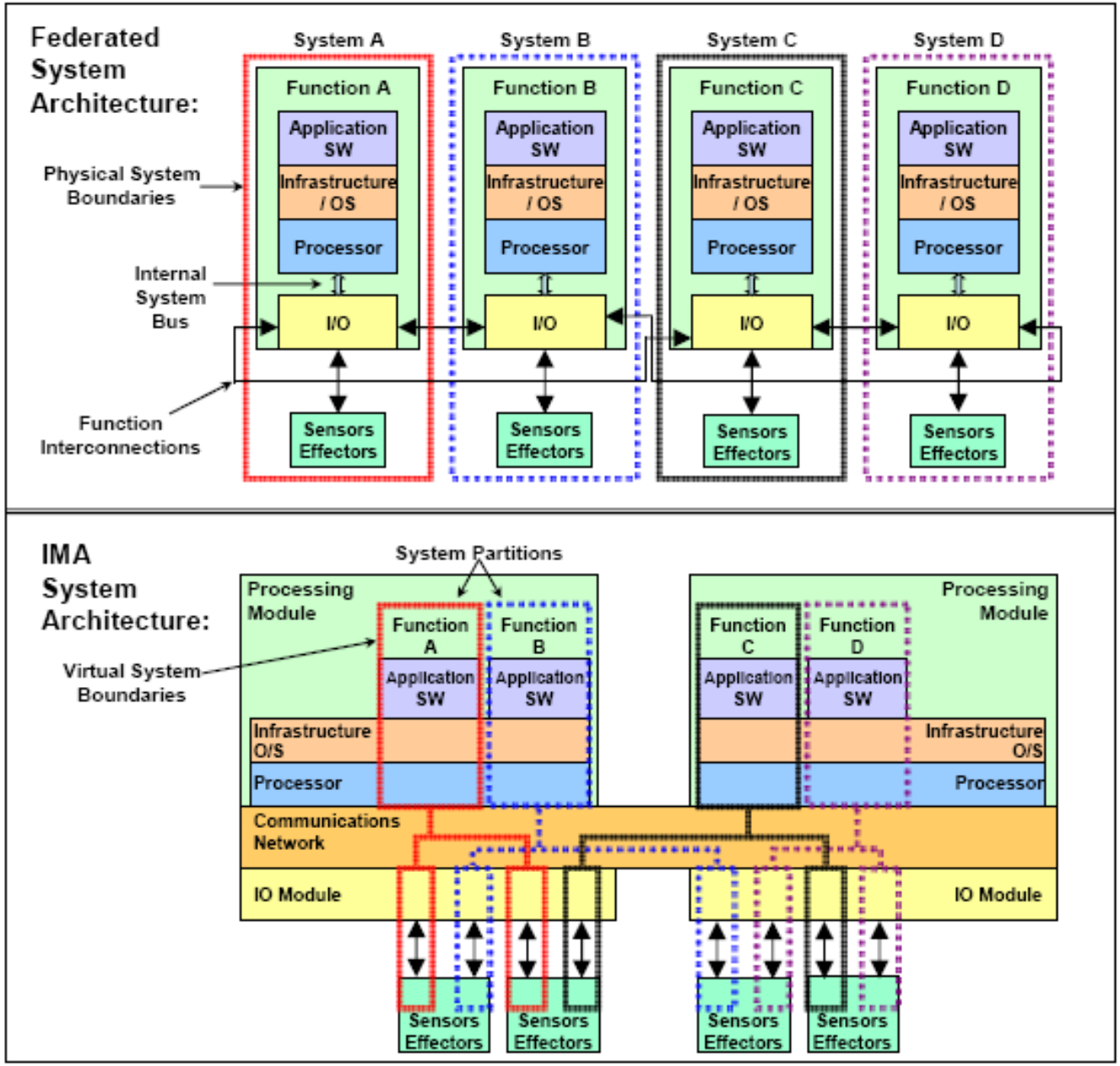
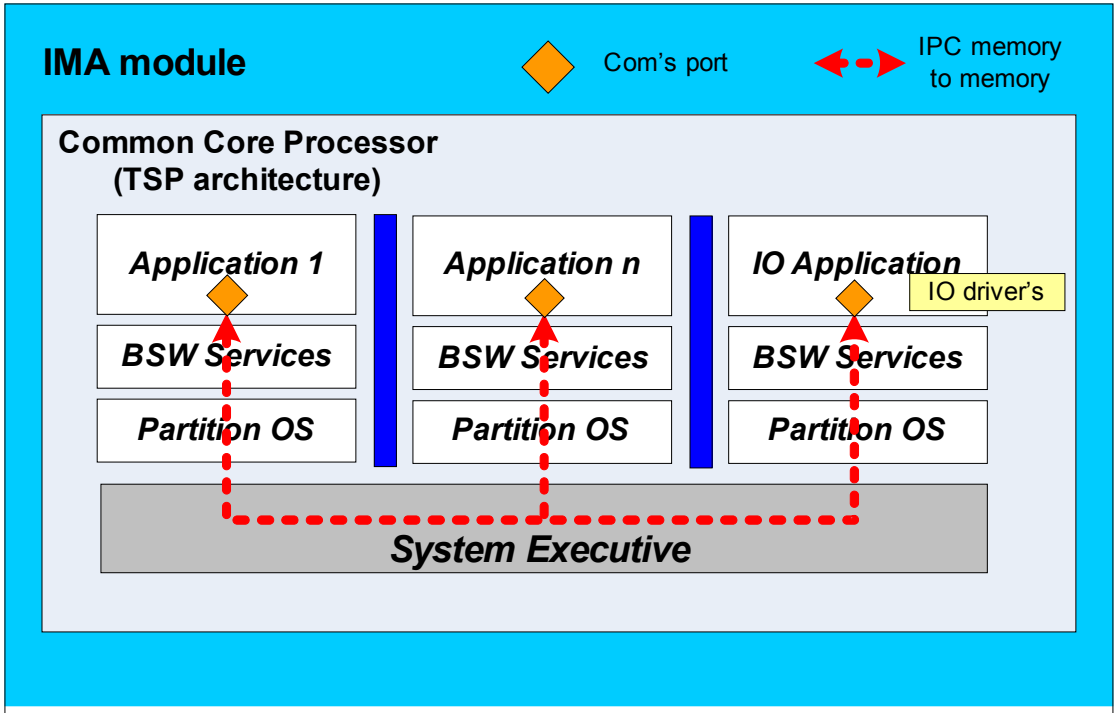


Figure 1. Compare Federated & IMA Architectures

Time & Space Partitioning Architecture



IPC through Memory to Memory transfer

What's happening now.

- System aspects of multi-core, The goal is
  - to investigate the various ways to use multicore for space based on spin-in from the non-space domain
    (symetric, asymetric, distributed OS, hypervisor, …)
  - to establish software driving requirement on multi-core design.
- HW-SW co-design
  - to go from avionics architecture towards implementation in software and/or in microelectronic technology
  - background is the Assert toolset extension towards microelectronic
- IMA for Space
  - Definition and prototyping of representative space application in a Time & Space software architecture.
- On-going studies in Securely Partitioning Spacecraft Computing Resources
  - Analyse and prototype the fundamental concept of securely separating a physical computer resource into multiple logical partitions for computer systems on-board a spacecraft.

µ-controllers

- High performance electromechanical systems.
  - Support multiple degrees of freedom
  - Coupling between axis's
  - Control frequencies 1KHz+
- Applications
  - High precision pointing mechanism 3-deg of freedom.
  - Thruster vector controllers for launchers (Vega, Ariane-5)
  - Micro vibration cancelling
  - Adaptive electromechanical systems (e.g. self calibrating systems)
  - etc
- Existing Space qualified µ-controllers cannot provide the required computing power for multiple coupled axis's of electromechanical actuators.

What happens elsewhere – an example.

- NASA is funding the Radiation Hardened by Design 49 core general purpose processor based on the Tilera TILE64™.
- Most properly ITAR protected.

Why Multi-core for Space?

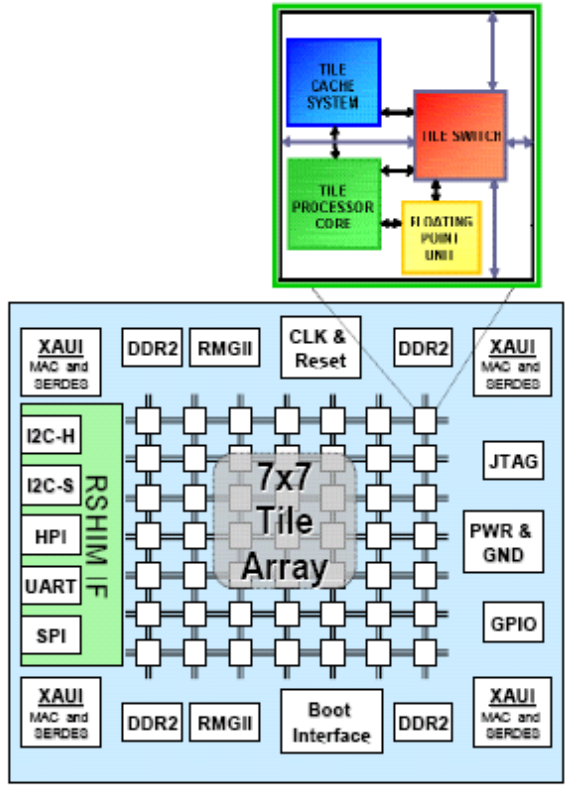
OPERA's Goal - Revolutionary Improvement in Processor Capabilities for Space Applications

- **Space processing challenges**
  - Advancing mission requirements
  - Shrinking decision timelines
  - Providing a common high-performance hardware and software technology foundation
- **OPERA is the Government's near-term low cost multi-core processor solution**
  - US Government owns the OPERA multi-core intellectual property
  - The OPERA program's Maestro chip provides processing leap-ahead capability for space applications
    - Breaks the paradigm of space electronics being a decade behind the commercial sector
    - Produces a radiation hardened state of the art general purpose processor
    - *100x more capable than current space qualified general purpose processors*

SRC: OPERA RHBD Multi-core; Michael Malone – Draper Laboratory; MAPLD – 31 August 2009

The Maestro Chip

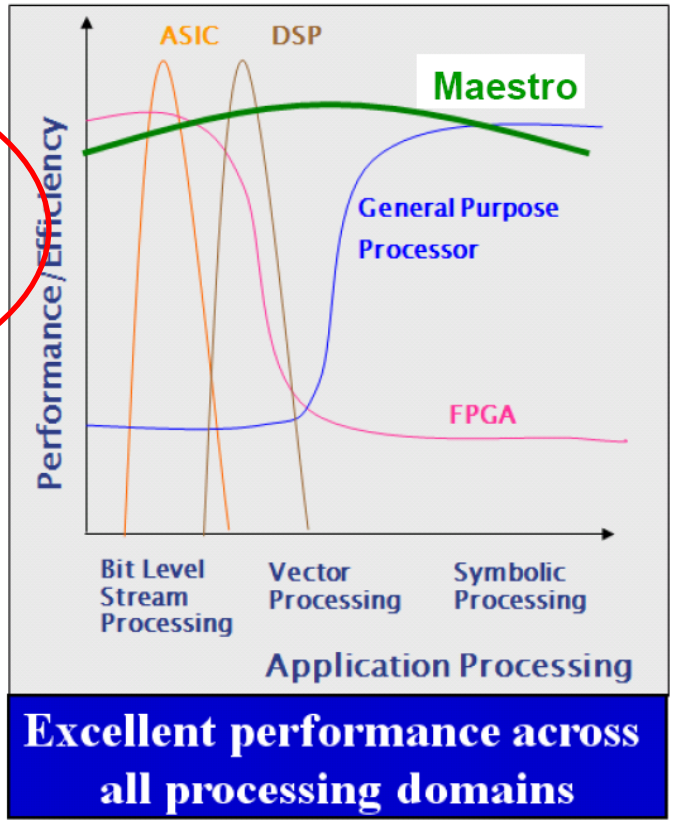
- **RHBD version of the Tilera TLR26480**
  - 7 x 7 core array
  - IBM 9SF 90 nm CMOS process
  - < 28 Watts Peak (selectable), 20 Watts typical (using 49 cores)
    - Can "nap" cores and reduce power
    - ~ 270 mW per core
  - Floating point unit in each processing core
    - IEEE 754 compliant, single and double precision
    - Aurora FPU IP
  - 500 Krad TID
  - Demonstrate NASA TRL-6 by December 2010
  - Software compatible with the Tilera TLR26480
    - Reduced number of cores, slower clock speed, added FPU
  - Tilera TLR26480 information can be found at www.tilera.com



SRC: OPERA RHBD Multi-core; Michael Malone – Draper Laboratory; MAPLD – 31 August 2009

OPERA Components

- **Hardware – Maestro Chip**
  - 49 core general purpose multi-core processor
  - 45 GOPS at 310 MHz
    - 22 GFLOPS (theoretical) at 310 MHz
    - Clock speed limited by memory
  - Four - 10 Gbps SERDES XAUI interfaces
  - Radiation Hard By Design (RHBD)
  - Developed by Boeing SSED
    - Uses Tilera Corporation IP
    - Additional third party IP
- **Software**
  - Basic compiler tools
    - Complements Tilera's toolset
  - Benchmark code
  - Performance and productivity tools
    - Parallel libraries, analyzer, debugger, run time monitor, OS ports



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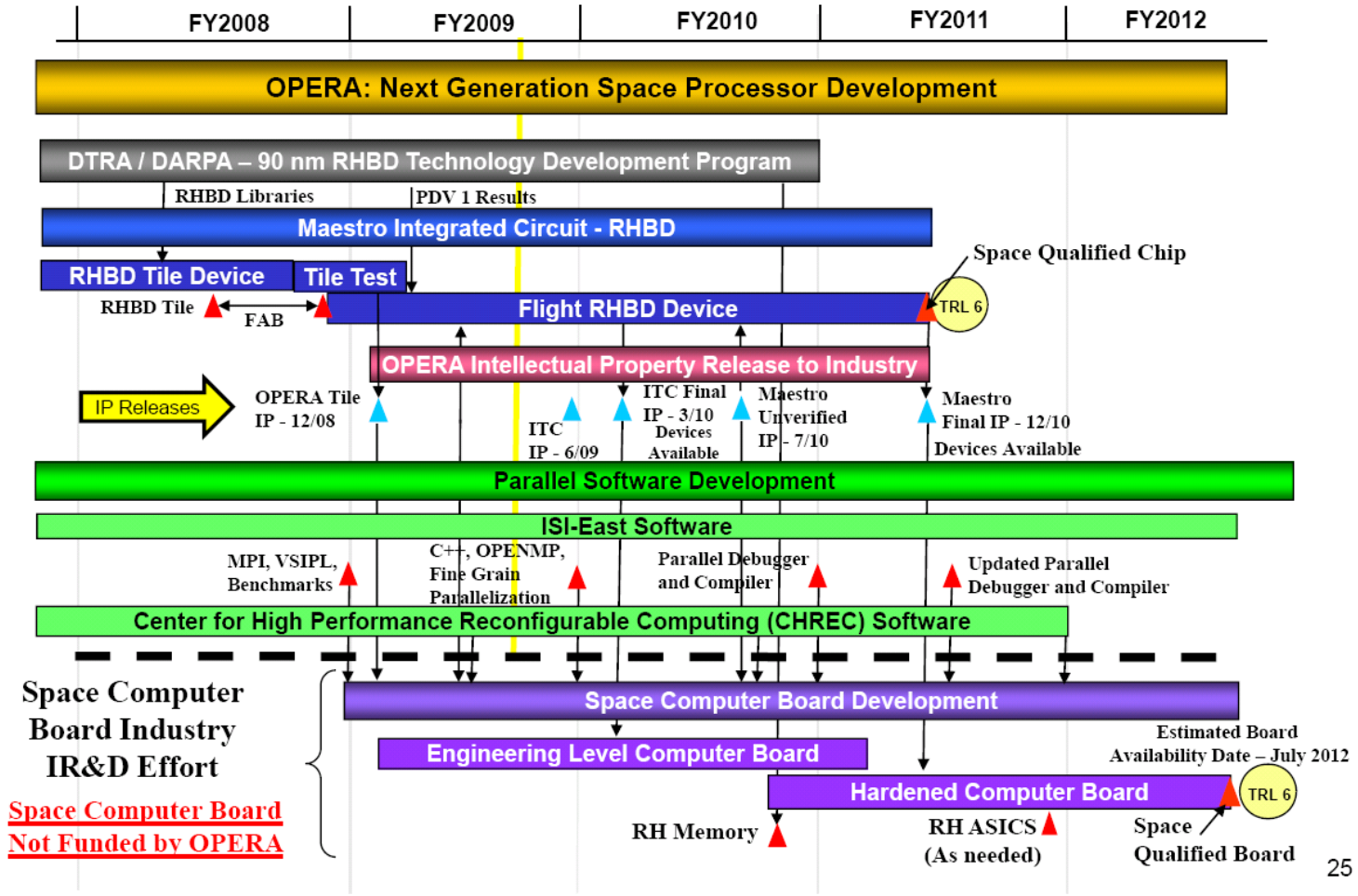
OPERA Program Roadmap



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