

# Spacecraft Controller On-a Chip with LEON3-FT (SCOC3)

## AUTHOR

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## INTRODUCTION

After two design studies implemented on reprogrammable FPGA, SCOC1 [1] [2] [3] and SCOC2, using LEON1 and LEON2 respectively, SCOC3 is a System-On-Chip for Spacecraft Control and Data Handling, featuring the LEON3-FT processor with GRFPU-FT, TM/TC interfaces, various on-board interfaces (RMAP Spacewire, CAN, 1553, UART), time management and event routing. Internal communication is distributed over a double AMBA-AHB bus structure with separate external memory ports, and the two buses are linked by inter-bus bridges.

SCOC3 was developed by EADS ASTRIUM under ESA contract supported by CNES and by EADS ASTRIUM internal funding.

## ARCHITECTURE

The block diagram of the SCOC3 is shown in Figure 1. There are three main areas of the chip:

1. The processor subsystem (top-right, blue) contains the LEON3-FT processor with GRFPU-FT and related peripherals: a memory controller, UART and Spacewire interfaces for debug purposes and inter-processor communication tasks, communicating via the CPU-AHB bus.
2. The on-board I/O subsystem (bottom right, yellow), which provides various I/O interfaces (UART, CAN, SpW, MIL1553 BC/RT). The interfaces and the TM/TC part exchange data via a separate IO AHB bus. Data exchanges are essentially of DMA type, the only AHB slave (besides the APB bridges for status, configuration and low data rate interfaces) is the IO memory controller.
3. The TM/TC subsystem (top-left and left, green) provides one packet telemetry encoder (PTME) and one telecommand decoder (TCDD) unit, with MAP interface and all external pins necessary to build a redundant, cross-strapped system. A Housekeeping function (HKPF) allows automatic generation of housekeeping telemetry.

The performance offered by a single on-chip bus in a system with processor and extensive IO traffic does not fulfil the requirements for latency and throughput. Backbone of on-chip data transfer is therefore a system of two cross-coupled AHB buses (CPU AHB and IO AHB). This concept also leads to a reduced number of bus agents on each bus and therefore improves timing (maximum clock frequency), and it allows operating both buses (and the subsystems attached to them) at a different clock frequency. The CPU AHB bus can be operated at an integer (1, 2) multiple of the IO AHB clock, allowing the optimisation and trade-off of performance versus power consumption depending on the application requirements. Any master on the CPU AHB Bus can access to the APB busses as Master through the APB Master interfaces. It is then possible to control the SCOC3 through the UART DSU interface for example. The hardware management of registers is split in three APB busses in order to separate different main functionalities such as processing, peripherals and TM/TC.

One of the main key points of SCOC3 is the integration of complete CCSDS TM and TC protocols and interfaces.

The TCDD (Packet Telecommand Decoder) is an improvement of the TC IP already implemented in SCOC1. This TC IP was based on the PTD ASIC MA28140. Work at segment layer level has been done in order to change MAP interfaces for CPDU, deciphering or cross-strapping purposes. All the four status registers FAR, CLCW, AUS, CPDUS can be read and written through APB. A local memory has been implemented in order to deal with authentication. This memory is scrubbed and protected by EDAC.

The STME (SCOC3 Packet Telemetry Encoder) provides all the functionalities of the ground telemetry system, integrating the PTME IP from ESA. The functionalities have been wrapped into a single module including an internal memory buffer.

## DEVELOPMENT STATUS

SCOC3 was manufactured by ATMEL. Prototypes were received in May 2009 and soldered on KerObs board as shown on Figure 2.

After a very thorough and huge hardware, software and system validation, the prototype approval was signed on 27 October 2009 confirming that the first ASIC run was the successful run

SCOC3 chipset is fully characterised and ready for EADS ASTRIUM projects (ASTROTERRA, SEOSAT computers) and also for any platform computers projects.

The SCOC3 ASIC is embedded on Ceramic Land Grid Array 472 ATMEL package (hermetic package with no columns). This CLGA will be assembled either with NTK LCI interposer (current ATMEL catalogue package), or with Six Sigma columns (available alternative already qualified at Astrium in a previous development).

## FOLLOW-UP ACTIVITIES

Subject to signature of a new ESA contract, SCOC3 will be established as an Application Specific Standard Product [4] available to all users in the ESA member and participating states, and the following SW tool roadmap will be developed:

- A hardware software interface layer which is independent of the real time operating system.
- A board support package adapted to operating system RTEMS
- Driver software functions which allow the use of main input output peripherals.
- Interface test applications which will be delivered with the provided board.
- A software environment development and RTEMS operating system associated tools.

A development environment for SCOC3 will be provided to standardize the code production tools. The main part of the environment integrates the tools used for the development of flight software (C compiler and RTEMS OS). The environment will be specially designed in order to avoid the use of tools which are under commercial license.

SCOC3 chipset may be sold with a SCOC3 simulator under licensing for customer requiring software development in parallel with a board.

## CONCLUSION

EADS ASTRIUM has designed, manufactured and tested a high performance new computer product based on SCOC3 chipset: Identified applications are both observation satellites with class 2 EEE quality level (ASTROTERRA, SEOSAT ...) or with class 1 EEE parts (Geostationary Telecom)

The first Prototype Flight Models of the SCOC3 on-board computer will be delivered by end 2010.

## CONTACTS

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## REFERENCES

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SCOC1 block diagram
- [2] Tests and Development results of a System-on-a-Chip for Satellite Data Handling, Marc Souyri, Marc Lefebvre, Roland Weigand, DASIA 2003
- [3] <http://conferences.esa.int/03C20/s1a-01.pdf> SCOC - A Spacecraft Controller On-a-Chip, R. Weigand, M. Souyri, M. Lefebvre, Workshop on Spacecraft Data Systems (SDS) 2003
- [4] [http://en.wikipedia.org/wiki/Application\\_specific\\_standard\\_product](http://en.wikipedia.org/wiki/Application_specific_standard_product)  
Definition of Application Specific Standard Product (ASSP)

Figure 1: Block diagram of SCOC3

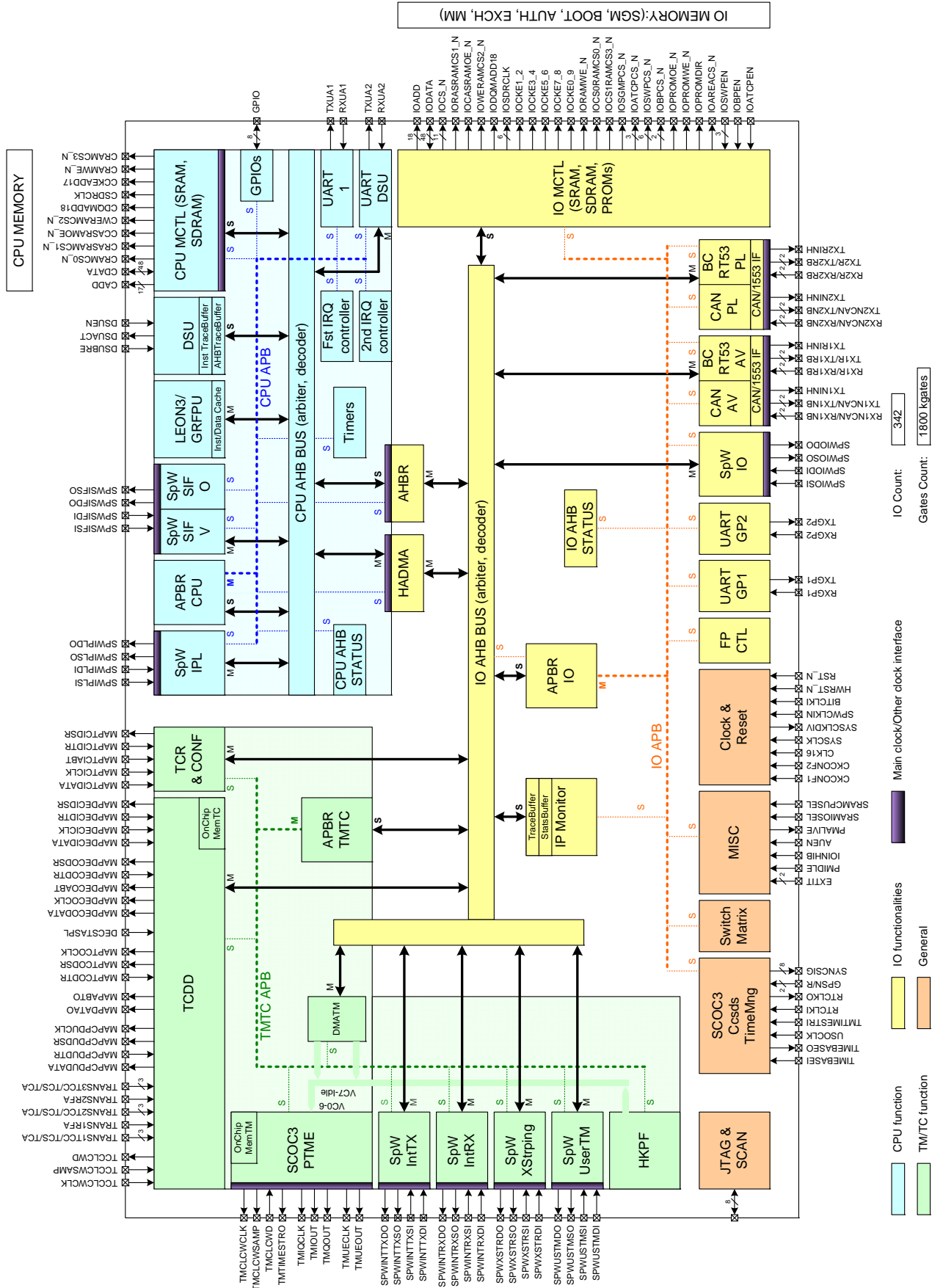


Figure 2: SCOC3 on KerObs board

