ESTEC

Spacecraft Controller On a Chip with LEON3-FT (SCOC3)

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Agenda

- **SCOC1 to SCOC3**
- **SCOC3 architecture brief presentation**
- **Development status**
- **Follow-up activities**
- **Conclusion**

SCOC3 heritage

- **EADS ASTRIUM has been working on SoC for the last ten years:**
  - SCOC3 has an heritage based on SCOC1 which was a study made with ESA funding.
  - SCOC3 benefits also of SCOC2 which was an internal EADS ASTRIUM study to continue the previous one.

- These studies showed several key points like internal bus arbitration, I/O interfaces traffic and memory bandwidth.

- **SCOC3 was developed by EADS ASTRIUM under ESA contract supported by CNES and by EADS ASTRIUM internal funding.**

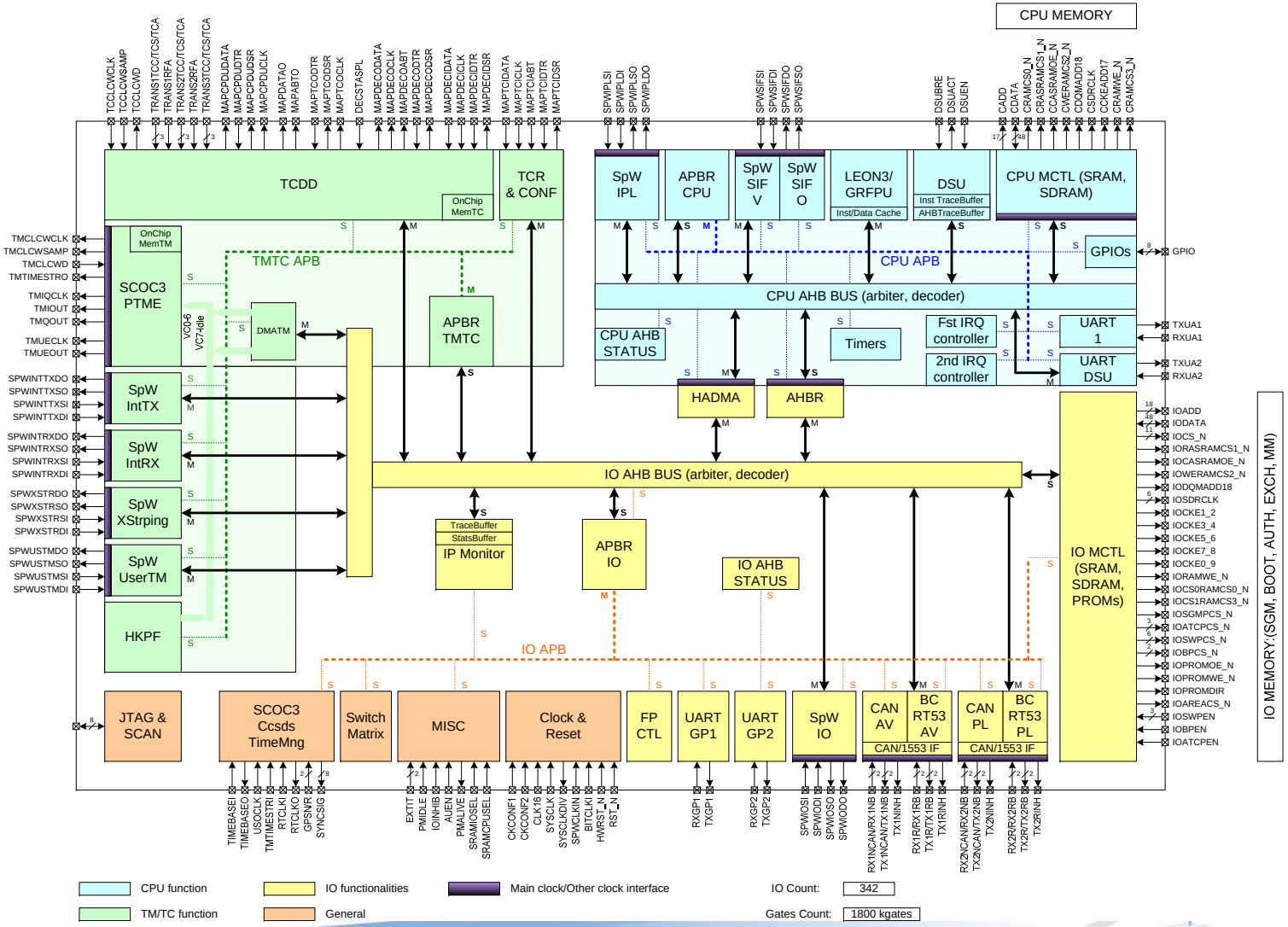
Some SCOC3 features

- SCOC3 is a System-On-Chip for Spacecraft Control and Data Handling, featuring:
  - The LEON3-FT processor with GRFPU-FT,
  - CCSDS TM/TC interfaces,
  - Various on-board interfaces (RMAP Spacewire, CAN, 1553, UART),
  - Time management and Event routing.

- Internal communication is distributed over a double AMBA-AHB buses structure with separate external IO and processor memory ports. The two buses are linked by inter-bus bridges.

- **SCOC3 integrates functions which were before on several ASICs. It is very attractive : small size in a qualified BGA package, low power consumption and rad-tolerant technology.**

SCOC3 architecture



A dual AHB bus architecture

- Latency and data throughput performances on-chip data transfer are achieved with a system of two cross-coupled AHB buses (CPU AHB and IO AHB) =>
  - Reduced number of bus agents on each bus,
  - Improves timing (maximum clock frequency),
  - Allows operating both buses at a different clock frequency,
  - Dual external IO and processor memory ports to keep maximum performance of the processor

- Any master on the CPU AHB bus can access to the APB busses as Master. It is then possible to control the SCOC3 through the UART DSU interface.

TM/TC interfaces integration

- **One of the main key points of SCOC3 is the integration of the complete CCSDS TM and TC protocols and interfaces.**

- TCDD (Packet Telecommand Decoder)
  - Provides all functionalities of the TC system
  - A local memory permits to deal with authentication

- STME (SCOC3 Packet Telemetry Encoder)
  - Provides all functionalities of the ground telemetry system (PTME),
  - The functionalities have been wrapped into a single module including an internal memory buffer.

- **SCOC3 may work as a powerful processor with the most needed peripherals including CCSDS TM/TC or as a whole CCSDS TM/TC chip.**

Development status and commercialisation

- Status:
  - SCOC3 is manufactured by ATMEL. Prototypes were received in May 2009.
  - After a very thorough and important hardware, software and system validation, the prototype approval was signed on 27 October 2009 confirming that the first ASIC run was the successful run
  - SCOC3 chipset is fully characterised and ready in due course for EADS ASTRIUM projects (ASTROTERRA, SEOSAT computers) and also for any platform computers projects.

- Commercialisation:
  - SCOC3 chipset will soon be commercially released.

Choice of package

- The SCOC3 ASIC is proposed as baseline with current ATMEL CCGA472 package, built with NTK interposer (SCI)
- Two quality flow are proposed : QML Q & QML V

- As an alternative to the SCI NTK interposer used with current ATMEL CCGA package, the SCOC3 could be also procured at LGA package
  - Hermetic package delivered with no column
  - Same quality level available : QML Q or QML V

- This alternative is under analysis at ASTRIUM, and would allow to assemble LGA with different columns as NTK ones.

SCOC3 gate level characteristics

- SCOC3 matrix: ATC18RHA95_504D (pad limited choice)
- Matrix size: 13x13=169 mm²
- **Chip size area in the matrix (pads, logic, hard blocks): 57.7 mm²**
- Number of logic gates: 1.8 Mgates
- Number of DFFs: 55000
- Number of memory bits: 2.2 Mbits equivalent to 1.8 Mgates

Follow up activities (1)

- **Subject to signature of a new ESA contract, SCOC3 will be established as an Application Specific Standard Product available to all users in the ESA member and participating states, and the following SW tool roadmap will be developed.**

- The software activity will consist in developing:
  - A hardware software interface layer which is independent of the real time operating system.
  - A board support package adapted to operating system RTEMS
  - Driver software functions which allow the use of main input output peripherals.
  - Interface test applications which will be delivered with the provided board.
  - A software environment development and RTEMS operating system associated tools.

Follow up activities (2)

- A development environment for SCOC3 will be provided to standardize the code production tools.
- The main part of the environment integrates the tools used for the development of flight software (C compiler and RTEMS OS).
- **SCOC3 technical support definition will also be addressed in these follow up activities.**
- **It will be necessary to perform radiation tests according to a Radiation test plan which is being prepared.**

Customer complementary needs opportunities

- SCOC3 chipset may be sold with a SCOC3 simulator under licensing for customer requiring software development in parallel with a board.

- Although negotiation is running, a low cost starter kit based on SCOC3 implementation in a XILINX should be available for software and systems developments. This starter kit will be funded by CNES.

- Current developed software run under RTEMS OS.
  Other OS might be available depending on funding and needs:
  - eCos
  - VxWorks up to 6.5
  - Linux, ThreadX, Nucleus…

Conclusion

- **EADS ASTRIUM has designed, manufactured and tested a high performance new computer product based on SCOC3 chipset:**
  - Identified applications are both observation satellites with class 2 EEE quality level (ASTROTERRA, SEOSAT, …) or with class 1 EEE parts (Geostationary Telecom)

- **The first Prototype Flight Models of the SCOC3 on-board computer will be delivered by end 2010.**