RUAG Space
Microprocessors in present and future equipment

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Products

Spacecraft Management Units

Guidance and Control Computers

Payload processing and control

Radio occultation instruments
SMU Technical Concept

- CPDU commands
- HPTM
- EGSE I/F
- SMU core
- TM/TC/RM/MM board
- Processor board
- External buses and links
- I/O bus
- I/O board
- Alarms
- External buses and links
- TC
- TM
- Alarms
- TM/TC/RM/MM board
- Alarms
- TM
- TC
- CPDU commands
- HPTM
- EGSE I/F
Current generation processor boards

- Based on TSC695 including:
  - COCOS ASIC
  - Ext. interfaces: 2x1553, 2xSpaceWire/UART, 2xPacketWire, Sync, EGSE
  - Int. interfaces: 1553, OBDH, 4xSpaceWire, 2xPacketWire Sync, Alarms

- Based on COLE ASIC including:
  - 1,8V DC/DC converter
  - Ext. interfaces: 2x1553, 2xSpaceWire, 2xUART, 2xCAN, Sync, EGSE
  - Int. interfaces: 1553, OBDH, 5xSpaceWire, 2xPacketWire Sync, Alarms
COCOS, CPU Companion and I/O ASIC

- CPU Interface
- Memory Interface
- Interrupt Controller
- Watchdog
- Alarms
- Memory Copy Controller
- On Board Time (OBT)

- 3 MIL-STD-1553B
- 1 to 3 UARTs (pins shared with SpaceWire)
- PCI bus
- 3 Packet Wire Receiver (PWR)
- 3 Packet Wire Transmitter (PWT)
- 3 to 6 SpaceWire (pins shared with UARTs)
COLE chip

Integration of:
- "LEON" SPARC v. 8 processor
- COCOS I/O controller

Major improvements:
- Processing Performance
- I/O Speed and Functionality (MMU, enhanced DSU, SpaceWire RMAP)
- CAN bus I/O
- Cost
Next generation computers

- >10 years design lifetime
- Higher performance, i.e. multi-core CPU needed
- Flexible architecture to handle future requirement changes
- New standards impose upgrade of IP blocks and software
- New interfaces such as sensor buses and wireless
- Built-in GPS receiver
- Star Tracker processing in the main computer
- Time and Space Partitioning support
Next generation computer architecture

- Processor technology evolves faster than system architecture
- Separate application processor from system application chip

- Fast bus slave I/F available as IP
- No need for advanced memory I/F on the CPU
- Backwards compatibility for I/O interfaces to reduce software development effort

**Diagram:**
- NVM
- Application specific memory
- CPU including RAM
- Bus I/F
- Application specific support chip
- Host computer(s)
- I/O interfaces: SpaceWire, 1553, CAN, SpaceFibre, WLAN
CPU architecture considerations (from 2006 microprocessor RT)

- Performance by extrapolation:
- Are European foundries competitive?
- Does the SPARC architecture give sufficient performance?
- Anything else we can do better in Europe?
- Do we have the resources to participate in the performance race?
- What will be the consequences if we do not participate?