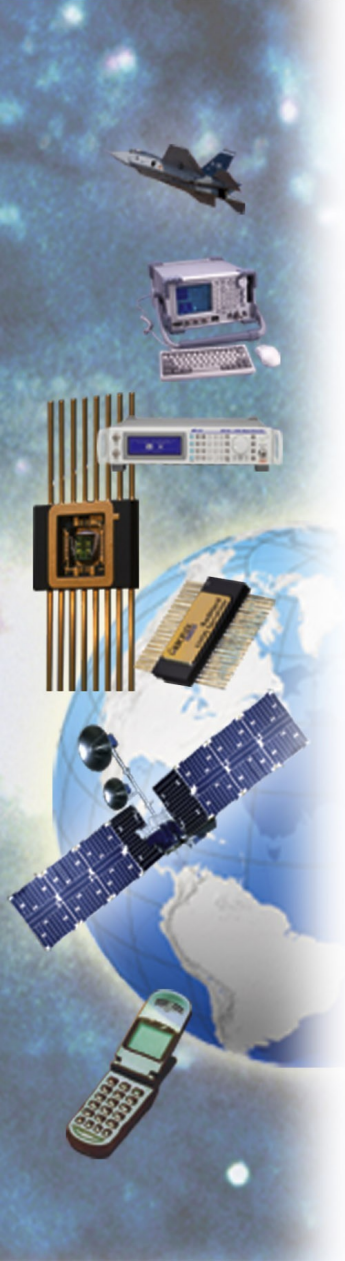


Next Generation Multi-Purpose Microprocessor

Presentation at MPSA, 4th of November 2009

www.aeroflex.com/gaisler



OUTLINE

- NGMP key requirements
- Development schedule
- Architectural Overview
- LEON4FT features and performance
- Software support
- Summary

NGMP Key Requirements

- SPARC V8 based multi-core architecture
- Average performance of 400 MOPS on GINA benchmarks
- Minimum of 200 MOPS on any single GINA benchmark
- SPARC compliant Memory Management Unit
- Improved debug support with respect to LEON2FT
- On-chip memory \geq 32 Mbyte
- On-chip interfaces (e.g. HSSL, SpW, PCI)
- Interface for scalable multi-processor architectures, co-processors and/or companion devices
- Maximum power consumption: 6W. Idle power 100 mW.

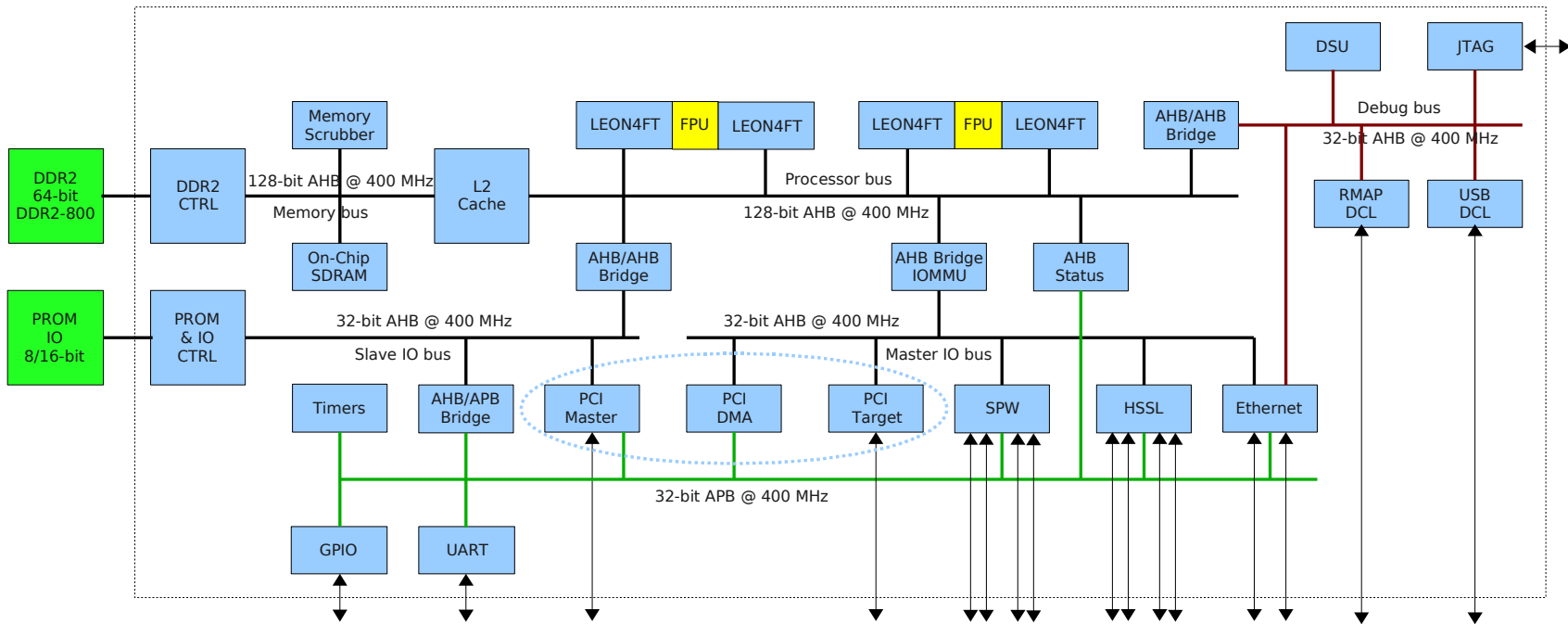
Development Schedule

- Aug 2009: Kick-off
- Feb 2010: Definition and specification
- Dec 2010: Final RTL code, FPGA Demonstrator
- Aug 2011: Verified ASIC netlist
- Manufacturing of prototype parts not yet decided
- Development of flight model in a separate contract

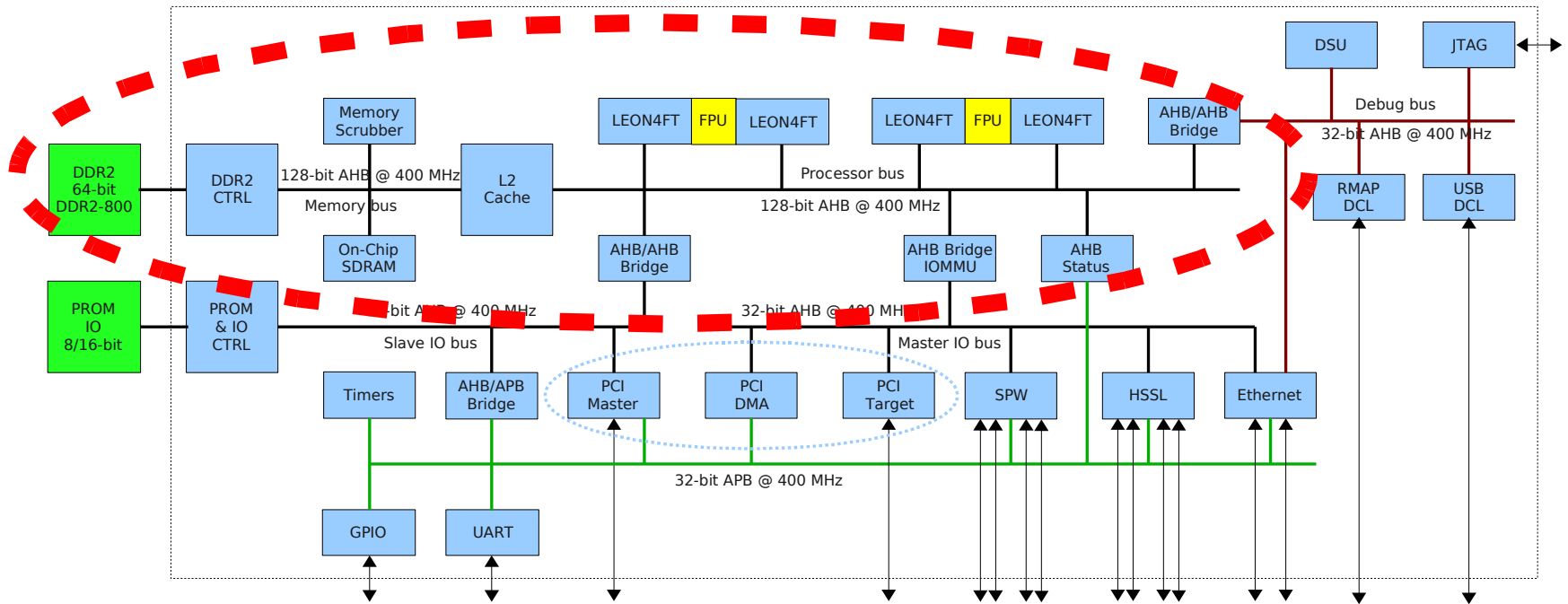
Current NGMP Definition

- Quad-core LEON4FT with two GRFPU
- 128-bit L1 caches, 128-bit AHB bus
- 2-8 Mbyte L2 cache, 256-bit, 4-way LRU
- 64-bit DDR2-800 Memory interface
- 32 Mbyte on-chip DRAM (if feasible)
- 4x GRSPW2 Spacewire cores @ 250 Mbit/s
- 32-bit, 66 MHz PCI interface
- 2x 10/100/1000 Mbit Ethernet
- Optional 2x HSSL

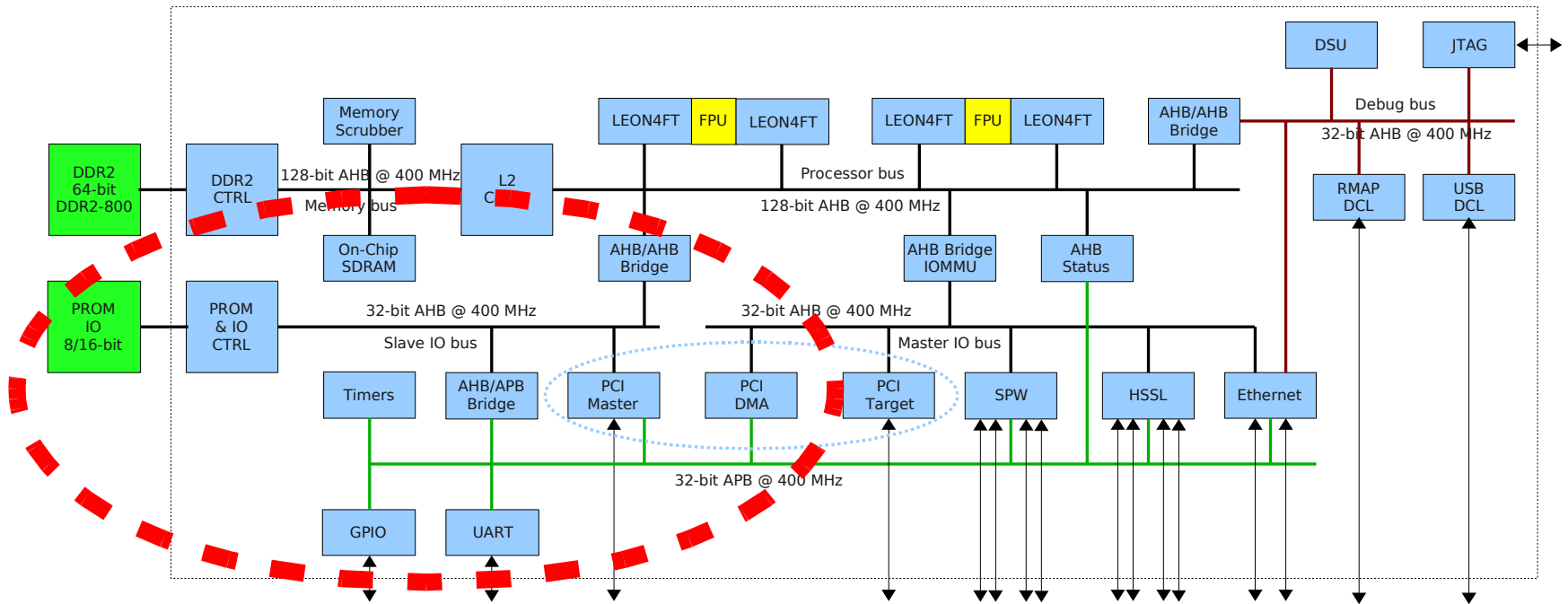
Architectural Overview



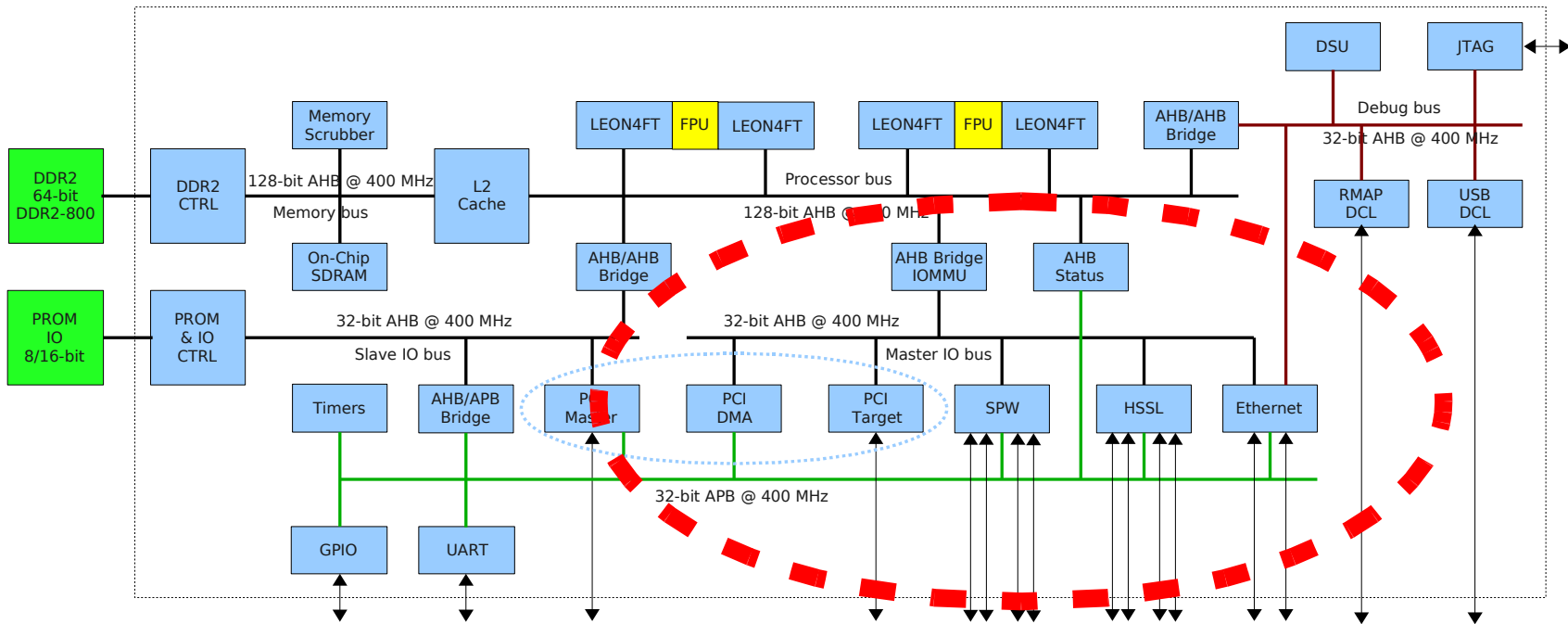
Processor and Memory bus



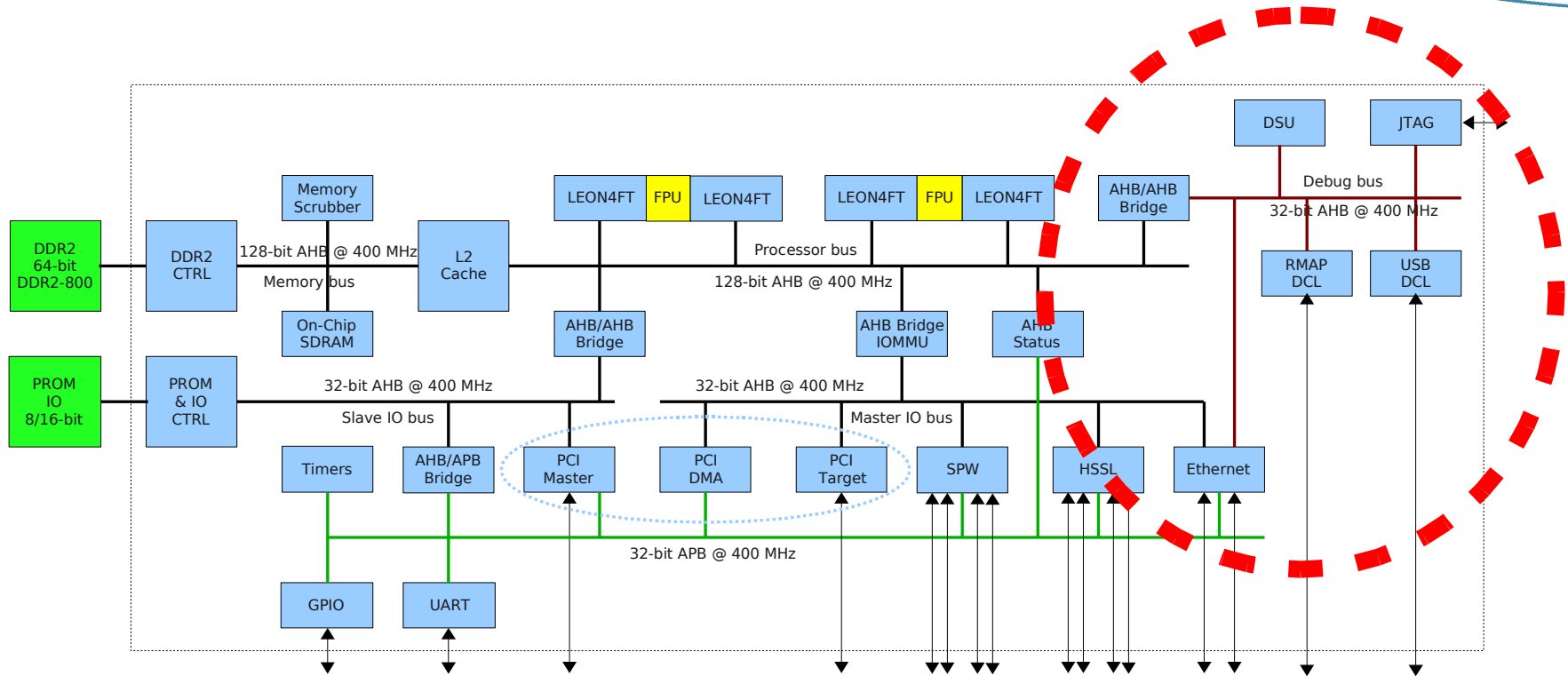
Slave I/O bus



Master I/O bus with I/O MMU



Debug bus with EDCL connection



LEON4FT Overview

- SPARC V8 compatible core
- 64-bit 4-port register file
- 64-bit single-clock load/store operation
- Branch prediction
- Extended store buffer
- Support for block move
- 64- or 128-bit AHB bus interface
- Performance counters
- Local timer and interrupt controller
- 1.7 Dhrystone MIPS/MHz, 0.6 Wheatstone MFLOPS/MHz
- 0.35 SPECINT/MHz, 0.25 SPECFP/MHz

L2 Cache

- L2 cache configurable with 1 - 4 ways, any size
- 256-bit internal cache line with 64-bit BCH ECC
- Copy-back and write-through operation
- 0-waitstate pipelined write, 3-waitstates read hit
- Essential for SMP performance scaling
- Reduces effects of slower memory (SDRAM) if DDR2 cannot be used

DDR2 controller

- DDR2-800 interface with 8-word read/write FIFO
- 64-bit data with 16 or 32 bit reed-solomon ECC
- Corrects two or four independent 4-bit errors
- Hardware scrubber and SEFI re-generator
- Dual-channel possible if enough pins in package

The NGMP will have improved debugging support compared to the LEON2FT and many existing LEON3 implementations. The new features include:

- Several high-speed debug interfaces
- Non-intrusive debugging through dedicated Debug bus
- AHB trace buffer with filtering
- Instruction trace buffer with filtering
- Hardware data watchpoints
- Data area monitoring

Improved Profiling Support

The NGMP has improved profiling support compared to the LEON2FT and LEON3. The new features allow to measure the following metrics:

- Processor performance and L1 cache hit rate
- AHB utilization
- L2 cache hit rate

Software Support



- NGMP is instruction compatible with LEON2/3
- Any compiler producing SPARC V8 code can be used
- GRMON debug monitor will be extended to support all new features
- Supported operating systems: RTEMS-4.10, eCos-2.0, Linux-2.6.29, VxWorks-6.7, LynxOS, ThreadX, Nucleus
- BSPs and drivers will be developed for RTEMS and VxWorks where necessary

The presented design is preliminary. Choices that are still open include:

- 2 or 4 CPU cores, shared or individual FPUs
- L1/L2 cache size, cache locking
- On-chip RAM size and type
- I/O MMU implementation
- High-speed interfaces
- External memory type

NGMP Commercialisation

It is the intent of Aeroflex Gaisler to make the NGMP available and supported as an Application Specific Standard Product (ASSP).

Aeroflex Gaisler is fully committed to perform the further development work to commercialize flight models (FM) and also to ensure that related technical support is provided over an FM product lifetime or at least eight years. The NGMP will be provided under fair and equal conditions to users in the ESA members and participating states.

Some of the key characteristics of the NGMP are:

- LEON4FT providing 1.7 DMIPS/MHz
- NGMP target frequency is 400 MHz
- Improved AMBA AHB bus bandwidth compared to LEON2/LEON3 systems
- Improved support for debugging and profiling
- Multiple AHB buses to partition the design
- L2 cache
- DDR2 memory with Reed-Solomon protection
- High-Speed Serial Links
- Immediate availability of a wide range of software

Questions?