ATMEL MICROPROCESSORS PRODUCTS FAMILY

Session 3: New Development & Investigation Areas

Presentation

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ABSTRACT

This paper presents the Magic DSP® IP available at ATMEL for future space applications.

Magic DSP is a high performance VLIW DSP delivering 1 Giga floating-point operations per second (GFLOPS) and 1.6 GOPS at a clock rate of 100 MHz. It is equipped with an AHB master port and an AHB slave port for system-on-chip integration. It has 256 data registers, 64 address registers, 10 independent arithmetic operating units, 2 independent address generation units and a DMA engine.

To sustain the internal parallelism, the data bandwidth among the Register File, the Operators and the Data Memory System, is 80 bytes/cycle. The Data Memory System is designed to transfer 28 bytes/cycle. This allows the Magic DSP to produce one complete FFT butterfly per cycle by activating all the computing units.

Magic DSP operates on IEEE 754 40-bit extended precision floating-point and 32-bit integer numeric format for numerical computations, while internal memory accesses are supported by a powerful 16-bit MAGU (Multiple Address Generation Unit). It has also on-chip 16K x 40-bit 6-access/cycle data memory system and 8K x 128-bit dual port program memory locations. Efficient usage of the internal program memory is achieved through a general purpose code compression mechanism and software pipelining support of systematic loops.

A C-oriented architecture and an optimizing assembler ease the user from the burden of dealing with the parallelism of the processor resources and significantly simplifies the code development. A rich library of C-callable DSP routines is available.

The presentation will cover the technical characteristics of the Magic DSP IP, its main features and performances. Some benchmarks obtained on typical DSP algorithms are reported. In the last part of the presentation, the tools already available for this IP are shown, the C Compiler and the Hardware Debugger, and the available libraries as well.