Magic DSP™

AGENDA

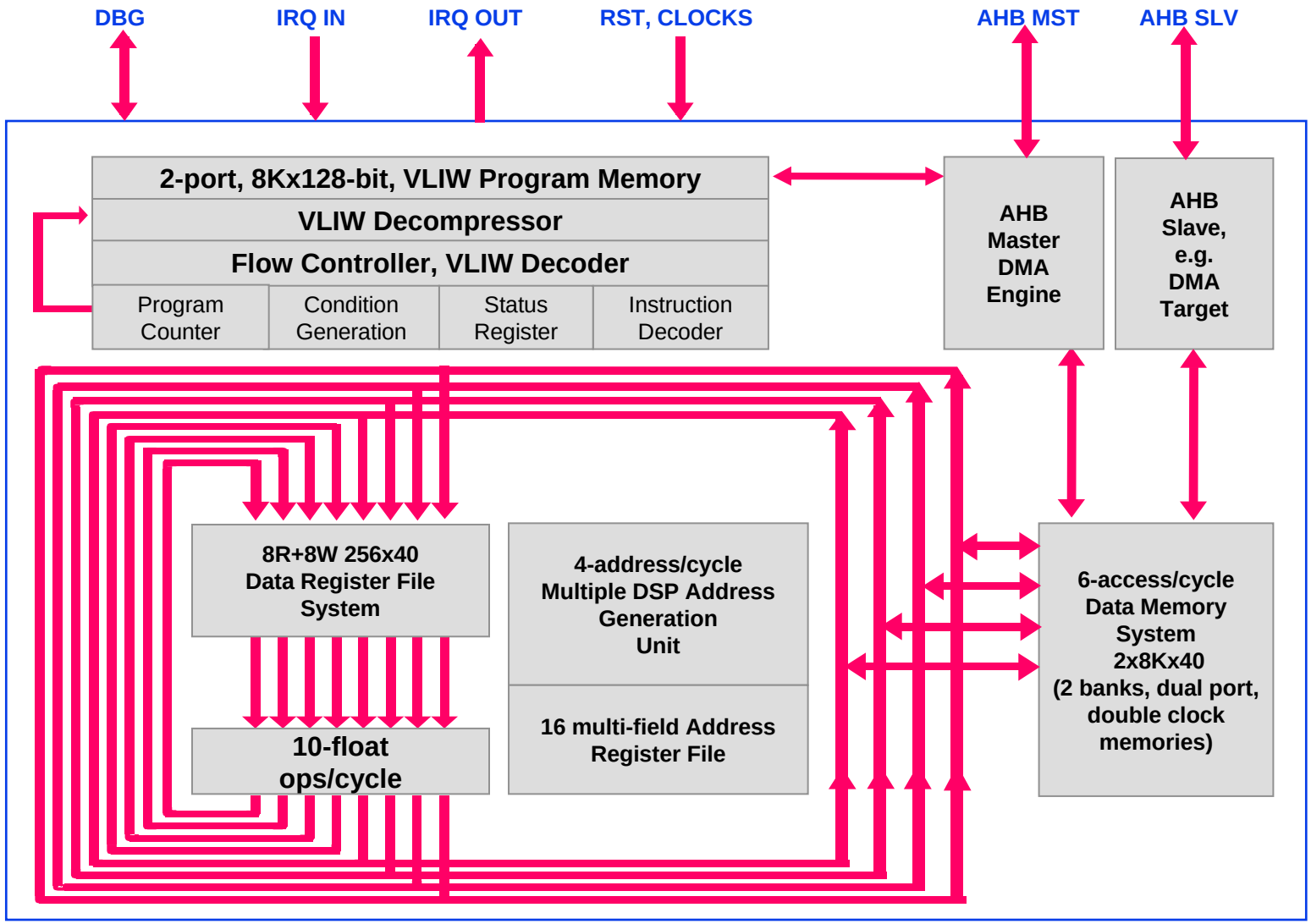
- Magic DSP features
- Magic DSP benchmark
- Programming tools

Magic DSP™ features

Magic DSP features

- C programmable VLIW DSP
- Floating point 32 / 40 bit
- Up to 10 floating point operations per cycle
  - 1GFLOPS @ 100MHz in 130nm (available)
  - 2GFLOPS @ 200MHz in 90nm (P&R estimate)
  - 2.75GFLOPS @ 275MHz in 65nm (P&R estimate)
- 2 address generation units, 4 memory accesses per cycle
- 6 port memory system allowing concurrent computation and data move
- Float – vector – complex native data type support
- Program Memory Management Unit (PMU). PM cache
- DMA engine supporting stridden memory accesses
- AMBA AHB master and slave bus interface
- Low power: 0.17 mW/MFLOPS mAgic (0.36 mW / MIPS ARM)

mAgicV IP Architecture



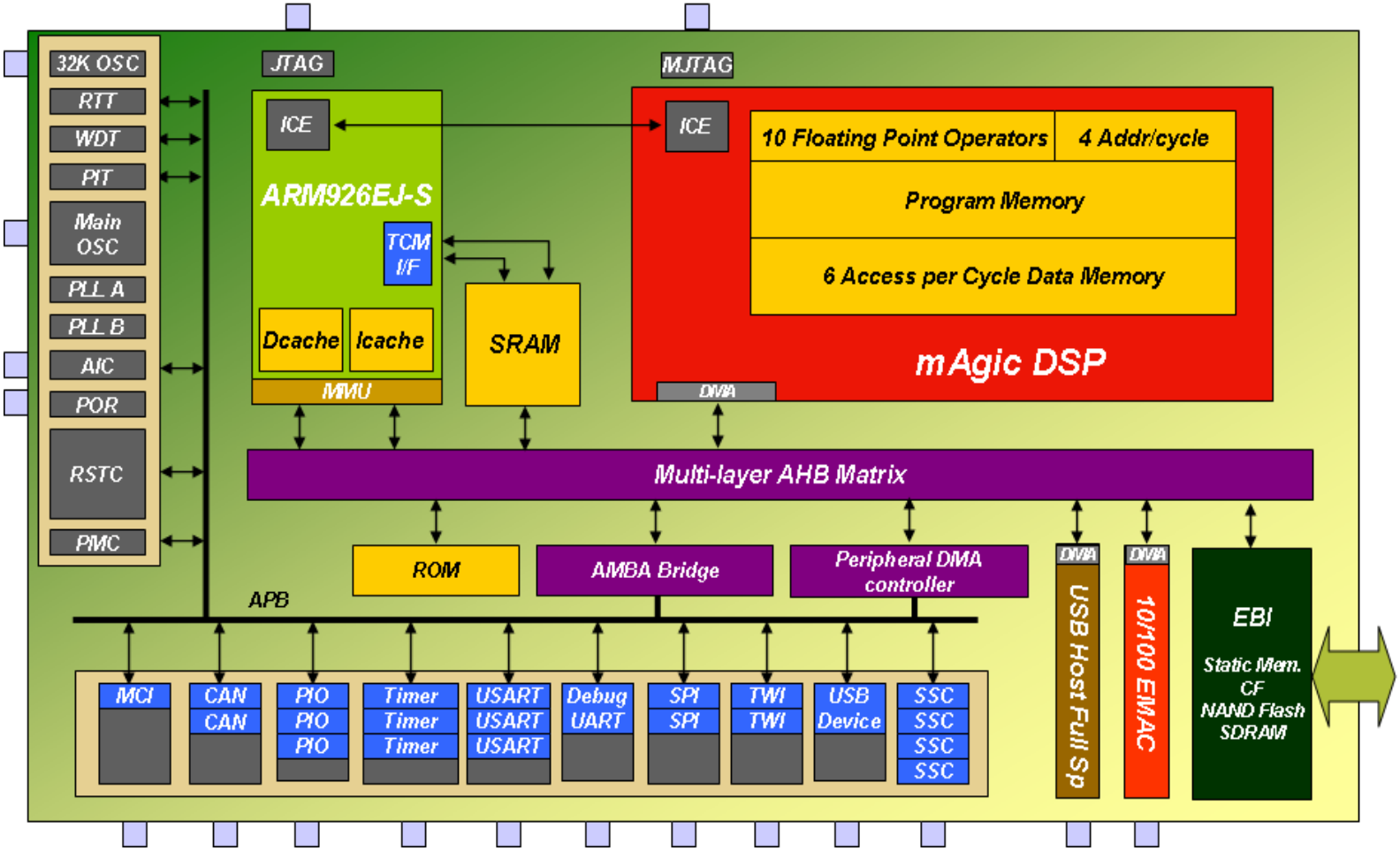
mAgicV IP Interfaces

- **Interfaces: (Functional IO → 255)**
  - **Reset: resetn**
  - **Clocks:**
    - **Hclk → AHB system clock**
    - **Clk → Core clock: (Hclk / x) with integer x**
    - **Clk200 → Memory clock: (Clk * 2)**
  - **AHB std Master Interface (115)**
  - **AHB Slave Interface (112) (compliant to sdt Lite → neither retry or split)**
  - **IRQ In:**
    - **sharm_irq0 (4 in grouped on int0), sharm_irq1 (4 in grouped on int1),**
    - **arm_irq(0) (on int2), arm_irq(1) (on int3)**
  - **IRQ Out:**
    - **sirq(0,1): pulse generation**
    - **sirq (2,3): toggling level generation**
    - **system interrupts: halt, exception, run, dma_eot**
  - **DBG Cross-triggering:**
    - **dbg_req_fr_arm, dbg_req_to_arm**
  - **BIST: single memory selectable BIST with bit error detecting (3 cntl + 6 results)**
  - **LOGIC SCAN: 20 scan lines (20 + 20 + 7)**

mAgicV IP Physical Characteristics

- **Gate count and area (0.13u process – 6 Metal Layers)**
  - **Core Logic = 580 kgates → cells area ~3.1 mm² / block area ~4.9 mm2 (density 63%)**
  - **Register File (2 x 128 x 40) = 265 kgates → cells area ~ 1.4 mm² / block area ~2.0 mm2 (density 70%)**
  - **PM SPRAM (4 x 8K x 32) → ~ 3.4 mm²**
  - **DM DPRAM (2 x 8K x 40) → ~ 5.2 mm²**
  - **Total Core area (w/o power stripes) → cells area ~ 13.1 mm² → block area 15.5 mm²**

Diopsis: ARM926 plus 1GFLOPS DSP



Very Low Power 250 mW core (hard test), package 15x15mm, pitch 0.8mm

Magic DSP™ benchmark

DSP Library

- **C callable optimized functions, written in C**
  - **Good template for code optimization**
  - **Functions can be modified and adapted if needed**
- **More than 200 functions available, covering all the basics of DSP**
- **All the functions works on array of the following types:**
  - **float / long**
  - **_v_float / _v_long**
  - **_c_float / _c_long**
- **Main groups of functions:**
  - **Simple:** array addition, fill, move, mul, fix, clip, sum…
  - **Trigonometric and hyperbolic:** sin, cos, tan, atan, asin, sinh, asinh…
  - **Power:** log, exp
  - **Matrix:** add, mul, determ, inverse, decomposition, trace…
  - **Miscellaneous:** sort, rand, sqrt, div, max, dist…
  - **DSP:** CrossCorr, Conv, levinson recursion, cepstral coeff. computation…
  - **Filters:** different implementations of FIRs and IIRs
  - **FFT and iFFT:** FFTs and iFFT for several number of points, real and complex data types

Performances

- **Performances of a DSP functions representative subset:**

Algorithm	Expected kernel length for sample	Actual kernel length for sample	Kernel performances
vfAdd	1.75	1.75	100 %
cfMul	1.5	1.5	100 %
vfDiv	6	6	100 %
vfSqrt	14	15	92 % (*)
vfLog	22	25	86 %
vfCos	19	19	100 %
vfExp	20	22	90 % (*)
FIR	1	1	100 %
FFT1024	5120 (80 - 80)	5511 (82 - 84)	~ 95 %

- **All the functions are written in C**

(*) Increasing the unrolling factor kernel performances reach 100 %
vf prefix → vector float data type
cf prefix → complex float data type

DSPLib documentation snapshot

Function	# Cycles	# VLIW	Interrupt Tolerant	Interruptible	Reserved Registers Used	Usable with arrays of single data aligned at dword
ALawToLin	42+Nx3	81	Y	Y	N	-
CepstrumToLP	Len even: 1.25 x N x N + 52 x N - 26.00 Len odd : 1.25 x N x N + 52 x N - 27.25	88	Y	Y	N	-
cfByfDivide	51+Nx8	59	Y	Y	N	N
cfClip	66+Nx11	110	Y	Y	N	N
cfConjConjMul	22+Nx1.5	28	Y	Y	N	N
cfConjMul	22+Nx1.5	28	Y	Y	N	N
cfConjScaleOffset	19+Nx1.25	24	Y	Y	N	N
cfConv	L odd: 62+10xL+ 1.25x(L-1)xM L even: 75+10xL+ (1.25xL+1)xM	146	Y	Y	N	N
cfConv_fast	L odd: 49.5 + 9.5xL + (L-1)xM L even: 63.5+ 9.5xL + (L+1)xM	151	N	Y	N	N
cfConv2d	43+(M-K+1)x(14+(N-K+1)x(11+Kx(8+1.25xK)))	89	Y	Y	N	N
cfDFTFwd_CToC	115+N+(N-1) x (23+5 x (int)[(N-1)/2])	147	Y	Y	N	N
cfDFTInv_CToC	106+N+(N-1) x (20+5 x (int)[(N-1)/2])	138	Y	Y	N	N
cfDist	86+9.5xN	150	Y	Y	N	N
cfDiv32	23+8xN	31	Y	Y	N	N
cfDiv40	34+10xN	44	Y	Y	N	N
cfDot	31+1.25xN	36	Y	Y	N	N
cfDot_fast	28+N	32	N	Y	N	N

Performance details available for all the 200+ functions in the DSPLib, making the performance of mAgic predictable.

Each function documented in detail in the DSPLib Manual

Programming Tools

mAgicV DSP: Native C Programming

- Performance from C better than hand-optimized assembler
- Support many processor independent optimizations.
- Support “memory disambiguation ”
- Support interrupt handling
- Back end optimizations including loop unrolling, SW pipelining and predicated execution

mAgic Tools

- **Third party Target Compiler Technologies Tool suite:**
  - **C compiler with GUI and project management**
  - **Binary tools**
  - **JTAG Debugger with GUI**
- **Custom tools including:**
  - **Code compressor**
- **Libraries:**
  - **Math lib**
  - **DSP lib (≈200 vectorial functions) – IPP compatibility ongoing**
  - **DBIOS library**
  - **Hosted I/O support libraries**

TARGET COMPILER TECHNOLOGIES

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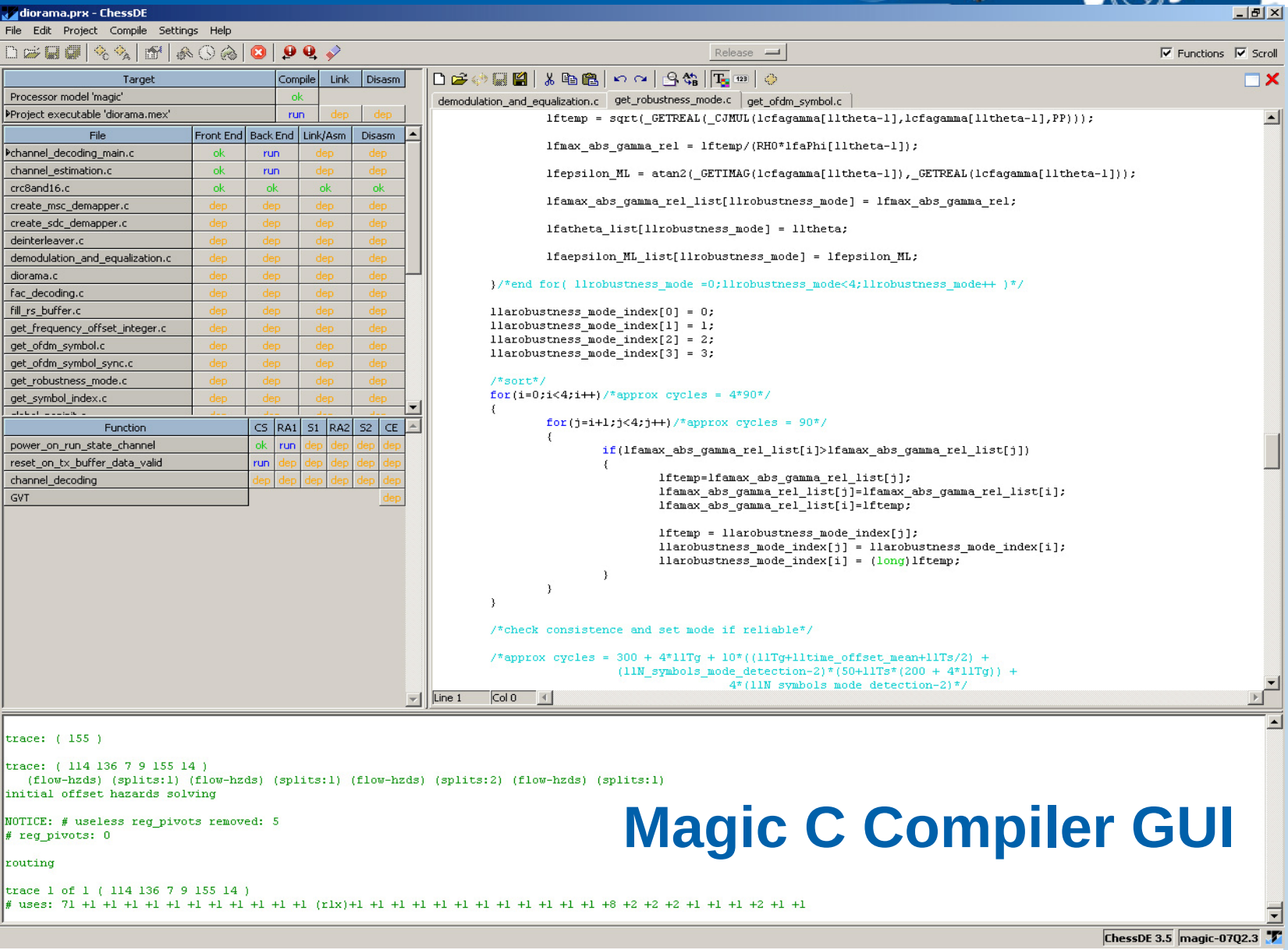
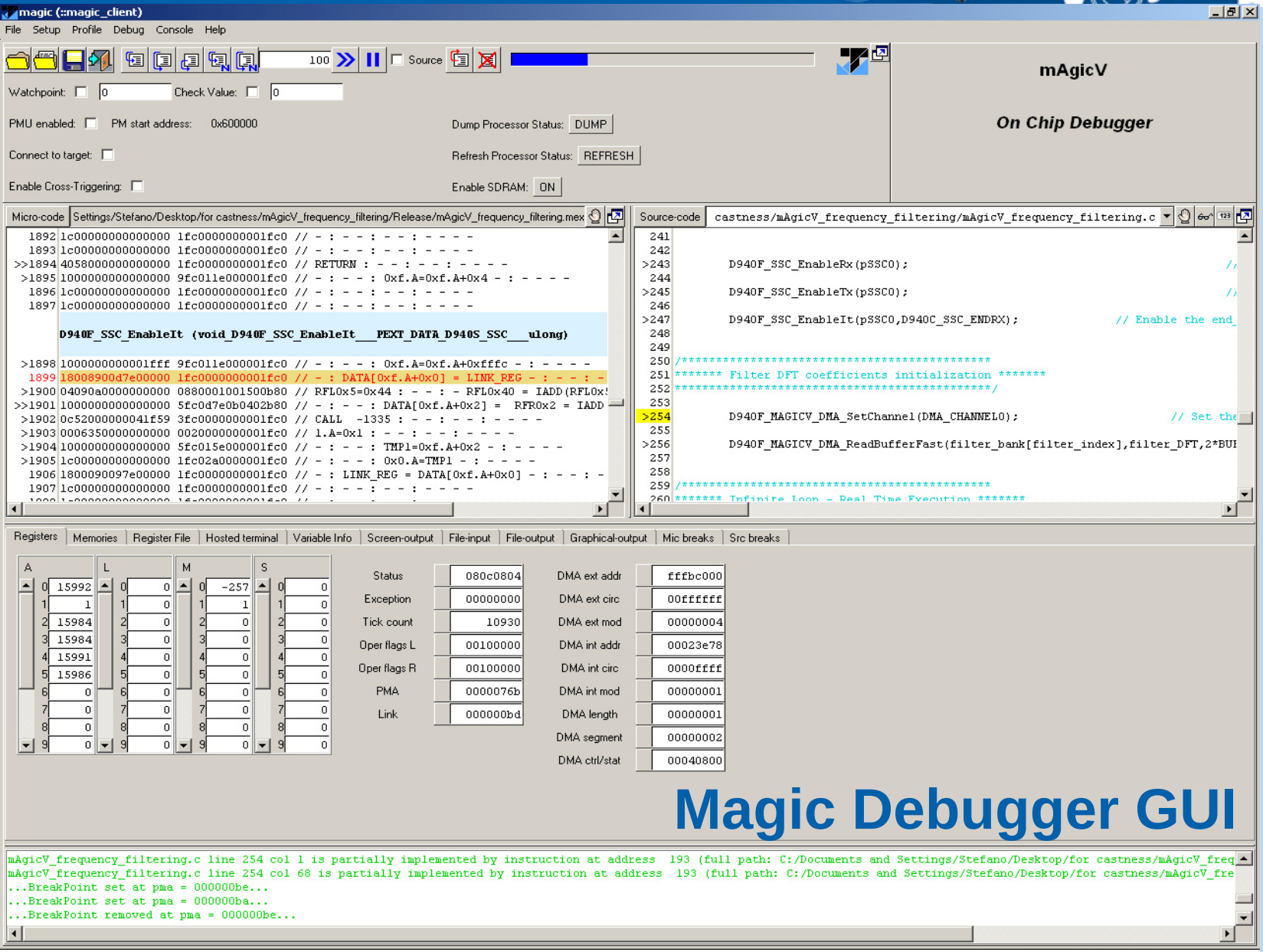


Magic C Compiler GUI



Magic Debugger GUI

Thank You