



# Magic DSP™



## AGENDA

- **Magic DSP features**
- **Magic DSP benchmark**
- **Programming tools**



# Magic DSP™ features

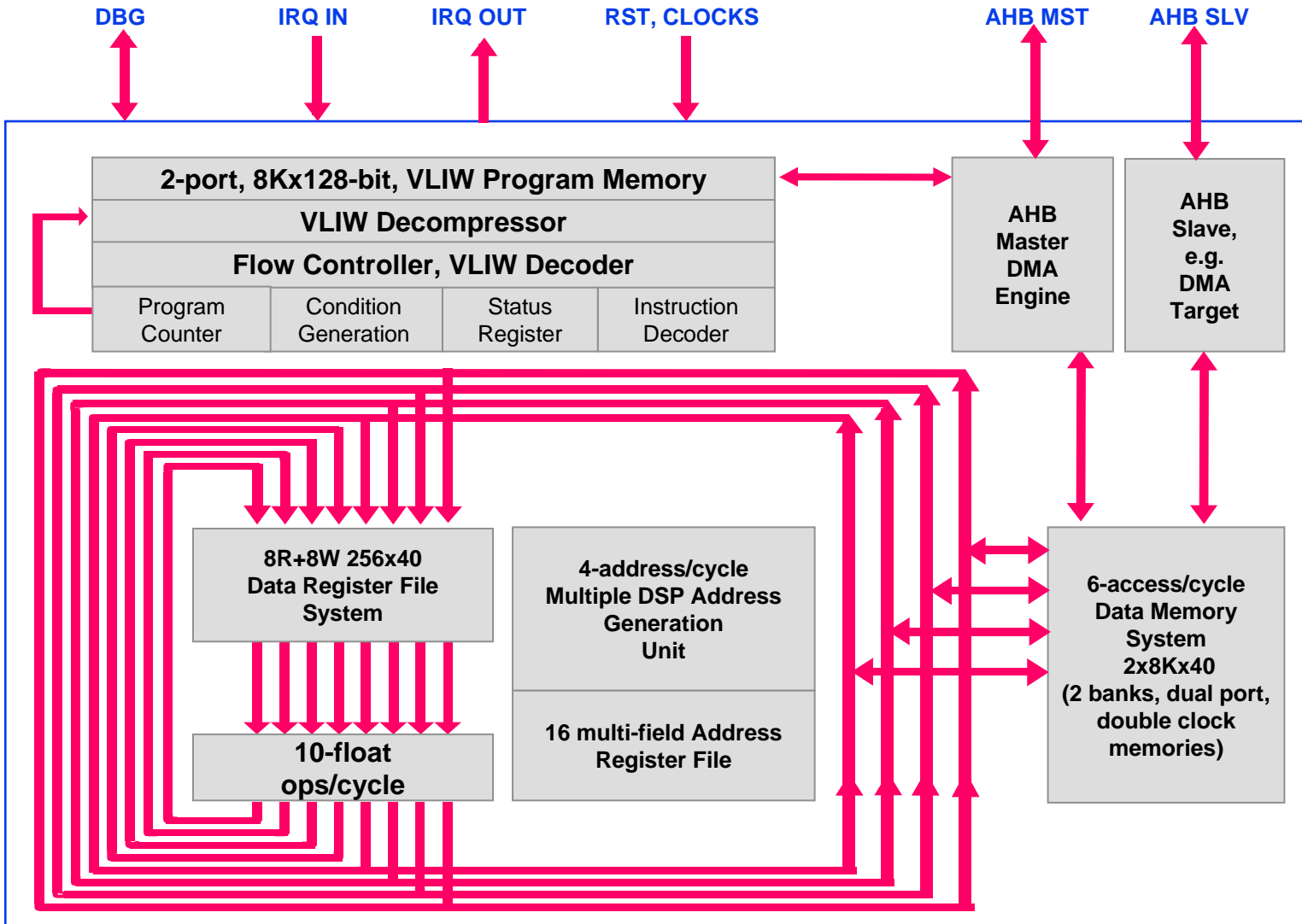


## Magic DSP features

- C programmable VLIW DSP
- Floating point 32 / 40 bit
- Up to 10 floating point operations per cycle
  - 1GFLOPS @ 100MHz in 130nm (available)
  - 2GFLOPS @ 200MHz in 90nm (P&R estimate)
  - 2.75GFLOPS @ 275MHz in 65nm (P&R estimate)
- 2 address generation units, 4 memory accesses per cycle
- 6 port memory system allowing concurrent computation and data move
- Float – vector – complex native data type support
- Program Memory Management Unit (PMU). PM cache
- DMA engine supporting stridden memory accesses
- AMBA AHB master and slave bus interface
- Low power: 0.17 mW/MFLOPS mAgic (0.36 mW / MIPS ARM)



# mAgicV IP Architecture





## mAgicV IP Interfaces

### ■ Interfaces: (Functional IO → 255)

- **Reset:** resetn
- **Clocks:**
  - Hclk → AHB system clock
  - Clk → Core clock: (Hclk / x) with integer x
  - Clk200 → Memory clock: (Clk \* 2)
- **AHB std Master Interface (115)**
- **AHB Slave Interface (112) (compliant to sdt Lite → neither retry or split)**
- **IRQ In:**
  - sharm\_irq0 (4 in grouped on int0), sharm\_irq1 (4 in grouped on int1),
  - arm\_irq(0) (on int2), arm\_irq(1) (on int3)
- **IRQ Out:**
  - sirq(0,1): pulse generation
  - sirq (2,3): toggling level generation
  - system interrupts: halt, exception, run, dma\_eot
- **DBG Cross-triggering:**
  - dbg\_req\_fr\_arm, dbg\_req\_to\_arm
- **BIST: single memory selectable BIST with bit error detecting (3 cntl + 6 results)**
- **LOGIC SCAN: 20 scan lines (20 + 20 + 7)**

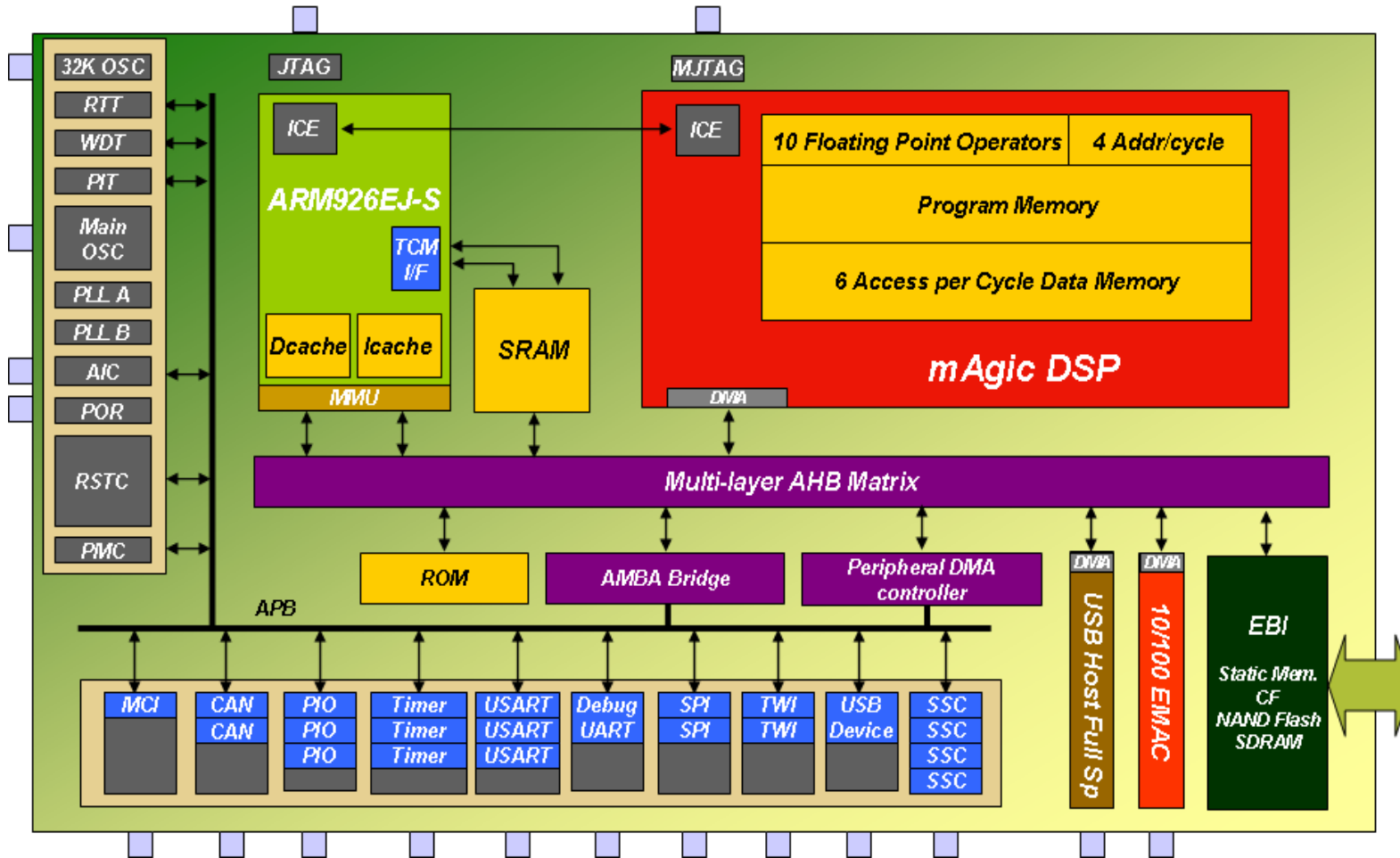


## mAgicV IP Physical Characteristics

### ■ Gate count and area (0.13u process – 6 Metal Layers)

- Core Logic = 580 kgates → cells area ~3.1 mm<sup>2</sup> / block area ~4.9 mm<sup>2</sup> (density 63%)
- Register File (2 x 128 x 40) = 265 kgates → cells area ~1.4 mm<sup>2</sup> / block area ~2.0 mm<sup>2</sup> (density 70%)
- PM SPRAM (4 x 8K x 32) → ~ 3.4 mm<sup>2</sup>
- DM DPRAM (2 x 8K x 40) → ~ 5.2 mm<sup>2</sup>
- Total Core area (w/o power stripes) → cells area ~ 13.1 mm<sup>2</sup> → block area 15.5 mm<sup>2</sup>

# Diopsis: ARM926 plus 1GFLOPS DSP



Very Low Power 250 mW core (hard test), package 15x15mm, pitch 0.8mm





# Magic DSP™ benchmark



## DSP Library

- **C callable optimized functions, written in C**
  - Good template for code optimization
  - Functions can be modified and adapted if needed
- **More than 200 functions available, covering all the basics of DSP**
- **All the functions works on array of the following types:**
  - float / long
  - `_v_float` / `_v_long`
  - `_c_float` / `_c_long`
- **Main groups of functions:**
  - **Simple:** array addition, fill, move, mul, fix, clip, sum...
  - **Trigonometric and hyperbolic:** sin, cos, tan, atan, asin, sinh, asinh...
  - **Power:** log, exp
  - **Matrix:** add, mul, determ, inverse, decomposition, trace...
  - **Miscellaneous:** sort, rand, sqrt, div, max, dist...
  - **DSP:** CrossCorr, Conv, levinson recursion, cepstral coeff. computation...
  - **Filters:** different implementations of FIRs and IIRs
  - **FFT and iFFT:** FFTs and iFFT for several number of points, real and complex data types



## Performances

### ■ Performances of a DSP functions representative subset:

Algorithm	Expected kernel length for sample	Actual kernel length for sample	Kernel performances
vfAdd	1.75	1.75	100 %
cfMul	1.5	1.5	100 %
vfDiv	6	6	100 %
vfSqrt	14	15	92 % ( * )
vfLog	22	25	86 %
vfCos	19	19	100 %
vfExp	20	22	90 % ( * )
FIR	1	1	100 %
FFT1024	5120 (80 - 80)	5511 (82 - 84)	~ 95 %

### ■ All the functions are written in C

( \* ) Increasing the unrolling factor kernel performances reach 100 %

vf prefix → vector float data type

cf prefix → complex float data type



# DSPLib documentation snapshot

**Performance details available for all the 200+ functions in the DSPLib, making the performance of mAgic predictable.**

**Each function documented in detail in the DSPLib Manual**

Function	# Cycles	# VLIW	Interrupt Tolerant	Interruptible	Reserved Registers Used	Usable with arrays of single data aligned at dword
ALawToLin	42+Nx3	81	Y	Y	N	-
CepstrumToLP	Len even: 1.25 x N x N + 52 x N - 26.00 Len odd : 1.25 x N x N + 52 x N - 27.25	88	Y	Y	N	-
cfByfDivide	51+Nx8	59	Y	Y	N	N
cfClip	66+Nx11	110	Y	Y	N	N
cfConjConjMul	22+Nx1.5	28	Y	Y	N	N
cfConjMul	22+Nx1.5	28	Y	Y	N	N
cfConjScaleOffset	19+Nx1.25	24	Y	Y	N	N
cfConv	L odd: 62+10xL+ 1.25x(L-1)xM L even: 75+10xL+ (1.25xL+1)xM	146	Y	Y	N	N
cfConv_fast	L odd: 49.5 + 9.5xL + (L-1)xM L even: 63.5+ 9.5xL + (L+1)xM	151	N	Y	N	N
cfConv2d	43+(M-K+1)x(14+(N-K+1)x(11+Kx(8+1.25xK)))	89	Y	Y	N	N
cfDFTFwd_CToC	115+N+(N-1) x (23+5 x (int)((N-1)/2))	147	Y	Y	N	N
cfDFTInv_CToC	106+N+(N-1) x (20+5 x (int)((N-1)/2))	138	Y	Y	N	N
cfDist	86+9.5xN	150	Y	Y	N	N
cfDiv32	23+8xN	31	Y	Y	N	N
cfDiv40	34+10xN	44	Y	Y	N	N
cfDot	31+1.25xN	36	Y	Y	N	N
cfDot_fast	28+N	32	N	Y	N	N





# Programming Tools



## mAgicV DSP: Native C Programming

- Performance from C better than hand-optimized assembler
- Support many processor independent optimizations.
- Support “memory disambiguation ”
- Support interrupt handling
- Back end optimizations including loop unrolling, SW pipelining and predicated execution



## mAgic Tools

- **Third party Target Compiler Technologies Tool suite:**
  - C compiler with GUI and project management
  - Binary tools
  - JTAG Debugger with GUI
- **Custom tools including:**
  - Code compressor
- **Libraries:**
  - Math lib
  - DSP lib ( $\approx 200$  vectorial functions) – IPP compatibility ongoing
  - DBIOS library
  - Hosted I/O support libraries



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# mAgic DSP overview

The screenshot displays the mAgicV On Chip Debugger interface. At the top, the title bar reads "magic (:magic\_client)". The main window is titled "mAgicV On Chip Debugger".

**Control Panel:**

- File Setup Profile Debug Console Help
- Watchpoint:  0 Check Value:  0
- PMU enabled:  PM start address: 0x600000 Dump Processor Status: DUMP
- Connect to target:  Refresh Processor Status: REFRESH
- Enable Cross-Triggering:  Enable SDRAM: DN

**Source Code:** `castness/mAgicV_frequency_filtering/mAgicV_frequency_filtering.c`

```

1892 1c00000000000000 1fc0000000001fc0 // - : - : - : - : - : - :
1893 1c00000000000000 1fc0000000001fc0 // - : - : - : - : - : - :
>>1894 4058000000000000 1fc0000000001fc0 // RETURN: - : - : - : - : - :
>1895 1000000000000000 9fc011e000001fc0 // - : - : - : 0xf.A=0xf.A+0x4 - : - : - :
1896 1c00000000000000 1fc0000000001fc0 // - : - : - : - : - : - :
1897 1c00000000000000 1fc0000000001fc0 // - : - : - : - : - : - :

D940F_SSC_EnableIt (void D940F_SSC_EnableIt PEXT_DATA D940S_SSC_ulong)

>1898 1000000000001fff 9fc011e000001fc0 // - : - : - : 0xf.A=0xf.A+0xffc - : - : - :
1899 1800890d7e00000 1fc0000000001fc0 // - : DATA[0xf.A+0x0] = LINK_REG - : - : - :
>1900 04090a0000000000 0880001001500b80 // RFL0x5=0x44 : - : - : RFL0x40 = IADD (RFL0x
>>1901 1000000000000000 5fc0d7e0b0402b80 // - : - : - : DATA[0xf.A+0x2] = RFR0x2 =
>1902 0c52000000041f59 3fc0000000001fc0 // CALL -1335 : - : - : - : - : - :
>1903 0006350000000000 0020000000001fc0 // 1.A=0x1 : - : - : - : - : - :
>1904 1000000000000000 5fc015e000001fc0 // - : - : - : TMP1=0xf.A+0x2 - : - : - :
>1905 1c00000000000000 1fc02a0000001fc0 // - : - : - : 0x0.A=TMP1 - : - : - :
1906 1800090097e00000 1fc0000000001fc0 // - : LINK_REG = DATA[0xf.A+0x0] - : - : - :
1907 1c00000000000000 1fc0000000001fc0 // - : - : - : - : - : - :
1908 1c00000000000000 1fc0000000001fc0 // - : - : - : - : - : - :
241
242
>243 D940F_SSC_EnableRx (pSSCO); //
244
>245 D940F_SSC_EnableTx (pSSCO); //
246
>247 D940F_SSC_EnableIt (pSSCO, D940C_SSC_ENDRX); // Enable the end
248
249
250 /*****
251 ***** Filter DFT coefficients initialization *****/
252 *****/
253
>254 D940F_MAGICV_DMA_SetChannel (DMA_CHANNEL0); // Set the
255
>256 D940F_MAGICV_DMA_ReadBufferFast (filter_bank [filter_index], filter_DFT, 2*BU
257
258
259 /*****
260 ***** Infinite Loop - Real Time Execution *****/
261

```

**Registers:**

A	L	M	S	Status	DMA ext addr
0 15992	0 0	0 -257	0 0	080c0804	ffbc000
1 1	1 0	1 1	1 0	Exception	00ffffff
2 15984	2 0	2 0	2 0	Tick count	00000004
3 15984	3 0	3 0	3 0	Oper flags L	00100000
4 15991	4 0	4 0	4 0	Oper flags R	00100000
5 15986	5 0	5 0	5 0	PMA	0000076b
6 0	6 0	6 0	6 0	Link	000000bd
7 0	7 0	7 0	7 0	DMA ext circ	00000001
8 0	8 0	8 0	8 0	DMA int addr	0000ffff
9 0	9 0	9 0	9 0	DMA int circ	00000001
				DMA ext mod	00000002
				DMA ext addr	00040800

**Registers Table:**

Register	Value
A0	15992
L0	0
M0	-257
S0	0
Status	080c0804
DMA ext addr	ffbc000
Exception	00000000
DMA ext circ	00ffffff
Tick count	10930
DMA ext mod	00000004
Oper flags L	00100000
DMA int addr	00023e78
Oper flags R	00100000
DMA int circ	0000ffff
PMA	0000076b
DMA int mod	00000001
Link	000000bd
DMA length	00000001
DMA segment	00000002
DMA ctrl/stat	00040800

**Registers Panel:** Registers A, L, M, S, Status, Exception, Tick count, Oper flags L, Oper flags R, PMA, Link, DMA ext addr, DMA ext circ, DMA ext mod, DMA int addr, DMA int circ, DMA int mod, DMA length, DMA segment, DMA ctrl/stat.

**Console:**

```

mAgicV_frequency_filtering.c line 254 col 1 is partially implemented by instruction at address 193 (full path: C:/Documents and Settings/Stefano/Desktop/for castness/mAgicV_fre
mAgicV_frequency_filtering.c line 254 col 68 is partially implemented by instruction at address 193 (full path: C:/Documents and Settings/Stefano/Desktop/for castness/mAgic_fre
...BreakPoint set at pma = 000000be...
...BreakPoint set at pma = 000000ba...
...BreakPoint removed at pma = 000000be...

```

## Magic Debugger GUI





# Thank You