Software development tools synthesis

Kjeld Hjortnaes – TEC-SWS
On-Board Software Systems Section

Software development tools

- The following slides gives a synthesis of commonly used tools for the ESA space micro-processors (ERC32 & LEON's).
- The list is focusing mainly on tools that are target hardware dependent.

Code generation tools

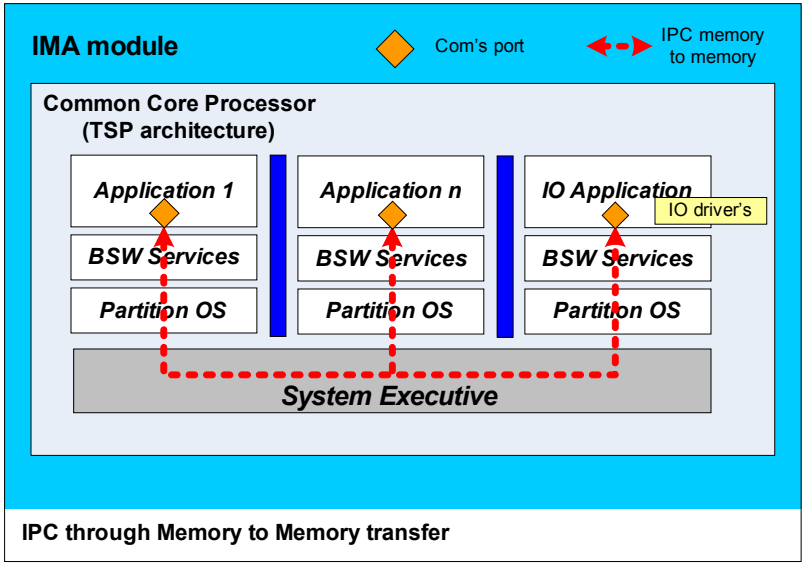
Cross compilers		ERC-32	LEON-II	LEON-III	Supplier	
C/C++	GCC	✓	✓	✓	GNU	
ADA	GNAT-PRO	✓	✓	Not yet	AdaCore	
	XGC	✓			Chris Nettleton	
	ObjectADA	✓	✓		Aonix	
JAVA	OVM		✓		Purdue Uni	
	PERC		✓		Aonix	
	Jamaica/ AERO	✓	✓		AICAS	
Matlab/ Simulink/ stateflow	Targetlink	Generates C-code			DSpace	
	Real Time workshop	Generates C/C++ code			MathWorks	

Available RTOS

RTOS		ERC-32	LEON-II	LEON-III	LEON-III (MMU)	Supplier
RTEMS (LGPL)	V4.8.0 (Open Src)	✓	✓	✓		Edisoft / OAR
	V4.6.5	✓	✓			OAR.
	V4.6.1+	✓				Astrium
VxWorks	V6.5-leon		✓	✓	✓	WindRiver
	V5.4-leon		✓	✓		WindRiver
eCOS (GPL)	V3.x	✓		✓ (SMP)	✓	Aeroflex-GR
ORK	Integrated with GNAT	✓	✓			UPM
Ostrales	Uses GNATPro	✓	(✓)			TAS (internal)

Available RTOS for Time & Space Partitioning

TSP RTOS		ERC-32	LEON-II	LEON-III	LEON-III (MMU)	Supplier
AIR-II RTEMS	TRL-3(4)		✓			GMV-SkySoft
PikeOS	Being ported to LEON		✓	✓	✓	SYSGO
XTratum	Being ported to LEON		✓	✓	✓	Uni of Valencia



Simulator / emulator support

Software emulators		ERC-32	LEON-II	LEON-III	LEON-III (MMU)	Supplier
TSIM	Instruction level	✓	✓ (0.3 x RT)	✓	✓	Aeroflex-GR
Leon-SVE	Instruction level	✓	✓			Spacebel
SimERC32/ SimLEON	Instruction level	✓	✓	✓		Astrium / CNES
Sim-SCOC3	Instruction level				✓	Astrium (internal)
QERx (LGPL)	Dynamic translation	✓	✓ (4-8 x RT)			FFQTECH SciSys Uni of Coimbra
ReSP (GPL)	Instruction level		✓	✓	Coming Soon	Politecnico of Milan
ESOC simulator	Instruction level	✓				ESOC

Dynamic translation emulator vs. TSIM

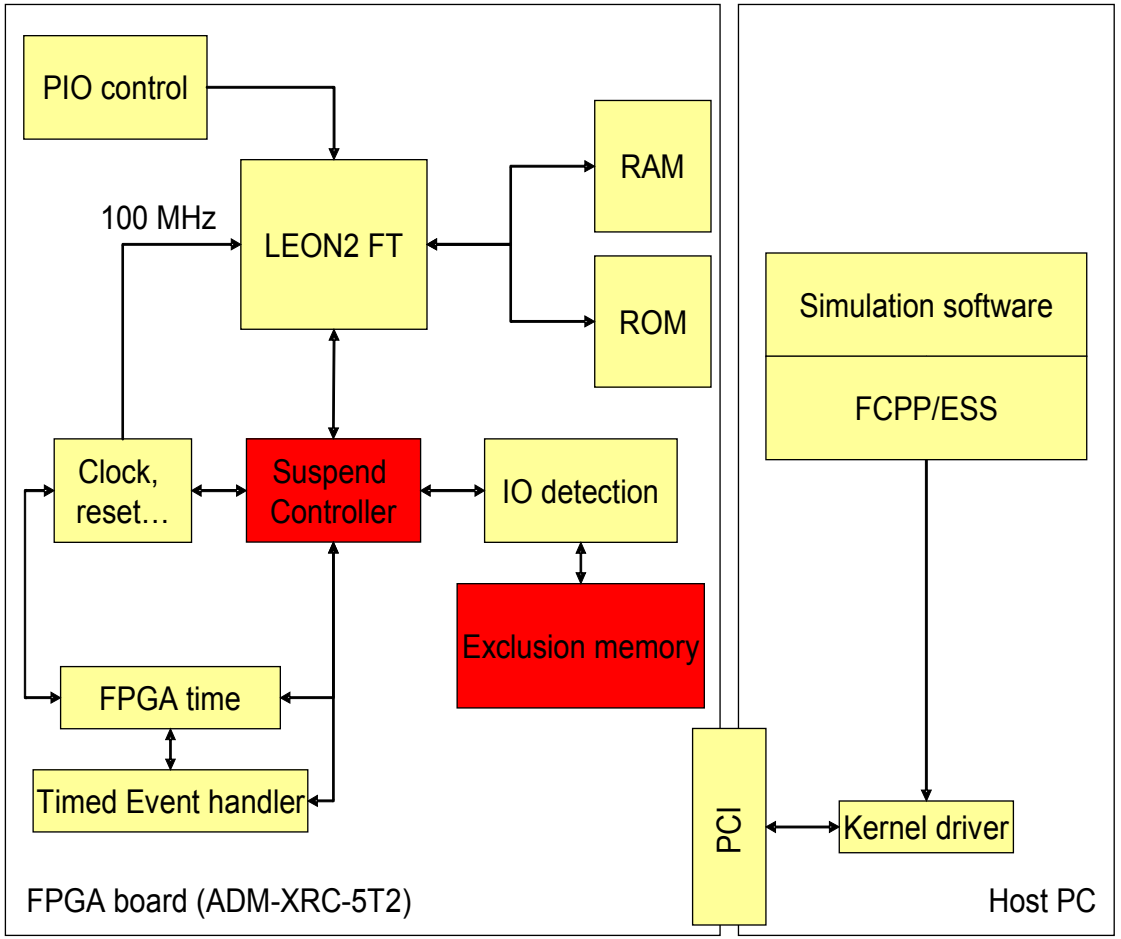
	TSIM ERC32*	QERx ERC32*	TSIM LEON2	QERx LEON2
Stanford Raw	1.23s	0.29s	2.43s	0.30s
Dhrystone Raw	64.20s	9.68s	216.00s	9.22s
Stanford Factor	1	4.2	1	8.1
Dhrystone Factor	1	6.6	1	23.4

- Stanford Benchmark provided with TSIM (not recompiled)
- Dhrystone benchmark, 1 Million iterations (recompiled from source)
- *ERC32
  - TSIM ERC32 v1.3
  - 32-bit SUSE 8.2, 2.8 GHz Intel Pentium 4 processor
- LEON2
  - TSIM LEON2 v2.0.9
  - 32-bit SUSE 10.1, 2.8 GHz Intel Pentium 4 processor
  - Simplistic cache modelling in QERx
- LEON TSIM slower that ERC32 TSIM
- QERx LEON2 ~10% faster than QERx ERC32 – timer model differences?

Simulator / emulator support

Hw-in-loop emulators		ERC-32	LEON-II	LEON-III	LEON-III (MMU)	Supplier
SHAM6	µ-p in the loop	✓ (25 Mhz)				Chess Engineering
LEON-SVF	FPGA LEON-II FT IP core		✓ (100 MHz)			ESA/Astrium -sas
TSIM-HW	FPGA LEON-II IP core		✓ (100 MHz)			Aeroflex-GR

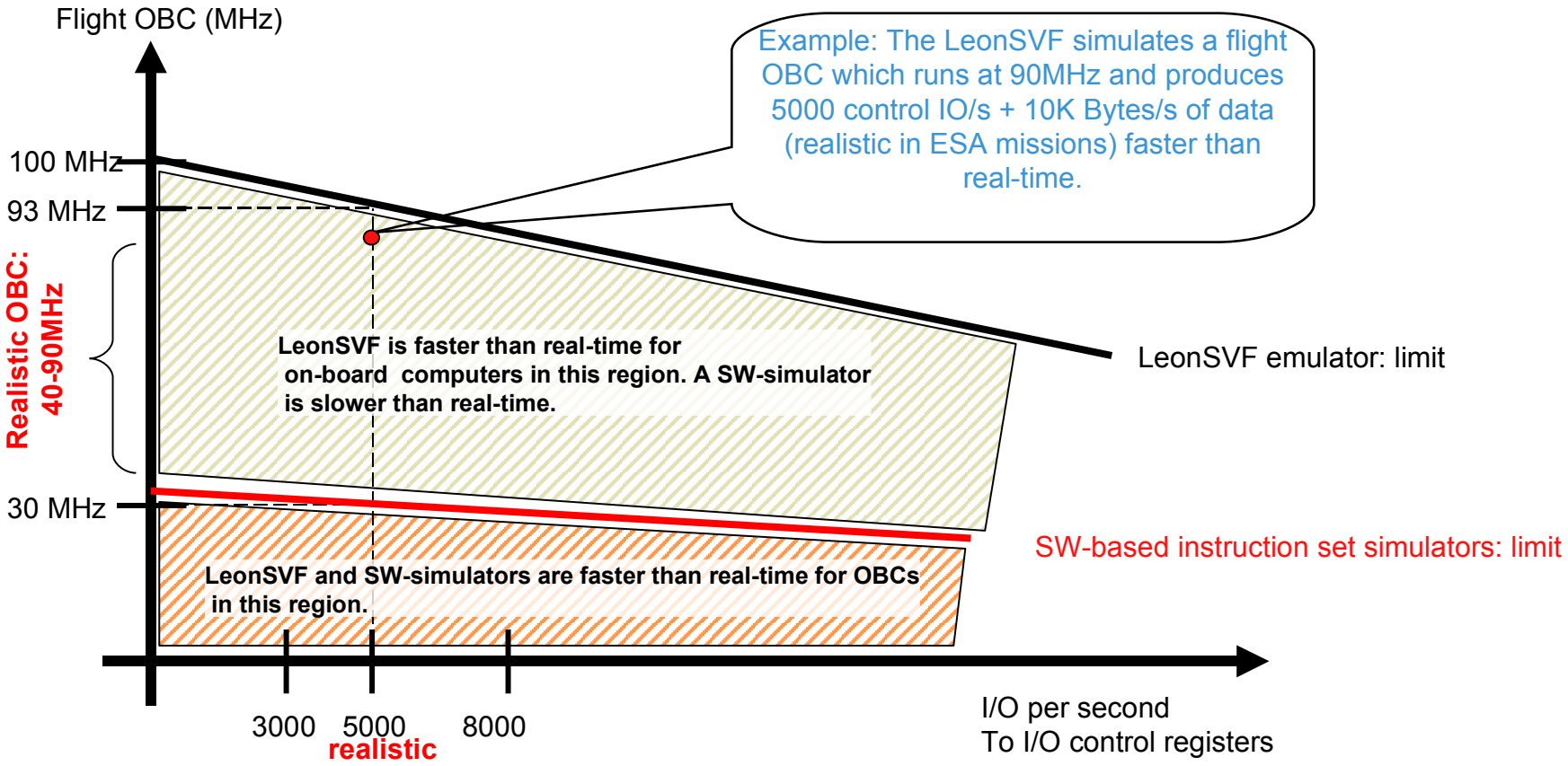
LEON emulator architecture



Key function Suspend Controller will suspend Leon while simulating I/O

LEON emulator performance

Emulator outperforms instruction set software simulators



Worst case execution tools

		ERC-32	LEON-II	LEON-III	LEON-III (MMU)	Supplier
Ait WCET	C and Ada Binary image		✓	✓		AbsInt
Rapitime	C and Ada measurement by code instrumentation	✓	✓	✓	(✓)	Rapita
Bound-T	Binary image	✓				Tidorum

Test tools

Unit and Integration test		ERC-32	LEON-II	LEON-III	LEON-III (MMU)	Supplier
CANTATA++	C/C++	Src code instrumentation				IPL
Adatest95	Ada95	Src code instrumentation				IPL
VectorCAST	C/C++/Ada	Src code instrumentation				Vector software
IBM-Rational Test Real Time	C/C++/ Java/Ada	Src code instrumentation				IBM
Klocworks	C/C++	Static analysis				IPL
Polyspace	C/C++/Ada	Static analysis				Mathworks