HiDCM-CLP
## (High integration Digital Control Module – Control Loop Processor)

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Abstract

Nowadays, space applications cover a large diversity of embedded functions ranging from on-board global management up to very specific tasks such as image processing, instrument positioning and so on. Because of its inherent flexibility and/or processing capability, the space community preferably utilizes a technical approach focused on software-based electronics. The field of control loops characterized by <u>hard real-time</u> constraints (loop frequency > 1 kHz) in conjunction with complex algorithmic needs currently lacks a microprocessor allowing to make the software approach economically and technically viable.

Electrical servo-actuator control, one of S.A.B.C.A company's core business, is an example of impacted application. A GSTP2 program allowed the company to develop a dedicated space-hardened microprocessor, called HBRISC2, integrating several architecture-specific features. In particular, the component includes a cache-free and RISC architecture to ensure a fully deterministic behaviour, an embedded robustness/anomaly management and a dual floating-points unit for high-demanding computation needs. In addition, a Simulink-based development environment allows automatic OS-less code generation.
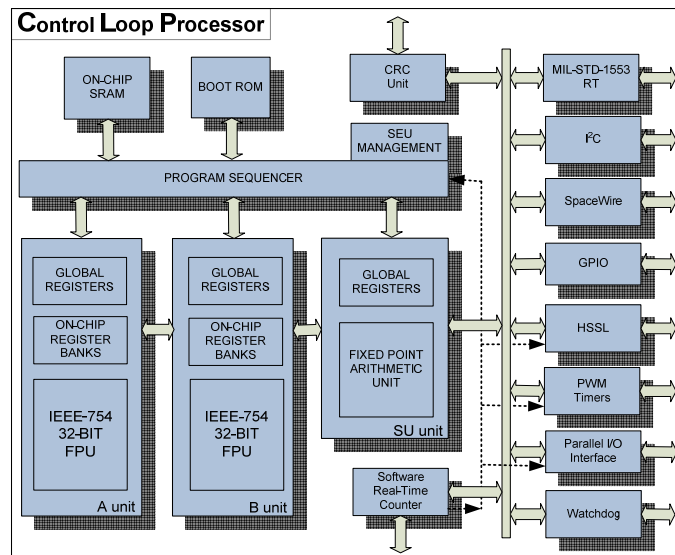
Today, the intention is to open this processor to general users facing similar issues. The development of a standard product – called Control Loop Processor (CLP) - based on HBRISC2 architecture, released from ITAR rules and harmonized towards ESA standards (IEEE-754 format, standard spacecraft I/Fs,…) is currently being evaluated by S.A.B.C.A. and ESA TEC/ED division. The development of one or several CLP's companion analog circuits is also foreseen to provide the required hardware support at the application level

(typically for efficient on-board sensors management). A complete project consortium, covering all aspects such as design, commercialisation, support and maintenance needs to be settled. The intention being to raise the CLP up to the status of "building block".