New Developments & Investigation Areas

Session 3 of

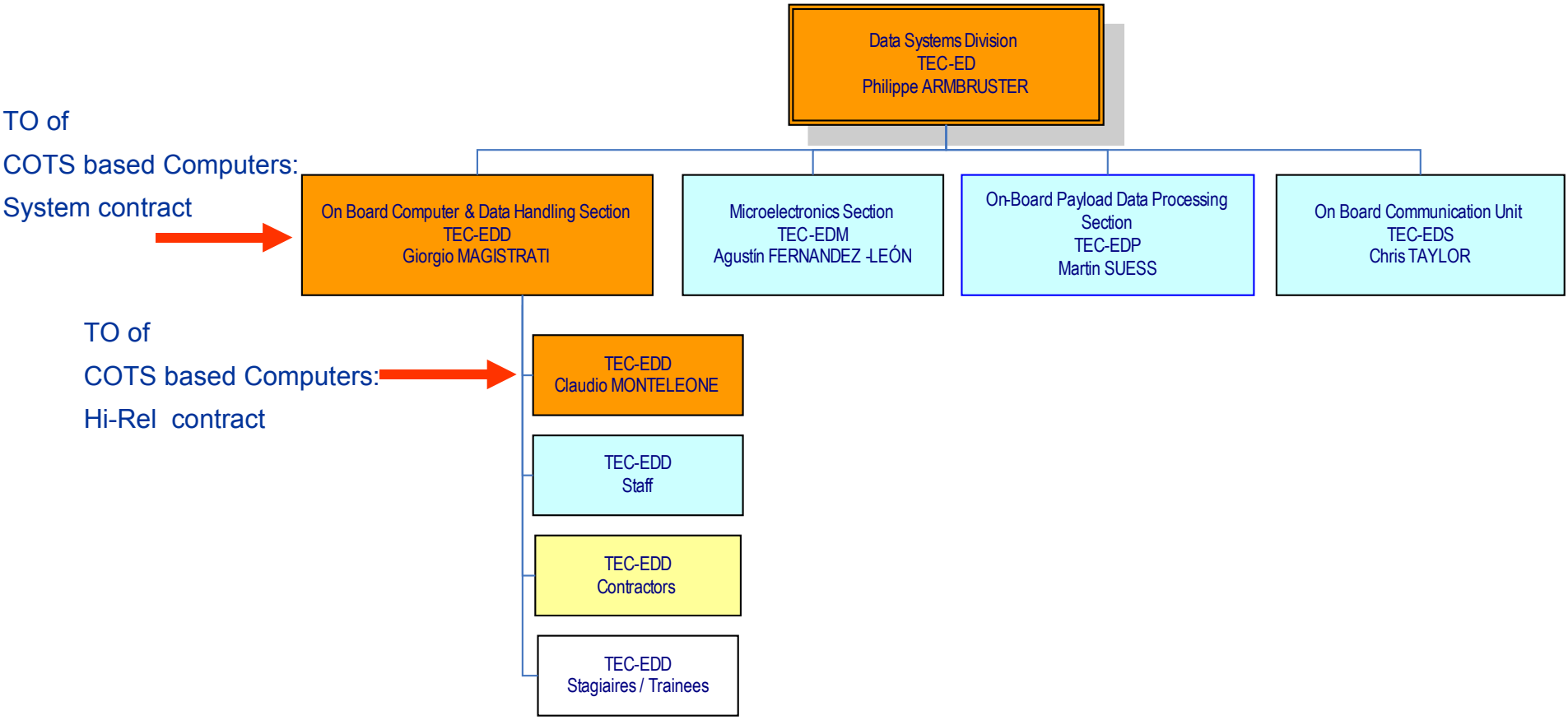
Round Table on MicroProcessors for Space Applications

List of Contents

- Requirements for MicroProcessors,
- Microprocessors Roadmap:
  - DSP,
  - COTS,
  - Development of µControllers for specific applications,
- New Developments,
- Agenda of Session 3.

TEC-ED Sections:

On Board Computer & Data Handling



Requirements for uProcessors

Science and Earth Observation missions, Telecom Satellites and Exploration programs are asking for micro-processors with **increased processing performance,**

Regardless of the increased level of complexity and performance a **high level of reliability and availability** have to be guaranteed,

Miniaturization, high integration and reduced Power consumption are mandatory features of the future On board Platform and Payload Computer and these requirements are driving the design of the future microprocessors,

The design of the microprocessor is driven also by the availability of other technologies available for space applications (e.g. **Memories, I/O I/Fs**) but can also drive them (e.g. **PoL regulators**),

Availability of tools for the complete development of the software is a reality but more and more complex features are required:

- Simulation of **multi-processor architecture,**
- **SW Development tool ►System Development Tool,**
- Injection of failures (internal/external RAMs,registers,…).

MicroProcessor Roadmap

With reference to the four routes/product lines defined in the **Round Table on Next Generation Microprocessors held at Estec on 11-13 September 2006**,

- **Route A**: a processor for data handling/data processing computers (presented in session 1 of this round table),

- **Route B**: a very high performance DSP. A round table dedicated to the Next Generation DSP has been organized as part of ADCSS07,

- **Route C**: COTS processors. The need of a harmonized approach to the use of COTS was highlighted,

- **Route D**: Microcontrollers (session 1 of this round table).

in this section we'll focus on on-going developments in Route B (with a set of a dedicated presentations) and Route C (1 presentation).

Furthermore some examples of development of microcontrollers for specific applications will be presented (1 presentation).

COTS

ESA has initiated in 2007 an activity (funded by TRP and GSTP programs) for the study of the use of **COTS based computers** in space. Several examples of computer architectures based on COTS have already flown (BIRD by DLR, DEMETER by CNES), are flying nowadays (e.g. ATV fault computer) or are under development.

Several reasons are behind the choice to investigate the use of COTS in space:

- **high computing performance** achievable with embedded/industrial solutions (especially for **High Performance Digital Signal Processing** applications)
- Their reduced procurement time (if true…) could be a plus in a trade off for the selection of the building blocks of an architecture (if **supervisory/mitigation techniques** can be implemented at system/board level)

Which are the targets of the **COTS based computers** activity ?

- definition of a process of proper selection of COTS parts,
- design of architectures based on them,
- estimation of performances in term of processing power, robustness w.r.t the space environment, availability and reliability,...,
- validation of prototypes (3 different computer architectures: Hi-R,Hi-V and Hi-P).

A dedicated presentation will follow.

COTS

Other activities have been initiated or are going to be initiated:

T201-002ED: Digital Latch Up and functional protection for COTS memories in space

Expected release date: Dec.09

Objective of the activity is to design and test an IP Core that allows data access to memory banks with the extra functionality of SEU/SEFI/microLATCH-up protection and redundancy techniques for current and near future generation of memories.

The IP core shall be tested using commercial FPGA technology and commercial SRAMs and/or FLASH, but taking into consideration its future space use in rad hard OTP FPGAs or ASICs, also as a possible protection module for SRAM-based reprogrammable FPGAs.

High Performance Payload Digital Signal Processor (HPPDSP) to support science missions.

KO end 2009

µControllers

µControllers are used in commercial and space applications not only as sort of "small" microprocessor (e.g. for power distribution systems) but quite often as a central core of **mechanisms control and control loops units**.

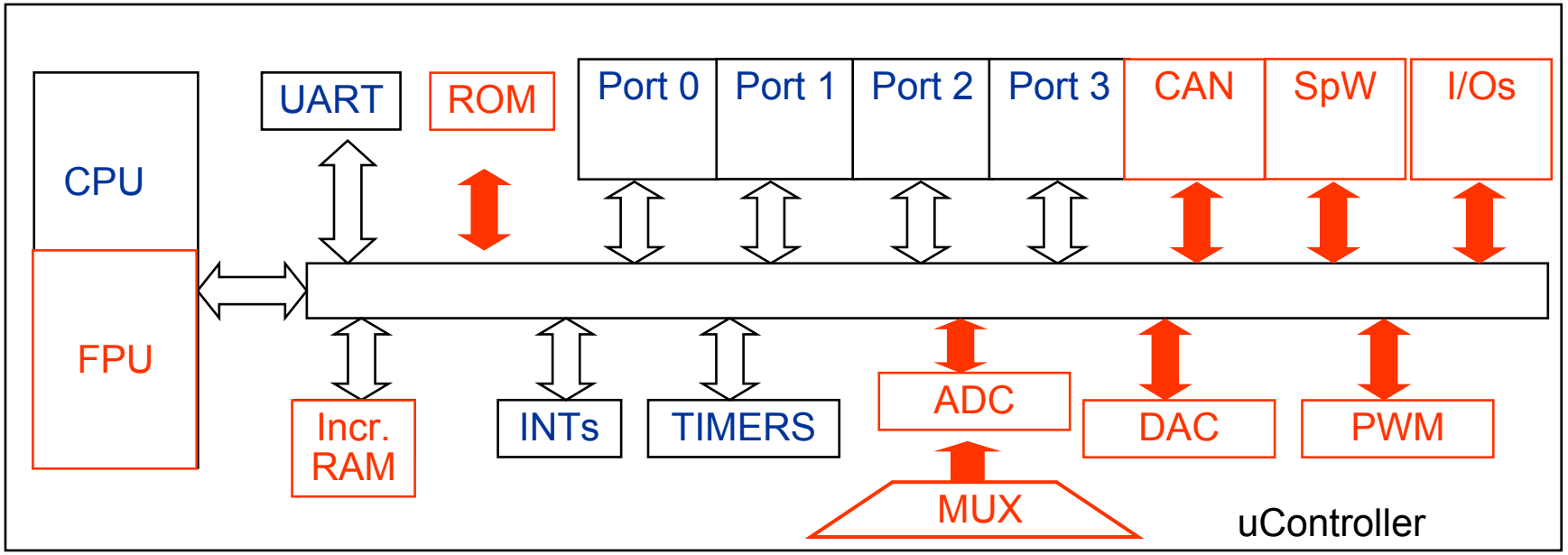
The availability of space µControllers allows to implement **software based control architectures** that give a higher flexibility w.r.t pure hardware solutions during the design phase: a microprocessor can provide a **local autonomous capability of monitoring and adaptation** to situations not completely predictable.

To be used in these specific types of applications some extra features have to be included:

- FPU (e.g. for Thruster control),
- PWM controller (e.g. for BLDC motors),
- On Chip Memory (ROM,RAM),
- ADC/DAC,
- General Purpose I/Os,
- Integrated Serial I/Fs (for an Highly Integrated Control Unit),
- Small Package,
- Low Power or Extremely Low Power Consumption,

….

Architecture: from a standard µController to a …



µController

Some solutions covering specific applications:

Development of a **Control Loop Processor** as standard product by S.A.B.C.A.

- See a dedicated presentation in this session

Motion Control Chip (MCC) The objective of this TRP activity initiated by TEC-MMA in 2008 is the development and the validation of a Motion Control Chip for the control of brushless-brushed motors and piezoelectric vibrators.

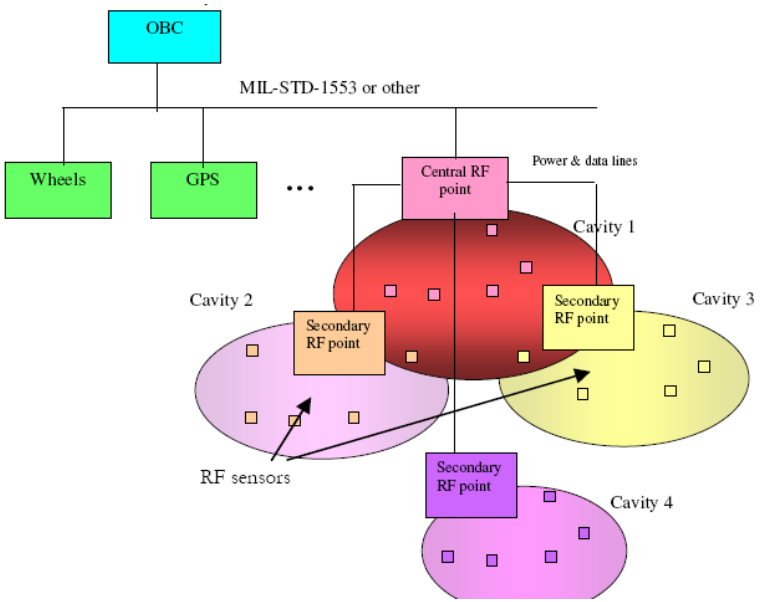
- Prime is AAC Microtec, Sweden. The other companies involved are : Selex Galileo, DLR, Aeroflex Gaisler, CSEM, and EADS Astrium-UK,
- The MCC is indeed more of a hybrid module than a pure integrated microcontroller chip,
- The microcontroller is implemented into an Actel 3ProAsic RT FPGA, using a LEON 3 FT IP core with 20MBit of SRAM (EDAC code included) The current FPGA implementation can be ported to an ASIC in the future,
- Interfaces with platform are: 28Vdc, and CAN (SpW as option)
- Potential applications are motion control units for rovers and drills,
- Control Loop Frequency: current = 10kHz, position, torque, speed = 1kHz *,
- Typical scenario is a distributed motion control system,
- Power consumption 2W stand-by, 5 W (driving a motor), Mass 80 g *.

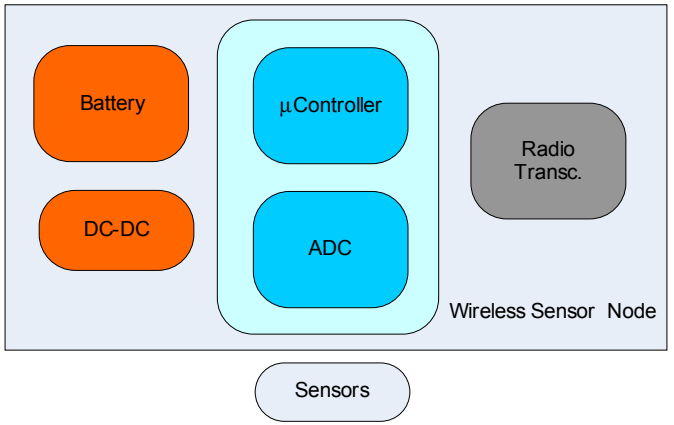
* Data from AAC Microtec AB

µController for Wireless appl.

ESA is defining a roadmap for use of wireless technology on spacecraft: **wireless sensor networking** for intra-spacecraft application is the first target of this roadmap.

A wireless sensor network will allow to acquire temperature, pressure, radiation, acceleration measurements.



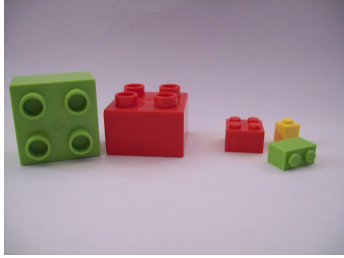


The µController will host the application SW and the SW part of the MAC layer of the Radio Transmission Protocol,

Extremely low power (< 0,1uA) in sleep mode (or powered off and waked up by the Radio Transceiver) and low power in active mode profiles are key features,

The availability of an Internal ROM/RAM would allow an high integration.

New Developments



The space market is following the consumer/industrial market: System on Chip, Multicore processor are already a reality but also deep submicron geometry and in the future Network on Chips are enabling technologies under development or analyzed

Deep Sub Micron (DSM) Asic Technology

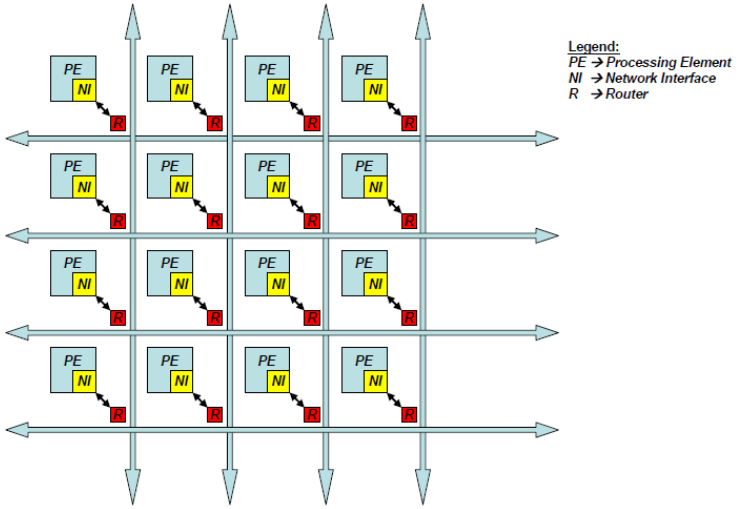
ST is the prime of an activity that has the following goals (KO Feb.2008,end 1Q 2010) :

- Refinement of requirements coming from Agencies (ESA, CNES) and primes (Astrium, TAS)
- Analyse the capability in term of reliability and radiation tolerance of an 65nm process for a space application .
- High pin count flip chip package assessment (800 …1000 pins)
- Future ASIC platform definition (structured ASIC / metal customizable)
- 6.25 Gbps high speed serial link (HSSL) study →embedded within future ASIC platform:
  - Requirements refinement,
  - Architecture study,
  - Design,
  - Prototyping of a quad HSSL (electrical, radiation, reliability)→aggregated data rate 25 Gbps

ESA reference: Laurent.Hili@esa.int

New Dev.

Networks on Chip (NoC*)



ESA and CNES (L. Hili / P. Perdu) have organized a round table on Network on Chip on the 17th and 18th September 2009.

NoC (elementary processing cores organized in 2-D or 3-D geometry connected together by neworks) could represent the natural evolution of a SoC considering the following trends:

- Increase of the **number** and **complexity** of needed **embedded functionalities,**
- **Shrinking of the silicon technology** and increase of the clock frequency (MHz ► GHz),
- **delay of internal buses** is higher than the single cell/transistor propagation time

Facts:

- NoC could easily implement **dynamic reconfiguration schemes** and **redundancies** for the improvement of the reliability of an avionics system,
- **Internal routing** is faster than **external routing** (based on standard communication paths as PCB tracks or harness),
- The first **commercial applications** of NoCs have already appeared on the commercial market. (mobile phone OMAP platform ► Texas Instruments).

What we need:

- Development and validated simulation tools that could allow the partitioning of the tasks among the elementary processing cores.

* Presentations of the NoCs round table are available at http://conferences.esa.int/01C25/NoC/

MPSA- Session 3 : agenda

14:00	14:40	HW & New related technology developments	ESA (G.Magistrati)
		SW & New related technology developments	ESA (K.Hjortnaes)
14:40	15:00	Next generation DSP roadmap and related ESA activities	ESA (R.Trautner)
15:00	15:15	SHARC(TM) Digital Signal Processor Core Technology and the Flexibility to Use for Custom Integration	ADI (A.Balivada S.Simha)
15:15	15:30	Possibilities for NGDSP implementation based on ATMEL DSP IP	ATMEL (G.Mantelet)
15:30	15:45	Texas Instruments COTS DSP chips for space applications	TI (Y.Tsikouris -Willgers)
15:45	16:05	High integration Digital Control Module- Control Loop Processor	SABCA (M.Ruiz)
16:05	16:20	Coffee Break	
16:20	16:40	Use of Cots Processors in space	ESA (C.Monteleone)
16:40	17:30	Round Table & Summary of the Workshop	All