ESA ADCSS '09
Astrium Microprocessors landscape

November 4th, 2009

All the space you need

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Astrium microprocessors landscape

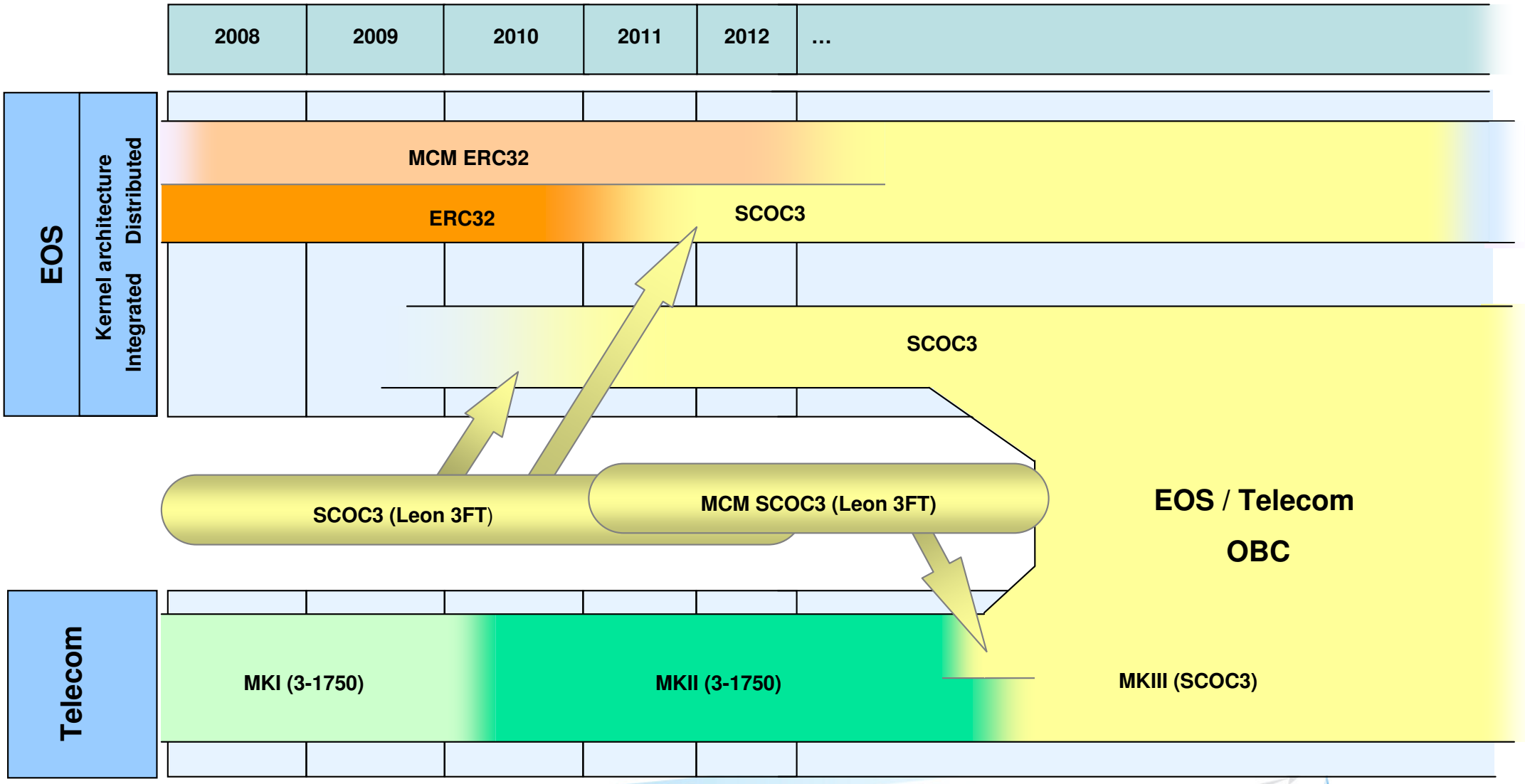
- Astrium has a substantial and large scale experience in the design, development and MAIT of On Board Computers and Microprocessors for space applications (satellites, manned missions, transfer vehicles, probes,…)

- Astrium is currently developping a new generation of integrated microprocessors based on LEON IPs:
  - SCoC3 based on LEON3FT, dedicated to Platform applications,
  - MDPA based on LEON2FT, dedicated to Payload applications

  ↳ These two processors are already selected for several satellite applications

- Astrium is also developping a high performant new generation computer for Orbital Infrastructures

Satellites Platform On Board Computer Roadmap



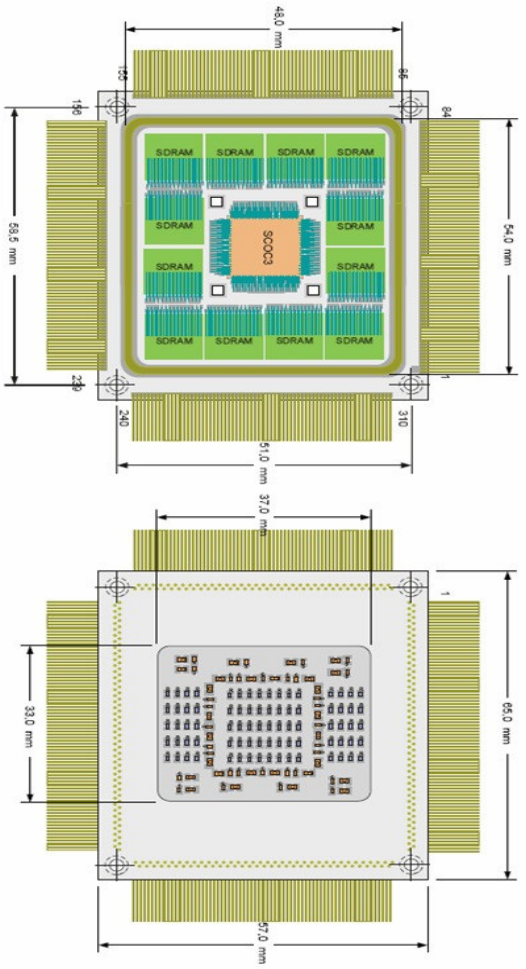
SCoC3 Computer

- OSCAR (**O**ptimized **S**pace **C**omputer **A**rchitecture with **R**econfigurable LEON3)
  - Volume 250 x 150 x 216 mm^3
  - Selected for Astroterra and Seosat
  - Based on SCOC3, ADT822 (Transceiver 1553 – ESA contract)
  - Evolution will be to go to quality level 1 (QML-V) applications (e.g. telecom)

Integrated solutions based on SCoC3: MCM

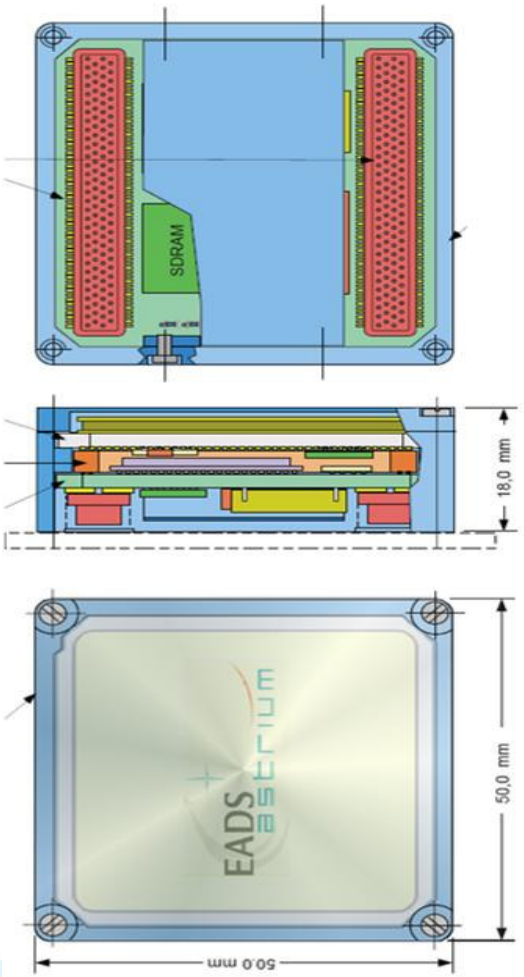
- MCM (Multi Chip Module)
  - Integrated system with memories
  - MCM technology enable to deliver quality level 1 (QML-V) part as well as quality level 2 (QML-Q)
  - CQFP package
  - ASTRIUM European manufacturer
  - *Example:* SCORPIO (CNES supported development)
    - ▶ SCoC3
    - ▶ 512 Mbytes protected processor memory
    - ▶ 512 Mbytes protected I/O memory
    - ▶ 370 CQFP package

  Manufacturing files ready



Integrated solutions based on SCoC3: SIP

- SIP (System In Package)
  - Integrated system with Alumina MCM (dice and small packages) + PCB (plastic or ceramic parts)
  - QML-V or QML-Q quality level
  - Very small (50*50*18 mm^3)
  - Fits with a full system (e.g. SCOC3, memories, large FPGA, point of loads supply, oscillators)



Computers road-map – SCOC3 new generation

SCOC3_NG:

For mid-term, taking benefit of DSM technology and larger pin number package

- keep SCOC3 architecture, current functions and I/Os interfaces
- add new functions due to various evolutions (parts, I/Os evolutions…)

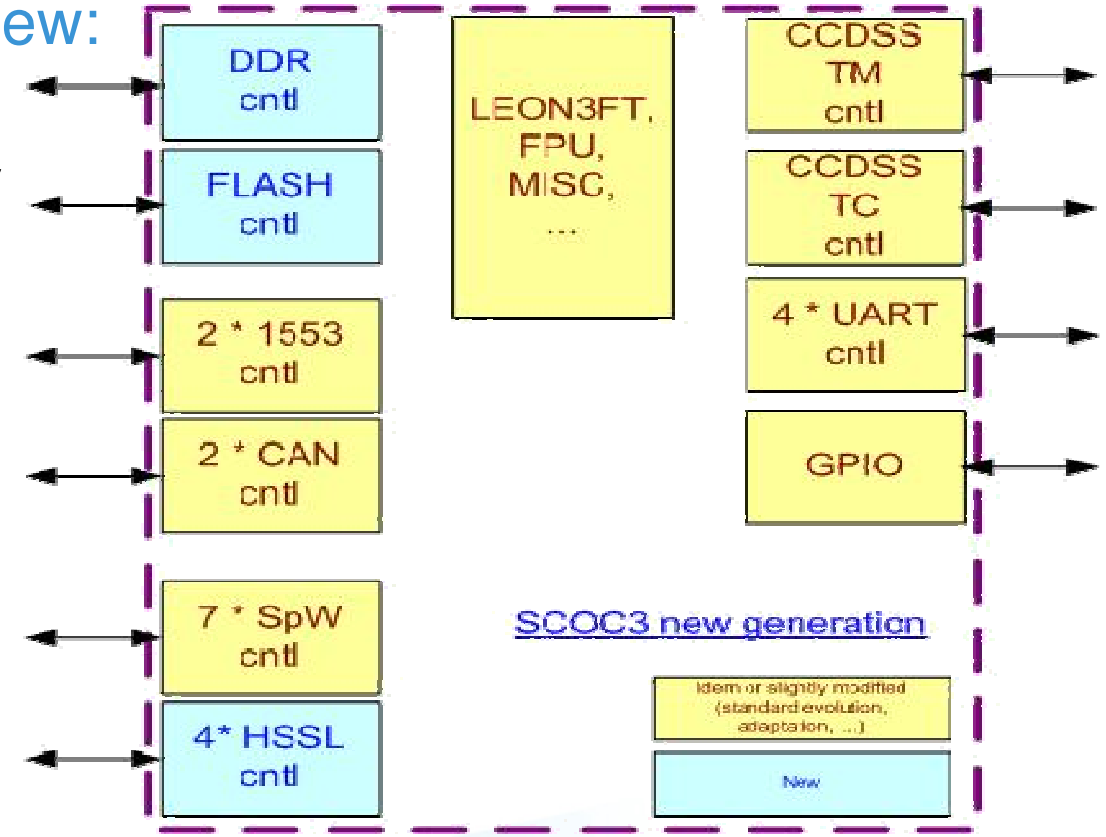
- Parts Evolution/Obsolescence management
  - Improvement of SDRAM controller to DDR2 or DDR3
    - DDR controller
  - Improvement of EEPROM to FLASH
    - FLASH controller
  - As a consequence, increase of memory data traffic (processor and I/Os)
    - AMBA traffic increase, new memory controllers, new or improved DMA controller, improved AMBA bridges

Computers road-map – SCOC3 new generation

- I/Os evolution
  - Perform I/O transfers on high speed serial buses
    - Implementation of HSSL links (PCI express 2.4 Gbps or more with several links)
  - Perform high speed I/O transfers with a European ATMEL FPGA companion
    - Implementation of HSSL links (PCI express 2.4 Gbps or more with several links)
  - Increase global I/O transfers performances
    - Improve AMBA traffic, memory controller, DMA controller, AMBA bridges
  - Increase of CGA package pin numbers

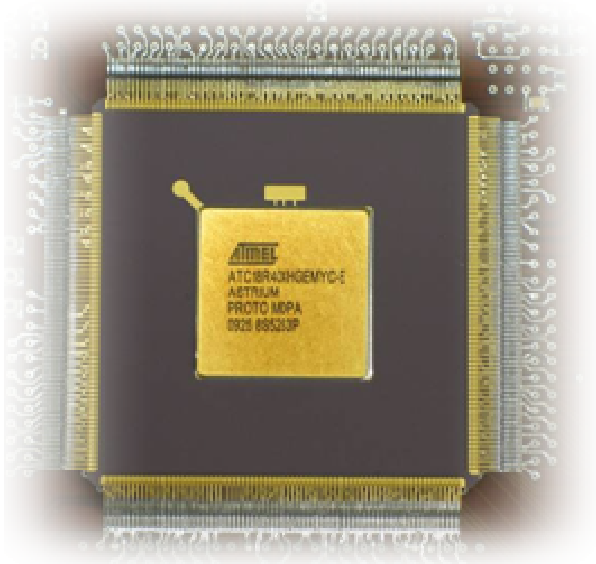
Computers road-map – SCOC3 new generation

- SCOC3 new generation overview:
  - Keep all SCOC3 functions
  - Make them evolving if necessary (yellow)
  - Add new functions (blue)



MultiDSP/µProcessor Architecture (MDPA) ASIC

- LEON2FT based System-on-Chip (SoC) operating at up to 80MHz; factor 5 of ERC32 performance (Hartstone benchmark)
- First SoC with SpaceWire router (path addressing) on-chip with 8 SpaceWire links operating at up to 200Mbps
- Further on-Chip features:
  - IEEE- 754 Floating Point Unit (Meiko)
  - 2 MilBus 1553 Controllers (Astrium SAS IP)
  - 1 CAN bus 2.0 Controller (ESA IP)
  - 2 UARTs
  - Modem based on DVB-S standard protocol (Astrium Ltd IP)
  - RMAP client compatible SpaceWire link
  - Debug Support Unit and Service interface
  - Watchdog, Timing functions
- Technology: Atmel ATC18RHA
- Package: CQFP352
- Testing according to QML-Q and QML-V



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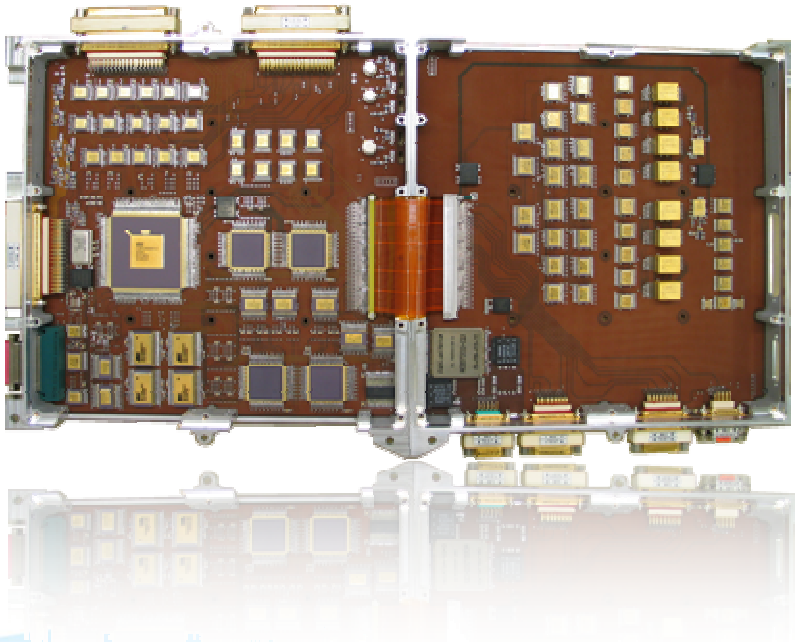
AlphaSAT Payload Controller with MDPA

- MDPA receives mobile communication requests and configures on-board switch subsystem accordingly
- Network Control Channel is regenerated by on-chip modem
- On-Board Switch connected via 8 SpaceWire links using RMAP protocol
- Spacecraft I/F: MilBus 1553 RT
- 16 Mbyte SRAM working memory, 2x 4Mbyte EEPROM, 64KByte PROM capacity
- 15 years GEO orbit operation
- PFM unit delivery: May 2010



Next Generation Mass Memory Supervisor using MDPA

- MDPA based controller and file system manager for next generation flash, SDRAM or DDR-RAM based mass memories
- Supports MilBus, CAN, UART or SpaceWire external interfaces
- Internal 16bit wide parallel memory module interface
- Main advantages over ERC32:
  - Higher performance by factor 5
  - Highly integrated , lower power (3.5W for board @40MHz)
  - More sophisticated test interface (direct register/memory access via DSU; watchpoints, Breakpoints, single step, etc)

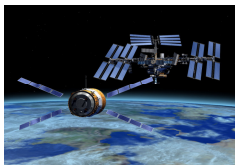
MDPA

Commercialisation

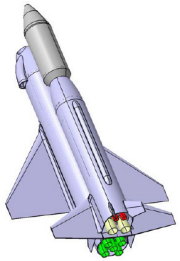
- The MDPA chip can be made available to interested parties on case by case basis
- The MDPA chip is in particular interesting for projects, which require
  - State-of-the-art assembly methods (Quad flat pack)
  - SpaceWire router integrated with LEON2FT processor; SpaceWire links can be multiplexed for cold redundancy operation
  - RMAP support on SpaceWire links
- The following software tools are available:
  - Boot strap
  - Low level Software routines according to ECSS-E40
  - Debug Support Unit Monitor (e.g. from Aeroflex Gaisler)
  - Service Interface box (USB interface) with host tools for software download, monitoring, task level debugging and task timing tool
  - MDPA simulator

Astrium ST's Computer Mission

- Astrium Space Transportation provides expertise in building modular, scaleable, high reliable and high available computers for
  - Space Infra-Structure applications (e.g. ISS Control & Payload-computer, ATV Control, X-38)



  - Future Launcher applications



  - Exploration applications (e.g. Moon-Lander, DEOS)

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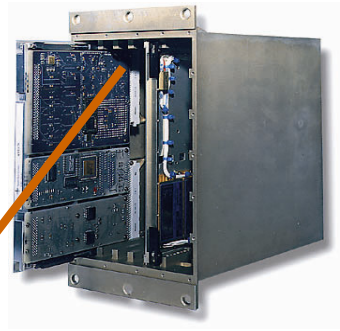
Definition of Computer Classes

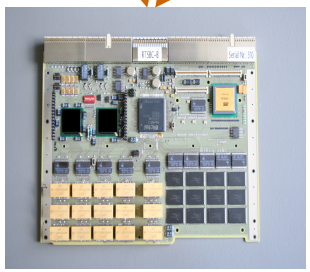
- Specification according Harvard Research Group:

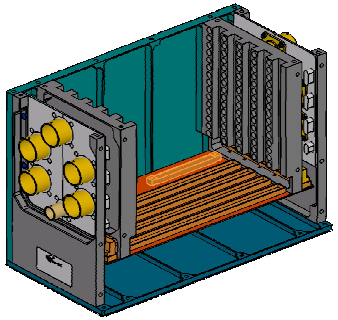
HRG Level	Description	Definition	Supported by Astrium ST
AEC-0	Conventional	Operation can be interrupted any time Data Integrity is not ensured	√: e.Cube P/L computer, 2nd level P/L CRTL
AEC-1	High Reliable	Operation can be interrupted Data integrity has to be ensured	√ : SPLC/SPAICE OBC and payload (P/L) computer
AEC-2	High Available	Operation interrupted only in a defined time frame Data integrity has to be ensured	√ : HiV COTS/SPAICE OBC and payload computer
AEC-3	High Resilient	Operation has to be guaranteed in a defined time frame Data integrity has to be ensured	√ : HiV OTS/FTC/SPAICE OBC for manned and critical missions
AEC-4	Fault Tolerant	Operation has to be guaranteed 24h a day/7 days a week Data integrity has to be ensured	√ : FTC/SPAICE OBC for manned and critical missions
AEC-5	Disaster Tolerant	Operation has to be guaranteed under all circumstances Data integrity has to be ensured	

Note: AEC= **A**vailability **E**nvironment **C**lassification

Astrium ST products vs. used CPUs (1)

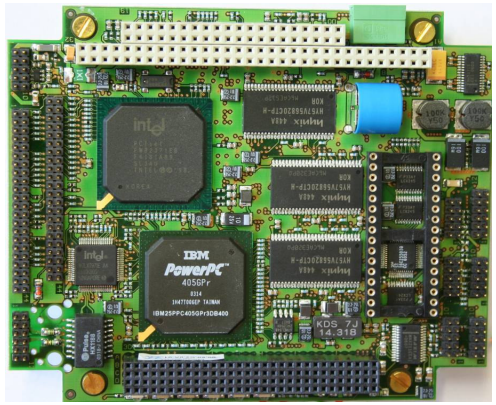




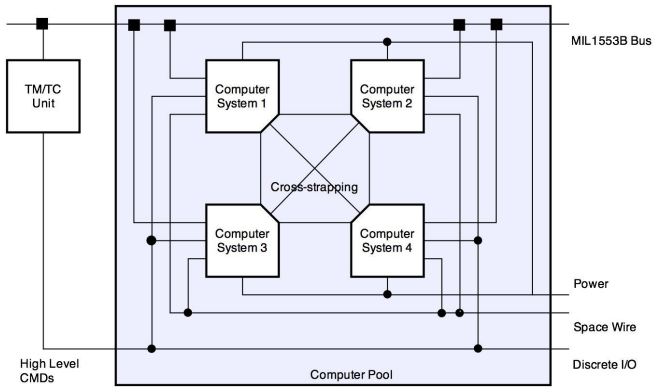


- FTC: ATV and ISS fault tolerant control computer, OBC for future launchers
  - ERC32, 3 chip version@16MHz
- SPLC: ISS rack and P/L control computer
  - ERC32, 3 chip version@16MHz
  - ERC32 SC@20MHz
- SPAICE: High performant successor of SPLC and FTC, space proven on ISS
  - LEON2 chip version@100MHz

Astrium ST products vs. used CPUs (2)



- e.Cube: space proven(vacuum), radiation characterized COTS com-puter for ISS, Shuttle and scientific rocket P/L/ and 2nd level P/L
  - PPC40x, 600 DMIPS@400MHz



- HiV: ESA study of a high available computer using COTS
  - LEON2 compatibility, PPC40x
  - 200 MIPS requested

Future need of CPUs and micro-controllers

- CPU candidates: LEONx, PowerPC, ARMx/CORTEX, ATOM(?!)
  - >(100MIPS / 25 MFLOPS)
  - Including: integer-, floating point- and memory management unit, cache, EDAC, SDRAM I/F
  - Parallel bus interface (e.g. PCI)
- Micro Controller candidates: 80xx, ATMEGA
  - Fully qualified, 8 bit micro-controller, high performance (10 MIPS)
  - Integrated FLASH, RAM and periphery (e.g. ADC, CAN bus…)
- Radiation Hard (or Tolerant)
- Availability of qualifiable RTOS
- Presence of large user forums for H/W and OS
- Readiness for High Language auto-coded GNC algorithms

Synthesis

- SCoC3 is the cornerstone of Astrium satellites computer road-map
- Astrium has the willingness to continuously improve this building-block by adding new functions and proposing integrated solutions based on SCoC3 (SIP, MCM)
- MDPA provides an integrated System-on-Chip solution for payload applications with high processing performance and standard interfaces to spacecraft and payload subsystems
- Astrium ST for Orbital Infrastructures computers (conventional, high availability, fault tolerant) is considering utilisation of standard building blocks which could meet future customer needs and continues to evaluate state-of-the-art technology