SHARC™ Digital Signal Processor Core Technology and the Flexibility to Use for Custom Integration

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Abstract

The SHARC™ Digital Signal Processor (DSP) has a very powerful core fully code compatible with the ADSP-21020, first generation of DSP Floating-Point processor. The current SHARC™ core allows multiple functions to be executed in parallel. It is based on a five stage instruction pipeline that scales well with deep sub-micron process technology. The core execution unit supports both SISD (Single Instruction Single Data) and SIMD (Single Instruction Multiple Data) modes of operation. This core is so designed that it can be used under a licensing model to allow it to be interfaced to custom peripherals and on-chip memory allowing the ability to create a customized DSP. This paper describes the core technology, the formal methodology used to design the core technology and the process technology used on one of its products that can be provided under license to ESA. It further describes the interface between the core and memory so that the memory can be customized as well. The core connects to a I/O bus that can be used to interface to various peripherals including custom peripherals. Design for Test (DFT) is also described in this paper. The paper also describes custom units and the tasks necessary to complete a fully integrated custom product.