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# TAS Experience and Development Strategy

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ADCSS 2009

Noordwijk, 4th November 2009

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  - Use of ERC32 and Leon in current / near future programmes
  - Expected advantages from NGMP
  - Plan to prepare for NGMP deployment

- **PAYLOAD DATA PROCESSING PERSPECTIVE (OPTICAL PAYLOADS, SAR, ALTIMETER)**
  - Use of TMS21020 in current / near future programmes
  - Overview of near future required processing performances
  - Review of NGDSP options
  - Approach to fill the Gap to NGDSP availability

- **SOME RUNNING DEVELOPMENTS**
  - DST ASIC flexible platform for TXP application
  - A fully reconfigurable OBP Processor based on FPGA
  - COTS Based Spaceborne Computers

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# PLATFORM DATA MANAGEMENT

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## Current application of ERC32 in TAS:

- Platform Computers for:
  - LEO platforms, as Sentinels, Export LEO
  - GEO platforms
  - EXM orbiter
- Other Equipments:
  - COSMO SAR Antenna Controller
  - Mass Memories
  - Cripto/Decrypto Units
  - Direction of Arrival Processor For Antenna Nulling System for Sicral 1B

## Programmes / Units where it is foreseen to use LEON2 (SOC or AT697F)

- EXM Descent Module and Rover Module
  - Increase of CPU and RAM capacity
- EXM RDA (Radar Doppler Altimeter)
- MTG
  - Increase of CPU and RAM capacity
- Next Observation Missions (2015/2020 horizon), as Sentinel follow-on
- Next Science Missions (2015/2020 horizon), as Cosmic vision
  - Obsolescence and CPU and RAM capacity increase trends.

**ERC32 based solution fulfil most of the PF needs. Transition to LEON2 will be driven by specific applications as MTG and EXM Rover.**

**TAS has already prepared transition to LEON2 PF, by running and checking its software on LEON boards. This is considered as no risk.**

## Transition to NGMP for PF processing

- Multicore
  - Multicore processor offers HW solution for segregate solutions
    - Clear splits between applications
    - Dedicate one processor to low level applications (communications, eqpt interface)
  - Direct impact on the global architecture
    - Function distribution
    - Possibility to introduce in central processor, sensors data processing
- Mid/long term target.
- RAM access performance shall also be addressed, to able to reach high CPU performance

## Plan to prepare it : we have to work on

- Architecture : to take advantage of the architecture without compromising system and software safety, quality, planning, … trade-off between several architectures
- Tooling : with the objective of abstracting distribution complexity to system and software developer
  - Modelling, …
  - Compilers, properties verification, …
  - Convergence between time and space partitioning and multi-core supervisors

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# PAYLOAD PROCESSING

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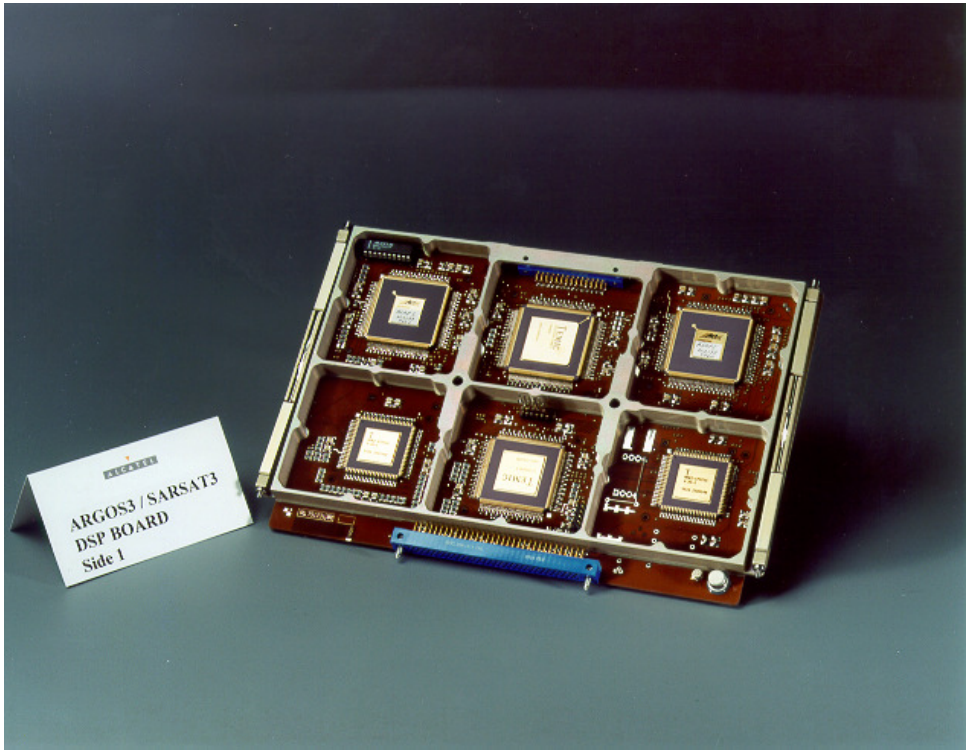
# Applications where it is still foreseen to use the TSC21020



## Current application of DSP21020 in TAS:

- RADAR digital processing units for altimetry and imagery.
- PDHT digital units.
- Antenna control units.
- For most of these applications the limited processing capabilities of the DSP shall be sustained by co-processing into ASIC or FPGA
- DSP21020 still foreseen for antenna control and for some altimetry missions.



# OPTICAL PAYLOADS, NEEDED PERFORMANCES ? (1/3)



***On board high power processing for Optical Payloads is a consequence of instrument high output data data rates combined with the need of on board processing at "pixel" level***

Some examples:

## ■Earth Observation Optical Payloads

- ✓ Instrument output data rate: ranges from few hundred of Mbps (for Medium Resolution 2m GSD and above) to several 10$^{th}$ of Gbps for very high resolution instruments (<<0,5m GSD)
- ✓ Type of processing to be performed on board dedicated to Compression: Pixel re-ordering, pixel equalization, Lossy or Lossless compression according to CCSDS 122-0. Algorithm with medium complexity.
- ✓ The instrument data rate must be combined with algorithms requiring up to 100 operations per pixel => power processing needs range from medium (few Gops) to very high (several several 100xGops).
- ✓ Large memory arrays needed
- ✓ NGDSP could be adequate for low / medium resolution, while only ASICs can provide the performances required for very high data rates, also in future.

# OPTICAL PAYLOADS, NEEDED PERFORMANCES (2/3)



## Spectro-imaging Optical Payloads

- ✓ Type of processing to be performed on board dedicated to Multispectral and Hyperspectral Compression: Pixel and spectral band re-ordering, pixel equalization, Lossy or Lossless compression according to CCSDS standard still under discussion in CCSDS working group. Algorithm with medium complexity.
- ✓ High instrument data rate due to large number of spectral bands (several hundreds)
- ✓ The instrument data rate must be combined with algorithms requiring up to 100 to 200 operations (TBC) per pixels
- ✓ Some Gops required. Implementation by ASIC but also a candidate for NGDSP.

## InfraRed Spectrometers (IRS)

- ✓ 2 Type of processing to be performed on board:
  - ✓ At detector frame rate: Optical Path Difference (OPD) measurement algorithm, re-sampling and decimation control, FIR filtering and Decimation
  - ✓ At pixel rate: detector non linearity correction (polynomial correction), ADC non linearity correction (look-up tables), band rejection for spike detection, re-sampling and filtering and Decimation, bit trimming lossless compression
- ✓ Instrument output data rates: range from 100 Mbps up to 3 Gbps depending on the IRS mission (MTG, Premier, IASI NG)
- ✓ Max required processing power: > 25000 FIR filters on more than 25000 pixels of more than 35000 samples in processing time < 9s
- ✓ Some Gops required. Implementation by ASIC but also a candidate for NGDSP.
- ✓ Memory for interferograms storage between two dwell times: > 28 Gbits

# OPTICAL PAYLOADS, NEEDED PERFORMANCES (3/3)



- **Cosmic vision programs**
  - ✓ PLATO
    - Windowing, Star intensity computation, barycentre location computation in each window
    - Nb of operation dependant upon nb of windows and assumptions on mission: Standard case with margins: processing power < 100 Mops
    - Need of approx 50 Mbits memory to store the windows associated to detected stars
  - ✓ EUCLID: CCSDS compression algorithm
    - Lossless compression
    - Processing power < 200 Mops with margins

Not so high as Earth Observation, but still exceeding Leon2. Also these are candidate for NGDSP application.

# RADAR ALTIMETERS – NEEDED PERFORMANCES



## Current Altimeters

- Current altimeter family implement a Low Resolution mode and a High Resolution mode
- The data of the High resolution mode and not processed on-board and are transmitted at a high date to the ground for processing
- Thus, the on-board processing (deramp processing) is the same for the two modes and is roughly limited to one 128-point FFT at a maximum rate of about 4 kHz.
- This processing is performed by one ASIC coupled with TMS21020 in charge of for low data rate processing (acquisition loop, tracking loop, formatting, etc…)

## Future Altimeters

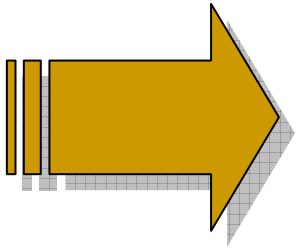
- For future altimeters, the data of the High Resolution mode will be processed on-board to reduce the instrument data rate
- Corresponding processing power is estimated to about 70 Mop/s
- This on-board processing is currently planned to be performed with 1 PowerFFT ASIC plus 1 µP LEON. Could be also a candidate for NGDSP use.

## Due to limited CPU power, On Board Processing is constrained to have:

- SAR Signal processing: only BAQ compression, implemented through dedicated ASICs
- Separated equipment for active antenna control

# New Generation Radar Digital Equipment

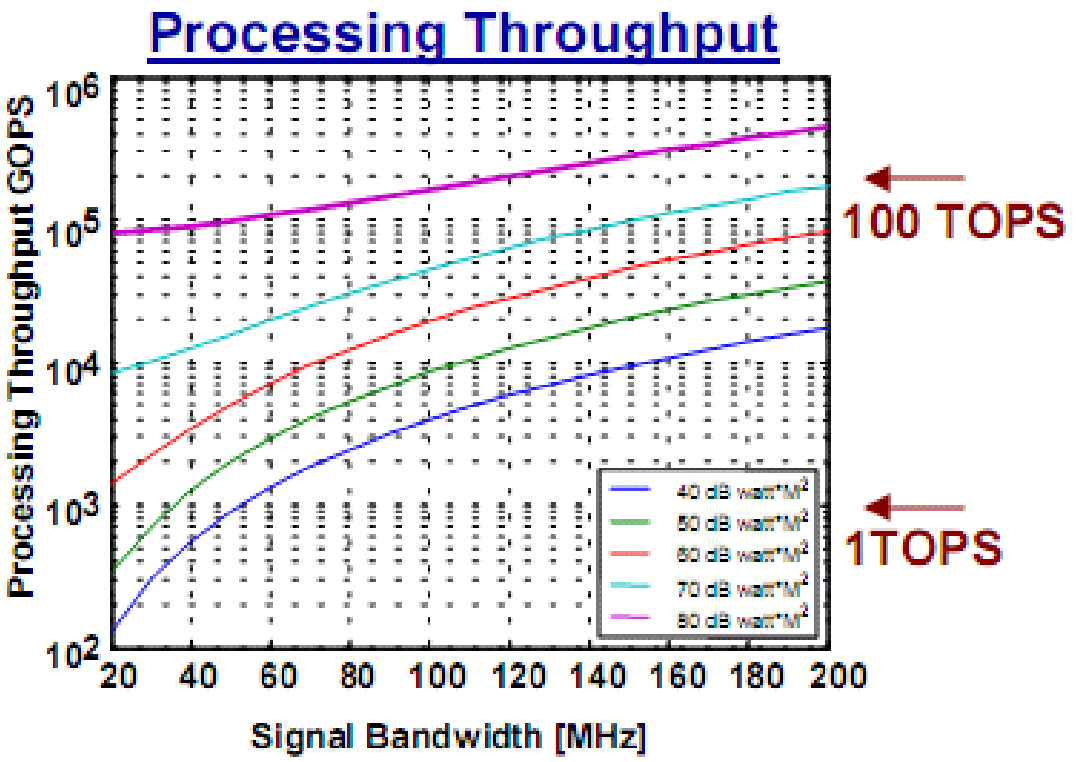
**What is expected From New Gen Digital Equipment ?**



- **Radar Command & Control**
- **Data Handling**
- **Near-real time Processing**
- **Active Antenna Improved Control**

# Needs for On Board Signal Processing

- Real-time or near real-time operations
- Wider signal bandwidth required for target discrimination
- Multi-channel operations (quad-pol, multi-beam,….)
- On-board processing required due to limited datalink bandwidth
- Processor must operate in radiation environment ➔ fault tolerance




**Space Time Adaptive Processing case**

**Apart from Tera Ops range,**
**demand for 100 to 1000 Mega Ops Radar Processors requires significant computer ARCHITECTURE and ALGORITHMS developments**

# Architecture



- **Architecture shall rely and be defined on radar algorithm data flow**

- **Mainly, it shall cope with:**
  - Algorithms which can be split through a function flow;
  - Computing power has to be distributed “on-line” as per different operative modes;
  - Cases where computing power is defined “a priori”; therefore it is important to exploit the upgrading capabilities of the processor to add new functionalities.

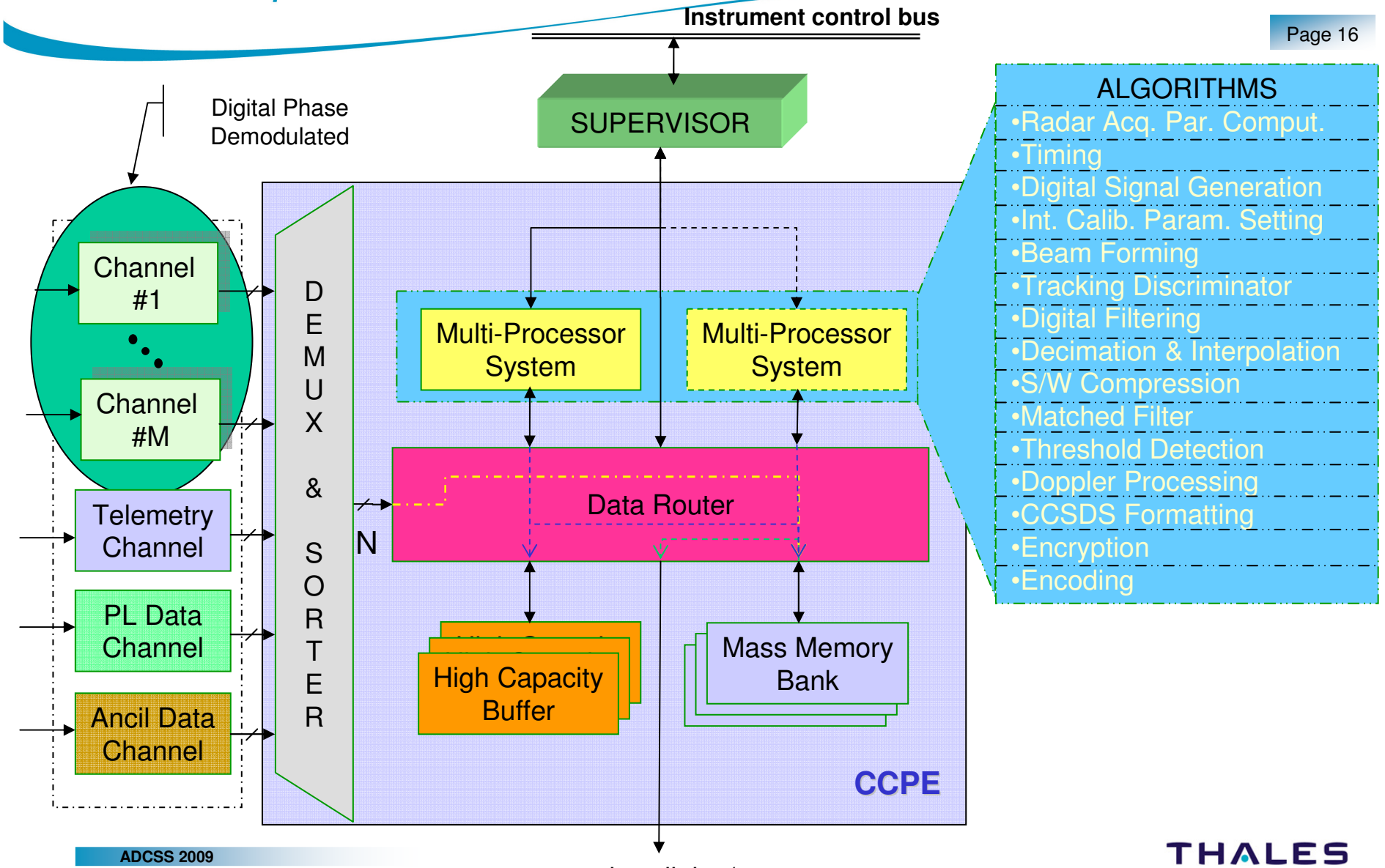
- **It has to allow the optimal resource allocation taking into account load and capabilities.**

- **It has to be modular and scalable**

- **S/W has to be layered among:**
  - Control system module ( layered among drivers of different boards)
  - High level modules implementing radar functionalities.

# Advanced Radar Processing Architecture Block Diagram





# Summary of needed processing characteristics and performances



- Wide range of applications, with different architectures, algorithms and performance needs
- Processing Power ranging between a hundred of Mops to thousand of Gops
- All at limit or exceeding Leon2 capabilities
- Only ASICs can cope with highest performance needs
- A wide range of applications, up to Gops class, could be covered by availability of a powerful NGDSP.

# NGDSP – expected advantages



NGDSP from ESA will allow:

- to combine:
  - the need of flexible architectures required by the very wide range of payload for space applications
  - and the need of high processing power for the most of the missions
- to enhance the re-use of standard hardware
- bring flexibility in the processing
- shorten the development plans

# NGDSP Development Options



- Reconfigurable DSP core arrays may not be suited for cameras/payloads with reduced complexity (high power consumption, ASIC implementation,…). Maturity and tools also to be considered
- Standard heterogeneous multi-core (Leon2+DSP): suited for all type of payloads requirements, but not available today and needs ASIC implementation
- Radiation hardening and adaptation of an existing DSP: could be a solution, but also in this case long term expected
- Custom heterogeneous multicore on FPGA and ASICs: optimized for specific applications but lack of flexibility
- TI DSP (COTS derived, available at level V): high processing power, flexibility, low power consumption, mature software development environment, but multi-processor configurations and export status to must be addressed.
- COTS PowerPC: this alternative solution must be considered for the very demanding optical payloads

# Waiting for NGDSP



**Since DSPNG is not yet available, the following solutions must be considered to the different projects needs:**

- **Software implementation on available CPU (Leon)**
  - ✓ Adequate for processing performed at sensor frame rate
  - ✓ Adequate for payloads with reduced instrument output data rate
- **FPGA (coupled with CPU for control)**
  - ✓ May be compliant with project requirements pending the speed limit and the required number of gates
  - ✓ Export Licences constraints to be taken into account
  - ✓ Works on a very large reprogrammable space qualified FPGA should be supported with the highest priority in Europe
- **ASIC (coupled with CPU for control)**
  - ✓ Space qualified solutions available today in Europe (0,35µm and 0,18 µm). ATC18RHA from ATMEL qualified by TAS and already embedded in equipments developed by TAS (ex. Galileo IOV)
  - ✓ Well suited for very high speed computation and interfaces
  - ✓ Allow to reduce the number of components
  - ✓ Constraints vs. cost, flexibility and compatibility with complex algorithms
  - ✓ Availability in Europe of space qualified ASIC processes with multi-wafer project capabilities is essential for European space industry

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# RUNNING DEVELOPMENTS

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# Dual Standard Transponder ASIC platform based on Leon 2FT and programmable DSP processing blocks



**Fully flexible platform supporting TT&C functions for Near Earth, Deep Space and Spread-Spectrum (i.e. Secure) applications.**

**The DST ASIC is under development in the frame of BepiColombo program using the ATMEL MH1RT technology.**

- 1.8 Mgates
- CQFP 352 pins

**Sign off with ATMEL planned on January '10**

**SoC Design Build around AMBA Bus, all Blocks are connected to AHB and/or APB.**

**The LEON2 used for:**

- Control and monitor all DSP blocks and TC/TM functions
- Implement low-rate DSP algorithms (FFT based signal acquisition, signal-to-noise ratio estimation, lock detection)

**Specific DSP blocks are used for:**

- DDS (Direct Digital Synthesizer)
- PN (Pseudo Noise) Type Ranging Processing
- Carrier and Clock recovery
- …

# FULLY RECONFIGURABLE REGENERATIVE OBP (ESTEC Contract 20707/07/NL/AD) 1/2



## Objective:

- To define the architecture and to develop the prototype of a fully/partially reconfigurable regenerative OBP making use of SRAM-based FPGA
- To define a suitable reconfiguration procedure to perform the planned full and partial reconfigurations in an efficient, reliable and secure way

## Main Features:

- U/L Channel Processor (UCP): demultiplexing, demodulation and decoding of a multicarrier, DVB-RCS compliant input channel having a bandwidth of 36MHz
- The UCP is fully and partially reconfigurable; reconfiguration scenarios include: FEC code change (turbo/convolutional), traffic profile change (MPEG/ATM), signal processing algorithms upgrade/modification, adding of new capabilities
- D/L Channel Processor: formatting, coding and modulation of a QPSK/8PSK DVB-S2 compliant output channel.

# FULLY RECONFIGURABLE REGENERATIVE OBP (ESTEC Contract 20707/07/NL/AD) 2/2



## Prototype Implementation:

- Commercial boards (Sinplicity/Hardi) based on XILINX Virtex-4 FPGA plus daughter boards (same source) for ancillary functions

## Contract Status:

- Phase 1 completed at the end of March 2008
- Critical Design Review completed at the end of February 2009
- Final Review planned for 1Q/2010

# COTS BASED SPACEBORNE COMPUTERS (1/2)



TAS is involved in two ESA Contracts:

- COTS Based Spaceborne Computer – System Study (ESA Contract N°20726/08/NL/GLC):
  - Leaded by TAS-F
  - Subcontractors: TAS-I; RUAG Austrian
  - In charge of co-ordinating all the parallel contracts:
    - Hi-Rel COTS Based Computer
    - Hi-Available COTS Based Computer
    - Hi-Performance COTS Based Computer
    - COTS Based Computer Software
- Hi-Rel COTS Based Computer (ESA Contract N°21863/08/NL/GLC)
  - Leaded by TAS-I, with SME and Academic partners

## Hi-Rel COTS Based Computer

- First step of a project aiming at implementing and qualifying COTS based solutions available for operational use.
- Current work focusing on Computer architecture and fault mitigation features, and to establish their validation and the qualification approach
- COTS devices families have been analysed and candidates selected, focusing on:
  - Memories (Flash NAND, NOR, DDR2, …)
  - Reprogrammable FPGA's
  - Processors
- Expected behavior under radiation has been analyzed on available tests results and countermeaures identified
- A detailed model of the whole Hi-Rel Computer, has been developed, using Virtutech Simics, including CPU Instruction Set Simulator, TMTC, I/O and Reconfiguration module, and complemented by a fault injection support tool
- Selected Processor is PC7448, providing GPP characteristics and also high performance processing capabilities (suitable for various applications)
- A hardware model is foreseen to be produced in step2, along with a test environment supporting fault injection on hardware
- Transient faults effects and mitigation effectiveness will be verified by exploiting both simulated and hardware environments