PAST, PRESENT AND FUTURE MICROPROCESSOR NEEDS AT SYDERAL

SYDERAL SA, Neuenburgstrasse 7, 3238 Gals, Switzerland, www.syderal.ch

Microprocessors are key components in almost all equipments provided by Syderal. Allowing to run a specific application software for each equipment, they make possible to add intelligence and flexibility at the user interface level as well as to manage all internal functionalities and appropriately define the hardware-software interface.
Syderal equipments mainly consist of mass memories and payload controllers. In addition to high level user interface flexibility and intelligence, these equipments usually require data processing and data handling performance that cannot be accomplished by software due to microprocessor limitation in reaction time and speed. Therefore, specific FPGA based hardware is coded to fulfill high speed data processing and handling performance.

Processor module developments started by employing the MA 31750 which was able to provide 1 MIPS, then a step forward in performance has been achieved through the use of the DSP 21020 which allowed to reach 20 MIPS and 40 MFLOPS. Today the current processor module is based on the Leon 2 FT allowing to achieve 86 MIPS and 23 MFLOPS. This module is going to be employed in the ICM for the Sentinel-1 mission and the PDHU for the GAIA mission.

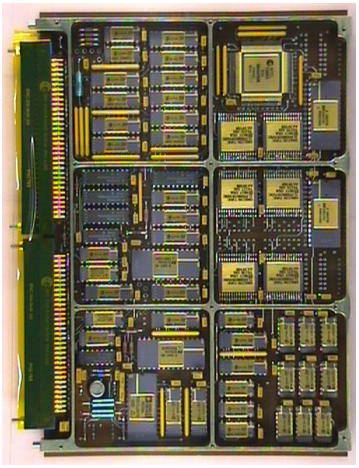

Figure 1 MA 31750 based module

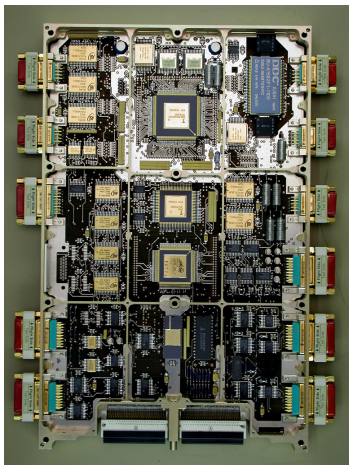

Figure 2 DSP 21020 based module

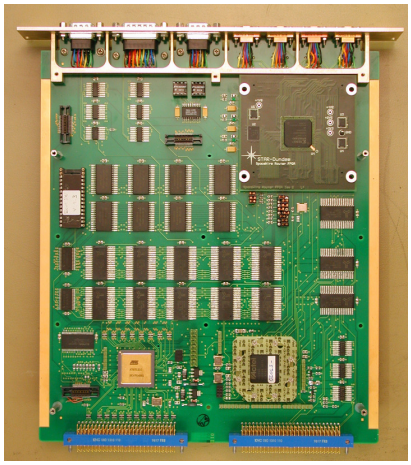

Figure 3 Leon 2 FT based module

Today the Leon 2 FT ASIC performance capability well fulfils our current need for both payload controllers and mass memories. Nevertheless, there is a concern for future availability of the version F of this ASIC. Additionally, the availability of a qualified operating system for this processor is a further need.

For future developments, it is envisaged that payload controllers might have the need for higher processing power capability in terms of MFLOPS with respect to the Leon 2 FT ASIC. Therefore, the availability of a more powerful alternative would be welcome.

Instead, future need for mass memory processing is towards small decentralized processing nodes allowing to give a software customizable interface to local hardware functions. As such complexity and flexibility could be better traded with performance. One way to achieve that could be by using microprocessor architectures based on the Leon FT core and customize them to meet specific interface requirements.