SpaceWire
Remote Terminal Controller

AT7913E

J. Ilstad
Onboard Payload Data Processing section (TEC-EDP)

ESA/ESTEC
**TEC-ED: Sections and association**

**Data Systems Division**  
**TEC-ED**  
Philippe ARMBRUSTER

- **On Board Computer & Data Handling Section**  
  **TEC-EDD**  
  Giorgio MAGISTRATI

- **Microelectronics Section**  
  **TEC-EDM**  
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- **On-Board Payload Data Processing Section**  
  **TEC-EDP**  
  Martin SUESS

- **On Board Communication Unit**  
  **TEC-EDS**  
  Chris TAYLOR

**Responsibilities:**  
Technical Officer SpW-RTC Development  
Support to payload processing developments  
Project support to ongoing missions  
SpaceWire Components Support
Overview

• Introduction
• ESA Strategy for Payload Developments
• SpW-RTC Description
• SpW-RTC and Onboard Data Handling
  – Application Areas
• Performances
• SpW-RTC Development Suites
• Usage in Missions
• Status and Availability
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**ESA strategy for payload developments**

- Development of **Application Specific Standard Products (ASSP)**
  - Devices capable of answering most onboard computing needs for the coming decade.

- Adopt upcoming ASIC developments to use **similar device architectures** based on **pre-validated ESA IP cores** for the purpose of reducing development time and recurring costs.

- Ensure SpW nodes developed by ESA to be **easily integrated** in ESA On-Board Distributed Computing and Control System.
SpW-RTC Description

Device
- SpW Remote Terminal Controller contains
  - Leon2 FT and FPU,
  - CAN-Bus (N&R selectable)
  - 2*SpW,
  - SRAM, FIFO, ADC, DAC, UART, Parallel etc. interfaces
- SpW link speeds 200MBit/s
- System-on-Chip for compact RT implementation
- SW can be uploaded via SpW link (RMAP compatible)
- Direct Memory and IO Access via SpW RMAP
- LGA 349
- Power consumption: \(~0.7W@50MHz~
- 1.8V core, 3.3V I/O
- RT CMOS Technology: **ATC18RHA** (0.18 µm)
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System on Chip Layout

- LEON2 FT IP core
- 64Kb On chip memory (EDAC)
- FIFO i/f (Parity check)
- JTAG i/f
- Memory Controller (EDAC)
- Memory mapped 24 bit GPIO
- Memory 24 bit GPIO
- 2 x UART Serial links
- 2 x UART Serial links
- 16 bit GPIO Prg I/O shared with IRQ and UARTs
- 2 x UART Serial links
- DSU Tracebuffer 512 lines 16bit
- Tracebuffer 512 lines 16bit
- ADC/ DAC i/f
- ADC/ DAC i/f
- AMBA BUS
- SRAM, (EE)PROM, Flash PROM

- LEON2 FT IP core
- 32 bit Timers
- DSU serial Link (UART)
- MUX
- Link 1
- Link 2
- Channel select
- On-Chip LVDS drivers
- SpW2 Core
- SpW Codec

- SpW2 Codec
- MUJ
- Memory mapped 24 bit GPIO
- Memory mapped 24 bit GPIO
- 2 x 32 bit Timers
- Memory mapped 24 bit GPIO
- Memory mapped 24 bit GPIO

- RUAG
  (SAAB Space)
  Developed IP core
- ESA
  Licensed IP cores
- Aeroflex
  Gaisler
  IP Cores

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Architecture

- 4 Kbyte I&D Cache
- 16 x 16 multiplier
- 8 register windows
- Radix 2 divider
- 5 Stage I-pipeline

Debug Support

- Memory Controller
- Debug Serial Link UART
- Debug Support Unit
- LEON2-FT SPARC V8 Integer Unit
- Integer Cache
- D-Cache
- AHB I/F
- AMBA AHB

Debug Support

- SRAM, PROM, EEPROM, FLASH-PROM
- RS232/422

Interrupts

- GPIO
- IRQ
- UARTs
- TIMERS
- AHB / APB bridge
- AMBA APB

DMA Transfers

- 32-bit Timers
- 24-bit General Purpose I/O
- ADC/DAC Ctrl I/F
- ADC/DAC
- ADC/DAC
- FIFO
- CAN Controller
- CAN
- Network
- SpaceWire
- Link
- SpaceWire
- Network
- On-Chip
- Memory
- AHB I/F
- AHB I/F
- AHB I/F
- AHB arbiter / decoder

EDAC functionality

- 24 GP I/Os
- 8 Pulse Generation lines
- 8/16 bit ADC/DAC
- Parity bits

EDAC functionality

- EDAC
- Functionality

EDAC functionality

- RMAP

ADCSS 2009

European Space Agency

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SpW-RTC and Onboard Data Handling

- Low/Med. Speed Bus: CAN
- High Speed Network: SpaceWire
- High Capacity Memory
- Telemetry Formatter/Encryption
- Data Compression
- SpW RTC
- Control Processor
- DSP Processor
- Instrument
- I/O Module (Optional)
- Router
- Component Level
- Board Level
- Spacecraft Control Bus
- Complex Instrument
- Inst. 1
- Inst. 2
- Inst. n
- V, I, T Acquisition (Monitor)
- Discrete Commands
- High Speed Network: SpaceWire
- Low/Med. Speed Bus: CAN
- SpW RTC
- Router
The SpW-RTC ASIC processor performance (@ 50MHz)

- **Dhrystone 2.1 benchmark**
  - 34.4 MIPS

- **Stanford benchmark**
  - 91 integer composite
  - 138 float composite

- **GNC benchmark**
  (68.6 million instructions, 16.6% present FP instructions):
  - 2.4 MFLOPS
Performances; Application Example

• Description of application:
  – executes **Dhrystone benchmark** via of chip SRAM
  – data transfers from **on-chip memory via loop backed SpaceWire links** (full duplex)
  – data transfers from **on-chip memory to external FIFO and back again**
  – 12bit value to **DAC and read back via ADC interface**
  – **GPIO pulse generation**
  – **CAN bus traffic** to external test equipment
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Performances; Application Example

- **GPIO Pulse generation:** 784 per second
- **DAC/ADC conversions:** 784 per second
- **ASIC Power Consumption:**
  - 342 mW (1.8V Core)
  - 230 mW (3.3V I/O)
  - 11.44 mW/MHz
- **FIFO throughput:** 295 Mbit/s, 1.35 clock per byte
- **Dhrystone Benchmark:** 27.9 MIPS (compared to 34.4 MIPS)
- **CAN communication:** 208 kbit/sec
- **SpaceWire loopback:** 587 Mbit/s (full duplex)
SpW-RTC Development Suites

Aeroflex Gaisler Products

Hardware
• ASIC Development board with housing and power supply
  – SpW-RTC prototype ASIC
  – RTEMS drivers for SpaceWire, CAN and FIFO
  – GRMON debug monitor

Software
• Bare-C compilation system (BCC)
• RTEMS – drivers and BSP
• Wind River VxWorks – drivers and BSP (sold separately)

Additional Tools
• GRESB – Ethernet SpaceWire bridge w. IP tunnel
• GRMON – debug monitor (debugging over RMAP)
• TSIM2 – instruction simulator with SpW-RTC loadable module
CAEN Aerospace / Aurelia Microelettronica Products

**Hardware**
- **A1493A** PCI-SpW/CAN
- **A1494** RTC Test-Bed

**Software**
- Linux based GUI control application.
- Uses SpaceWire RMAP to control, program and debug the SpW-RTC chip.

**Tools**
- Compatible with GRMON tool which can be obtained from Aeroflex Gaisler
Usage in Missions

• Implemented in Bepi Colombo instruments:
  – MERMAG
    • Magnetometer
  – SIMBO-SYS
    • Spectrometer and Imagers integrated package
• Solar Orbiter
  – Base lined for several instruments to form a common payload interface.
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Status and Availability

- Prototypes available W7 2009 (done)
- Prototype approval foreseen W12 2009 (done)
- AT7913E Atmel Standard Product (Q4 2009)
- Availability: EMs (early Q1 2010), FMs (Q3 2010)