High integration Digital Control Module, *Control Loop Processor*

HiDCM – CLP

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BACKGROUND (1/3)

S.A.B.C.A.

- **Scope: hard real-time control loops characterized by both**
  - Frequency higher than 1 kHz
  - Complex control algorithms needs
- **Today, no cost and technical effective solution available**
  - LEON: not deterministic due to cache
  - COTS DSP: ITAR sensitive, not space qualified
  - FPGA: expensive, ITAR restrictions, systematic redevelopment

BACKGROUND (2/3)

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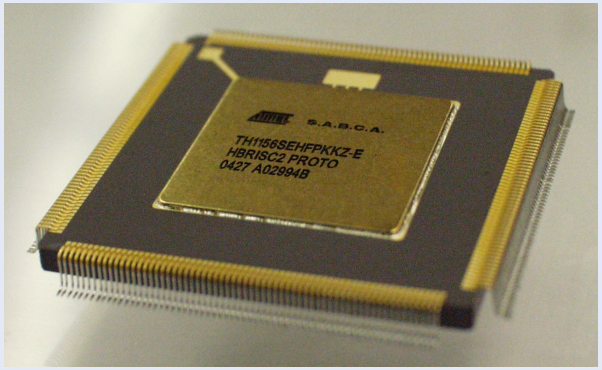
High Integration Digital Control Module
Control Loop Processor

- **Typical application:**
  Electrical actuation subsystems for space vehicles
  - 3 embedded control loops, fastest running @ 20 kHz
  - GSTP2-IMCM program led S.A.B.C.A. to harden existing proprietary BRISC processor (*HBRISC2*)



  - Core of the control electronics of each VEGA launcher TVC (S.A.B.C.A. core business)
  - Tomorrow evolution to more integrated solutions

BACKGROUND (3/3)

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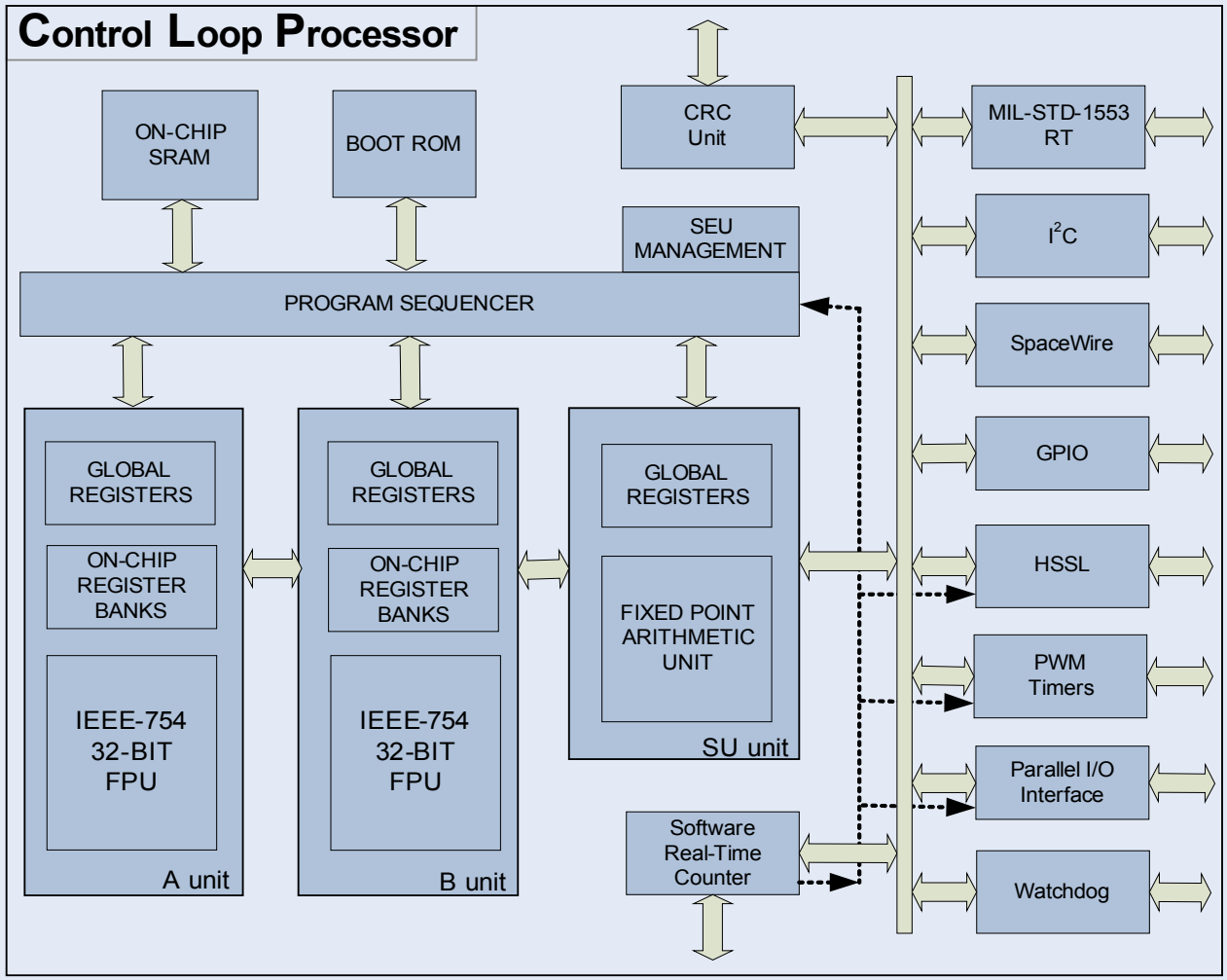
- ***Control Loop Processor*: from specific design to ASSP**
  - Based on HBRISC2 key features (cfr next slides)
  - Standardized to IEEE-754 format and spacecraft interfaces
- **Distinctive features w.r.t. current solutions:**
  - Fully predictable and uninterruptible architecture
  - Accessibility to general users (without skills in VLSI design)
  - Programmable, tailoring made with simple and OS-free SW
  - ITAR free

FEATURES (1/4)

S.A.B.C.A.

High Integration Digital Control Module
Control Loop Processor



FEATURES (2/4)

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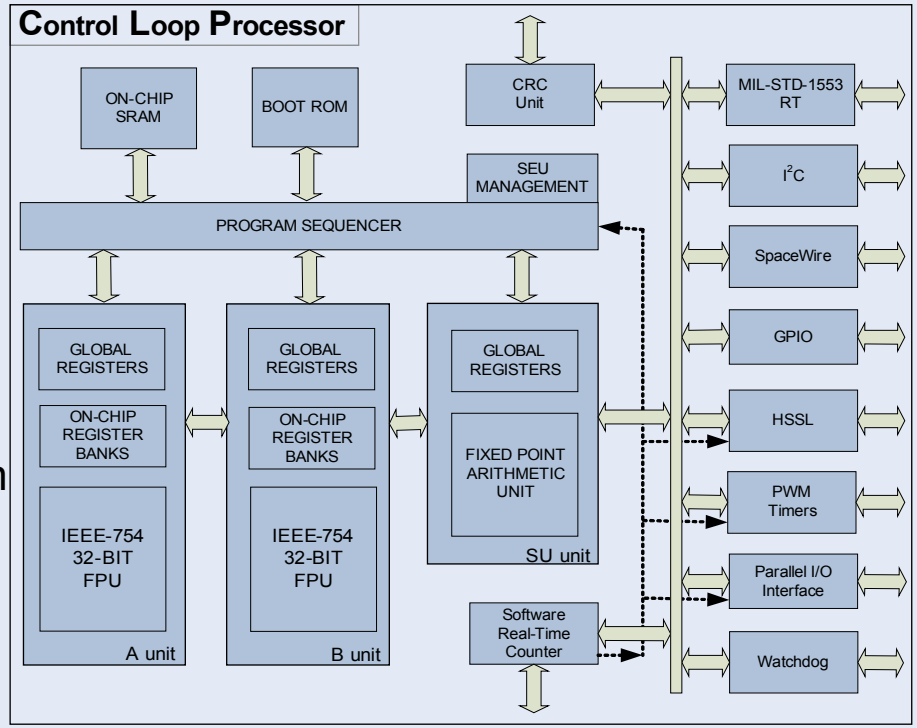
High Integration Digital Control Module
Control Loop Processor

- Standard product
- Cache-free, RISC machine, uninterruptible
  - Fully predictable CPU load
  - Easier SW validation
- Dual Floating-Point units
  - Exploit application parallelism
  - Support complex algorithms
- On-chip 1-Mbit SRAM
  - Holds program code only
- IEEE-754, 32-bit format, exception-free and saturating arithmetic
  - Handling of high dynamic data
  - Avoid fixed-point related issues (rescaling, overflow,…)
  - Safe behaviour



FEATURES (3/4)

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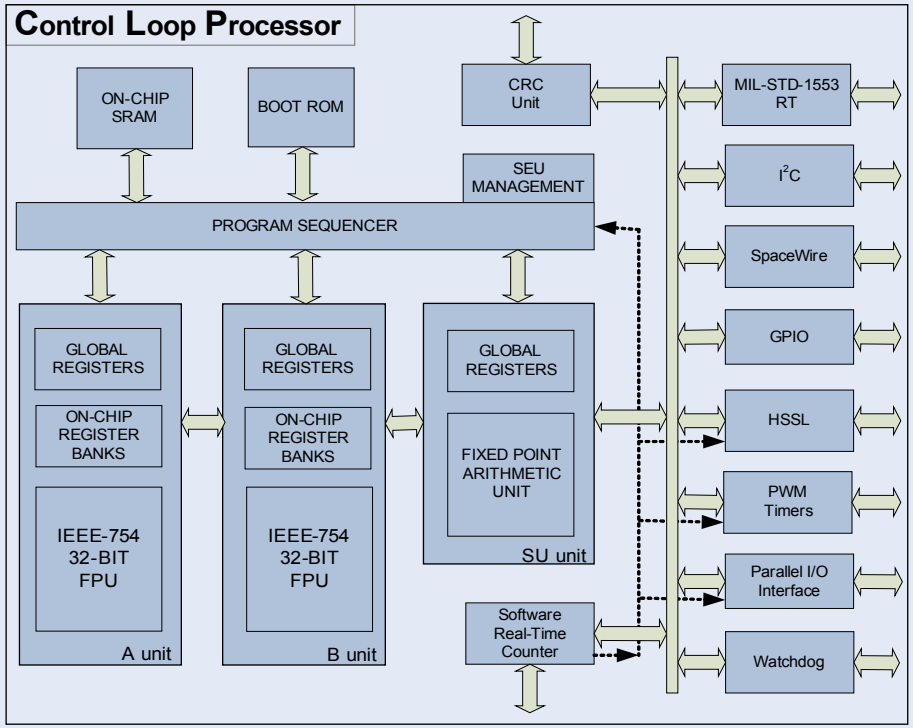
High Integration Digital Control Module
Control Loop Processor

- Full visibility at Simulink-level via real-time tracing
  - Easier SW validation
- On-chip 10-kbit memory data, organised in banks
  - Suppress SRAM access
  - Fast access
  - Double data fetch
- Automated SEU detection/correction
  - Transparent effect for SW



- Autonomous functions to support application interfaces
  - Automatic SRAM upload and CRC check via on-chip uploader (Boot ROM)
  - Access to external memory (RAM, EEPROM,…)
  - Embedded PWM generation, sensors excitation, ADC interface

FEATURES (4/4)

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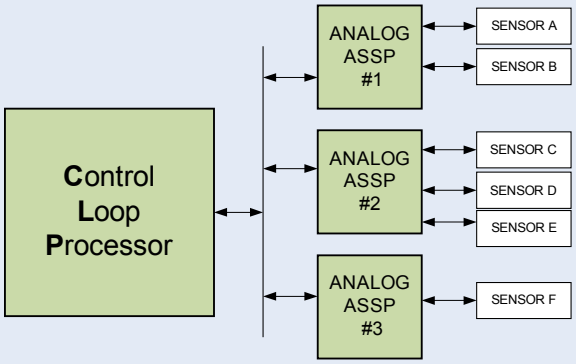
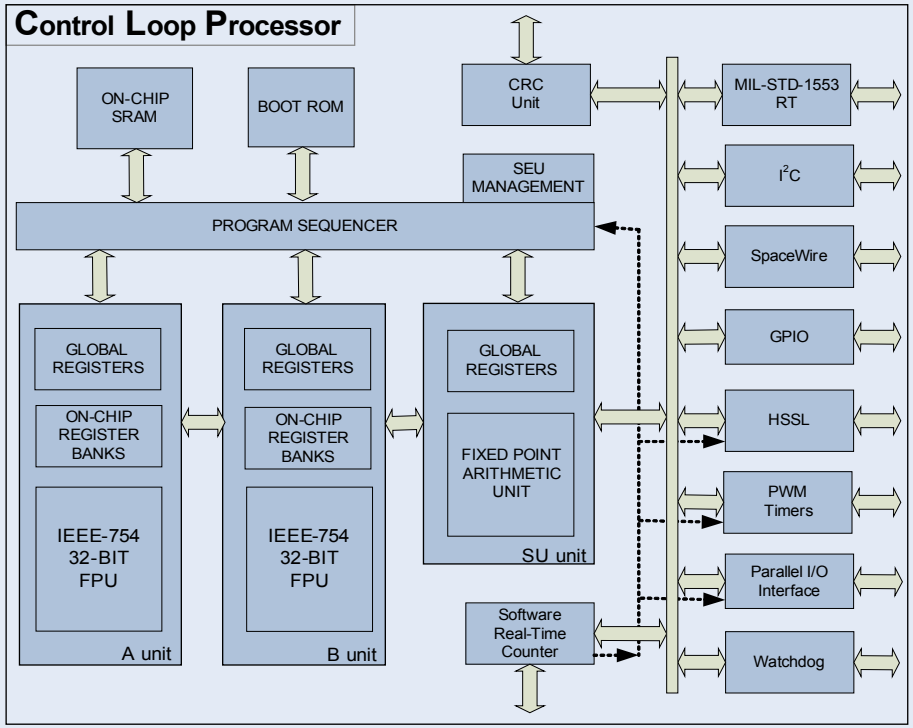
High Integration Digital Control Module
Control Loop Processor

- Real-time counter
  - Automatic SW/HW synchronisation
  - Predictable behaviour at board level
- Standard bus interfaces
  - Reduce glue logic
- Targeted performance
  - 50 MIPS/100 MFLOPS
  - 300-500 mW (@f_{max})





- Towards *High integration Digital Control Module* (HiDCM) architecture
  - Interface with one or several standard analog ASSP for sensors management,…

SOFTWARE TOOLS (1/2)

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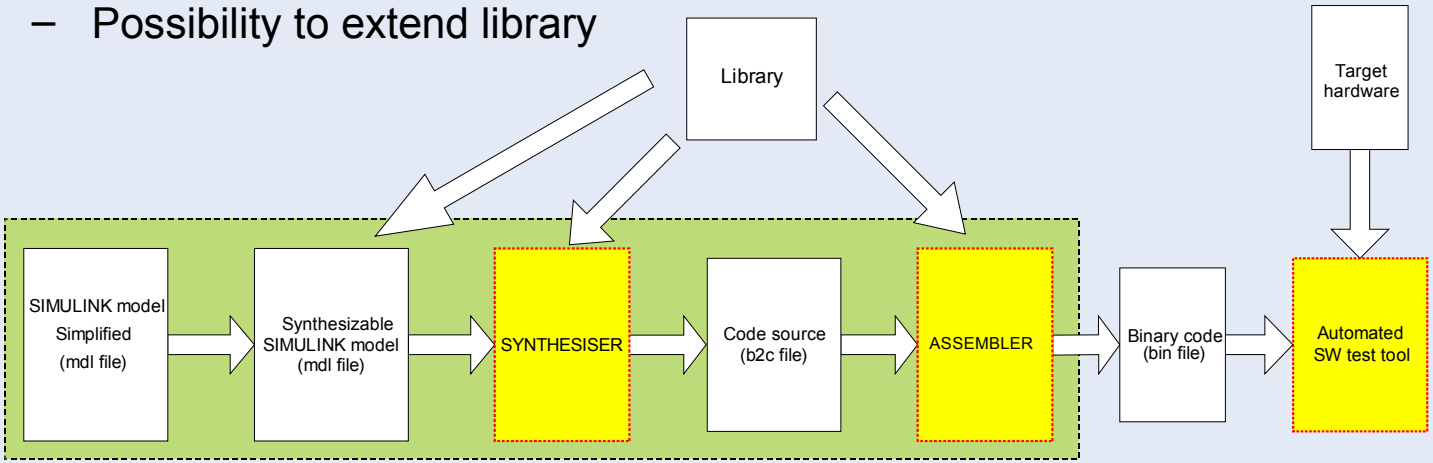
- *Application Development:*
  Simulink-based, automated code generation
  - OS-free and highly efficient code
  - No SW knowledge required
  - Fully deterministic and sequential execution
  - Static register allocation, exclusively using on-chip data memory
  - Same source for simulation and generation
- *Library SW element development:*
  Assembler-based
  - Possibility to extend library



SOFTWARE TOOLS (2/2)

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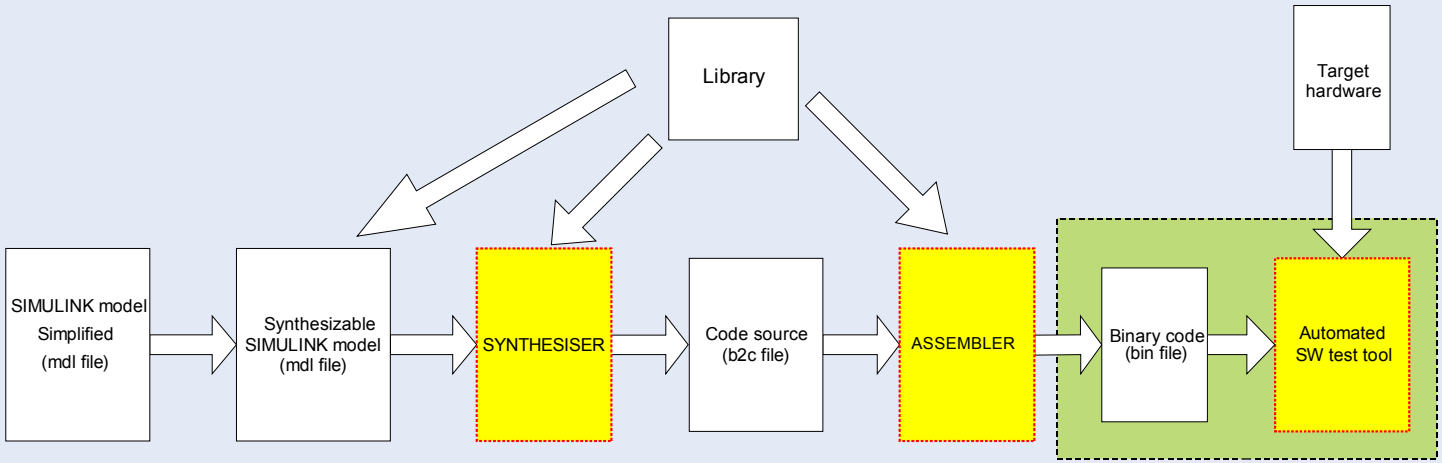
- *Application Debugging, fine-tuning and formal validation: Automated SW test tool, based on real-time reporting*
  - Operations eased by:
    - Direct correlation with Simulink simulations
    - Predictable execution of generated code
    - Code based on pre-validated (UT-passed) library elements
  - Use of SpaceWire (ESA preferred)
- *Library SW element validation: Automated SW test tool*
  - Allow unit testing with high code coverage



APPLICATIONS

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High Integration Digital Control Module
Control Loop Processor

- **Space-vehicles/spacecraft actuation control systems**
  - Thrust vector control
  - Attitude control
- **Mechanisms control systems**
  - Fine pointing applications (antenna, mirror,…)
- **Robotics**
  - Wheel steering, braking and driving systems
  - Positioning systems (flexible arm,…)
- **Active damping control systems**
- **And so on…**

CONCLUSION

S.A.B.C.A.

- **GSTP5 Element-2 program is targeted:**
  Chipset For Critical Control Loops In Space Applications
  - CLP for digital, SW-based, control
  - Analog ASSP(s) for the interface with sensors
- **Pre-requisites to start the program**
  - Consolidate applications of the product (interest shown by TEC/ED)
  - Decline requirements for CLP and analog ASSP(s)
  - Consortium covering all aspects of the life cycle of this “building block”
    - HW & SW Design, foundrie(s), component(s) validation and qualification
    - Commercialisation, support to users and long-term maintenance
- **Goals:**
  - Provide full access of the chipset (and SW tools) to the European space community
  - Cope with future ESA programs needs in line with ESA Product Policy